These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}...-0.3V to +6.0V
V+ (NOTE 1).......................................-0.3V to +7.0V
V- (NOTE 1).......................................+0.3V to -7.0V
V+ + |V-| (NOTE 1)..+13V
I_{CC} (DC V_{CC} or GND current)........................±100mA

Input Voltages
TxIN, $\overline{EN}$...-0.3V to +6.0V
RxIN...±25V
Output Voltages
TxOUT...±13.2V
RxOUT, ...-0.3V to (V_{CC} +0.3V)
Short-Circuit Duration
TxOUT...Continuous
Storage Temperature......................-65°C to +150°C

Power Dissipation per package
20-pin SSOP (derate 9.25mW/°C above +70°C)..............750mW
18-pin SOIC (derate 15.7mW/°C above +70°C).............1260mW
20-pin TSSOP (derate 11.1mW/°C above +70°C).............890mW
16-pin SSOP (derate 9.69mW/°C above +70°C)..............775mW
16-pin Wide SOIC (derate 11.2mW/°C above +70°C)........900mW
16-pin TSSOP (derate 10.5mW/°C above +70°C).............850mW
16-pin nSOIC (derate 13.57mW/°C above +70°C)...........1086mW

Maximum Junction Temperature ....+125°C
Thermal Resistance (16-pin TSSOP) Θ_{JA} ....100.4°C/W
Thermal Resistance (16-pin TSSOP) Θ_{JC} ....19.0°C/W
Thermal Resistance (16-pin QFN) Θ_{JA} .... 44.0°C/W
Thermal Resistance (16-pin QFN) Θ_{JC} ....7.3°C/W

NOTE 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.
NOTE 2: Driver Input hysteresis is typically 250mV.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.5V with T_{AMB} = T_{MIN} to T_{MAX}, C1 - C4 = 0.1μF.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC CHARACTERISTICS					
Supply Current		0.3	1.0	mA	no load, V_{CC} = 3.3V, T_{AMB} = 25°C, TxIN = GND or V_{CC}
Shutdown Supply Current		1.0	10	μA	$\overline{SHDN}$ = GND, VCC = 3.3V, T_{AMB} = 25°C, TxIN = Vcc or GND
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW	GND		0.8	V	TxIN, $\overline{EN}$, $\overline{SHDN}$, Note 2
Input Logic Threshold HIGH	2.0		Vcc	V	Vcc = 3.3V, Note 2
Input Logic Threshold HIGH	2.4		Vcc	V	Vcc = 5.0V, Note 2
Input Leakage Current		±0.01	±1.0	μA	TxIN, $\overline{EN}$, $\overline{SHDN}$, T_{AMB} = +25°C, V_{IN} = 0V to V_{CC}
Output Leakage Current		±0.05	±10	μA	Receivers disabled, V_{OUT} = 0V to V_{CC}
Output Voltage LOW			0.4	V	I_{OUT} = 1.6mA
Output Voltage HIGH	V_{CC} -0.6	V_{CC} -0.1		V	I_{OUT} = -1.0mA
DRIVER OUTPUTS					
Output Voltage Swing	±5.0	±5.4		V	All driver outputs loaded with 3kΩ to GND, T_{AMB} = +25°C

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.5V with T_{AMB} = T_{MIN} to T_{MAX}, C1 - C4 = 0.1µF. Typical values apply at V_{CC} = +3.3V or +5.0V and T_{AMB} = 25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER OUTPUTS (continued)					
Output Resistance	300			Ω	V_{CC} = V+ = V- = 0V, V_{OUT}=$\pm$2V
Output Short-Circuit Current		$\pm$35	$\pm$60	mA	V_{OUT} = 0V
Output Leakage Current			$\pm$25	µA	V_{CC} = 0V or 3.0V to 5.5V, V_{OUT} = $\pm$12V, Drivers disabled
RECEIVER INPUTS					
Input Voltage Range	-15		15	V	
Input Threshold LOW	0.6	1.2		V	Vcc = 3.3V
Input Threshold LOW	0.8	1.5		V	Vcc = 5.0V
Input Threshold HIGH		1.5	2.4	V	Vcc = 3.3V
Input Threshold HIGH		1.8	2.4	V	Vcc = 5.0V
Input Hysteresis		0.3		V	
Input Resistance	3	5	7	kΩ	
TIMING CHARACTERISTICS					
Maximum Data Rate	250			kbps	R_L = 3kΩ, C_L = 1000pF, one driver active
Receiver Propagation Delay, t_{PHL}		0.15		µs	Receiver input to Receiver output, C_L = 150pF
Receiver Propagation Delay, t_{PLH}		0.15		µs	Receiver input to Receiver output, C_L = 150pF
Receiver Output Enable Time		200		ns	
Receiver Output Disable Time		200		ns	
Driver Skew		100		ns	$\| t_{PHL} - t_{PLH} \|$, T_{AMB} = 25°C
Receiver Skew		50		ns	$\| t_{PHL} - t_{PLH} \|$
Transition-Region Slew Rate			30	V/µs	Vcc = 3.3V, R_L = 3kΩ, C_L = 1000pF, T_{AMB} = 25°C, measurements taken from -3.0V to +3.0V or +3.0V to -3.0V

Unless otherwise noted, the following performance characteristics apply for V_{CC} = +3.3V, 1000kbps data rate, all drivers loaded with 3kΩ, 0.1μF charge pump capacitors, and T_{AMB} = +25°C.

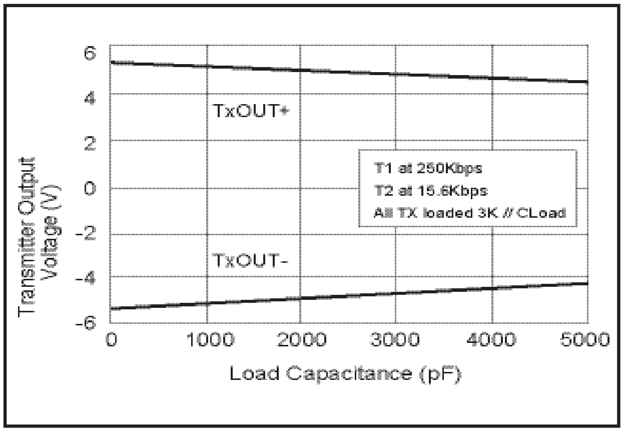


Figure 1. Transmitter Output Voltage vs Load Capacitance

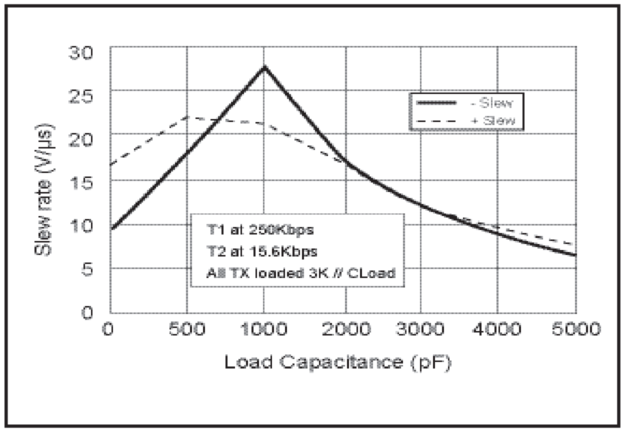


Figure 2. Slew Rate vs Load Capacitance

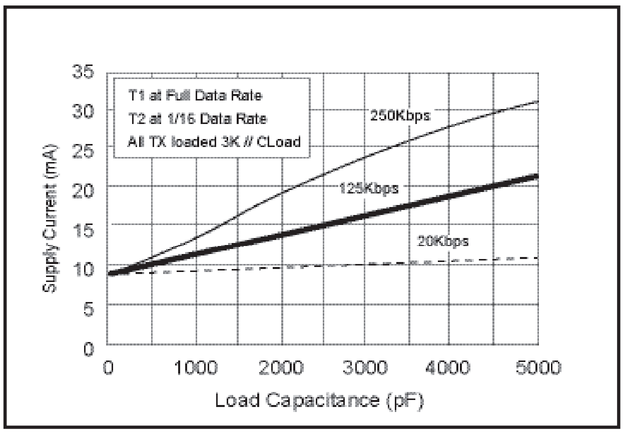


Figure 3. Supply Current VS. Load Capacitance when Transmitting Data

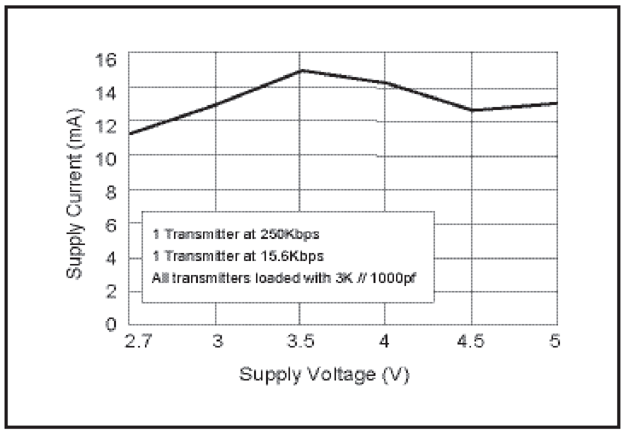


Figure 4. Supply Current VS. Supply Voltage

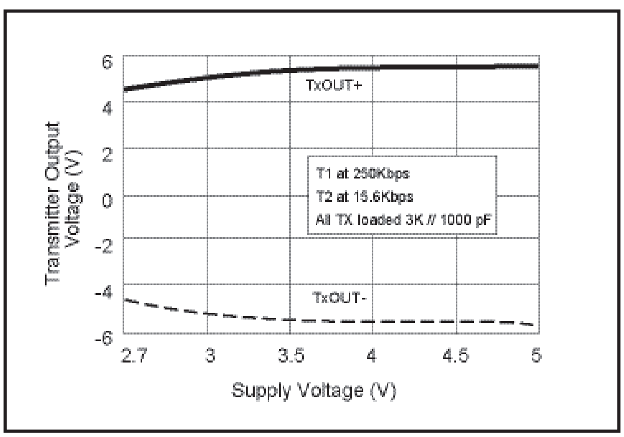


Figure 5. Transmitter Output Voltage vs Supply Voltage

NAME	FUNCTION	PIN NUMBER			
		SP3222EB		SP3232EB	
		SOIC	SSOP TSSOP	SSOP TSSOP NSOIC WSOIC	QFN
$\overline{EN}$	Receiver Enable. Apply Logic LOW for normal operation. Apply logic HIGH to disable the receiver outputs (high-Z state)	1	1	-	-
C1+	Positive terminal of the voltage doubler charge-pump capacitor	2	2	1	15
V+	+5.5V output generated by the charge pump	3	3	2	16
C1-	Negative terminal of the voltage doubler charge-pump capacitor	4	4	3	1
C2+	Positive terminal of the inverting charge-pump capacitor	5	5	4	2
C2-	Negative terminal of the inverting charge-pump capacitor	6	6	5	3
V-	-5.5V output generated by the charge pump	7	7	6	4
T_1OUT	RS-232 driver output.	15	17	14	12
T_2OUT	RS-232 driver output.	8	8	7	5
R_1IN	RS-232 receiver input	14	16	13	11
R_2IN	RS-232 receiver input	9	9	8	6
R_1OUT	TTL/CMOS receiver output	13	15	12	10
R_2OUT	TTL/CMOS receiver output	10	10	9	7
T_1IN	TTL/CMOS driver input	12	13	11	9
T_2IN	TTL/CMOS driver input	11	12	10	8
GND	Ground.	16	18	15	13
V_{CC}	+3.0V to +5.5V supply voltage	17	19	16	14
$\overline{SHDN}$	Shutdown Control Input. Drive HIGH for normal device operation. Drive LOW to shutdown the drivers (high-Z output) and the on-board power supply	18	20	-	-
N.C.	No Connect	-	11, 14	-	-

Table 1. Device Pin Description

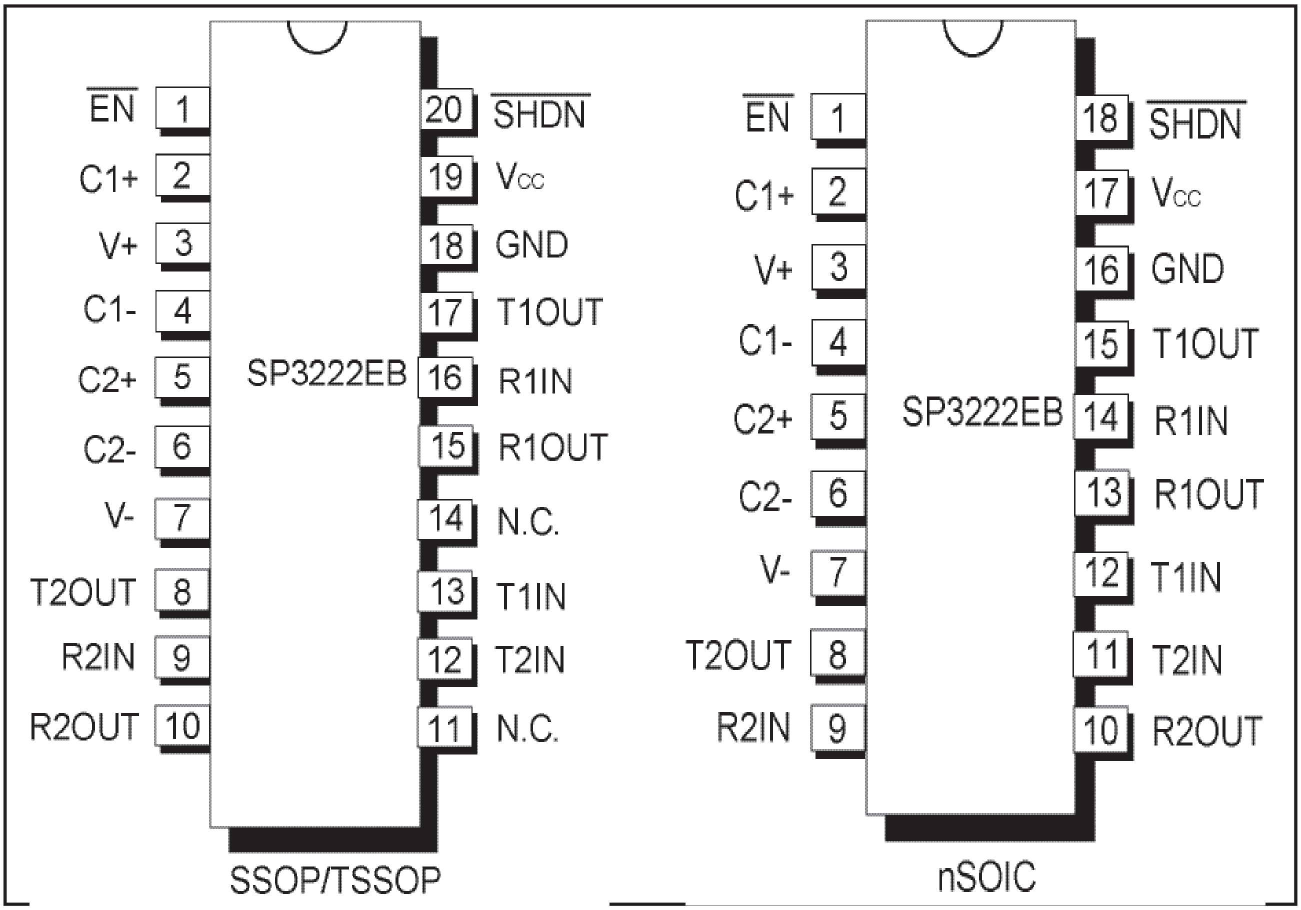


Figure 6. Pinout Configurations for the SP3222EB

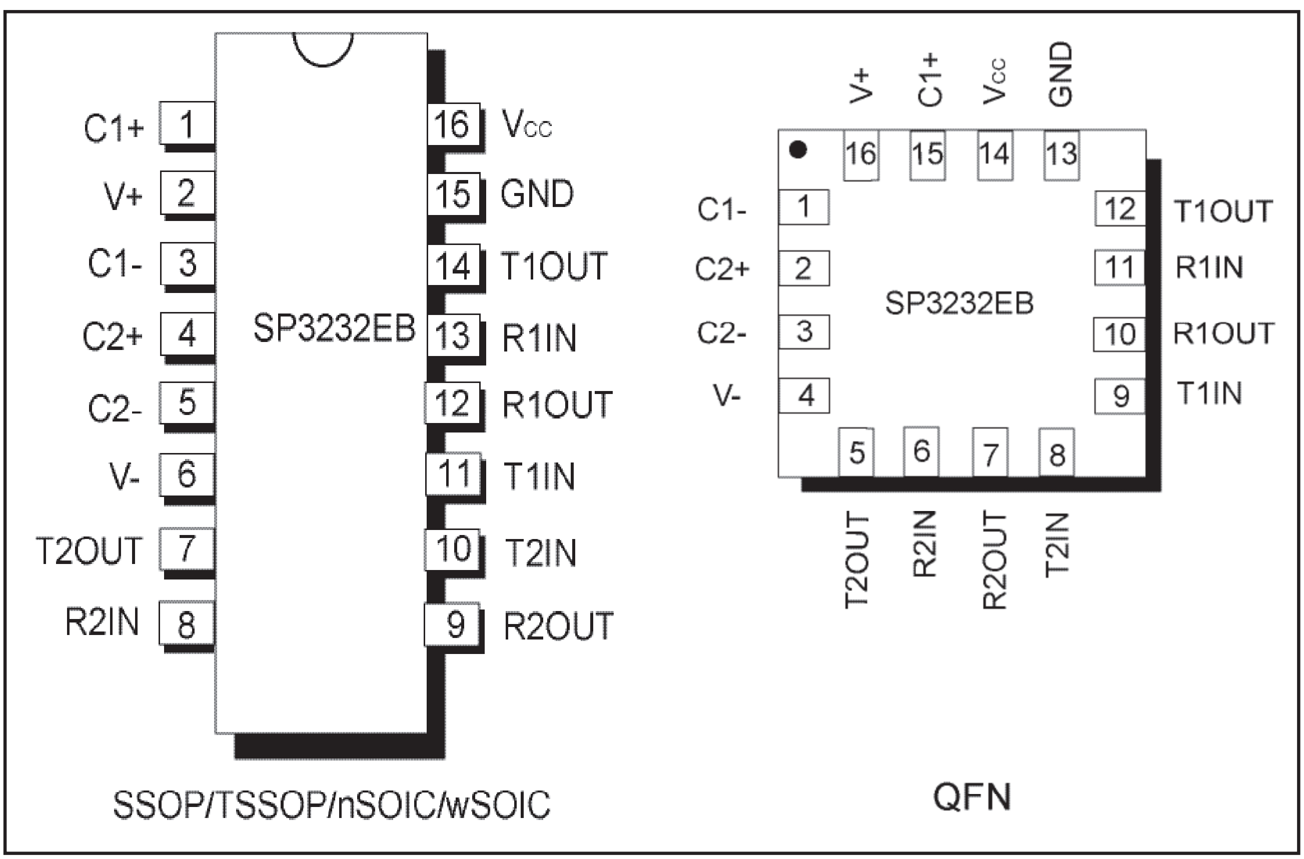
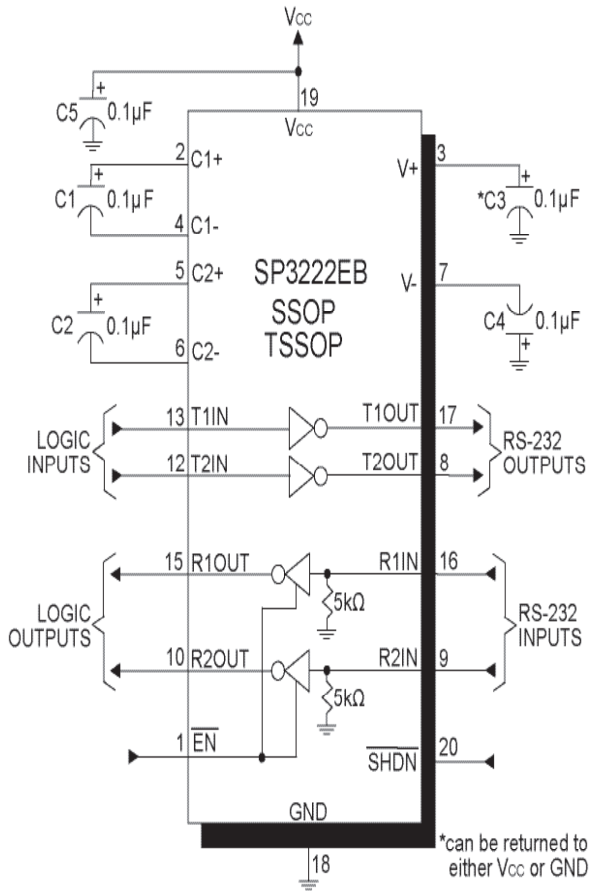


Figure 7. Pinout Configuration for the SP3232EB



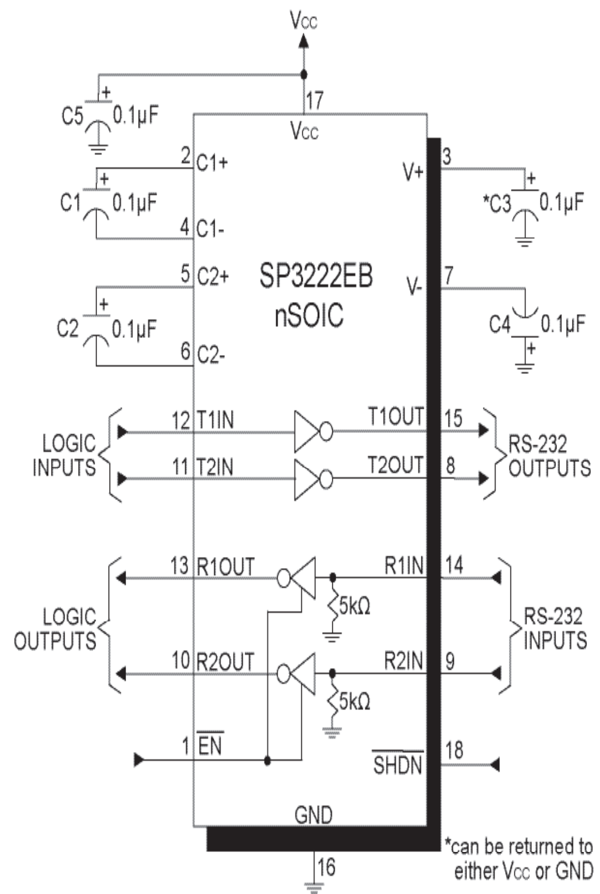


Figure 8. SP3222EB Typical Operating Circuits

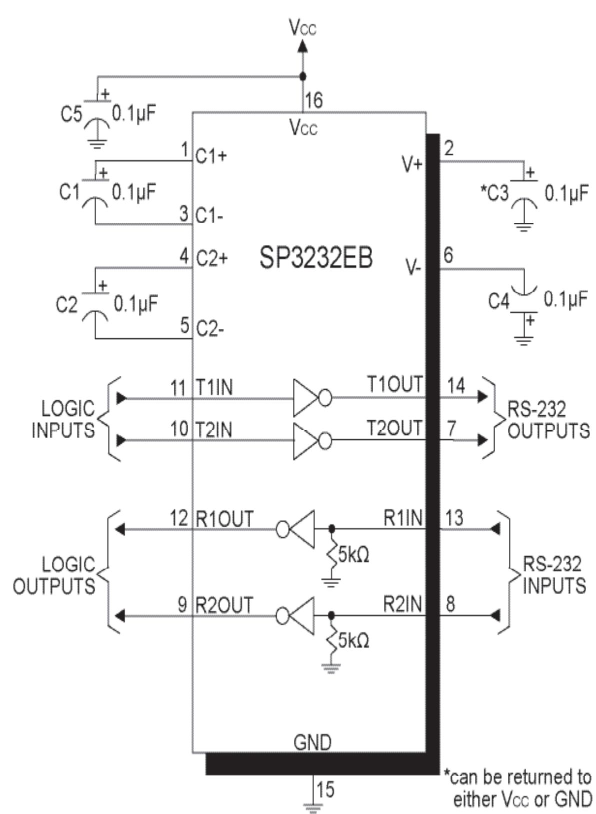


Figure 9. SP3232EB Typical Operating Circuit

The **SP3222EB/SP3232EB** transceivers meet the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The **SP3222EB/SP3232EB** devices feature **Exar's** proprietary on-board charge pump circuitry that generates ±5.5V for RS-232 voltage levels from a single +3.0V to +5.5V power supply. This series is ideal for +3.3V-only systems, mixed +3.3V to +5.5V systems, or +5.0V-only systems that require true RS-232 performance. The **SP3222EB/SP3232EB** devices can operate at a data rate of 250kbps when fully loaded.

The **SP3222EB** and **SP3232EB** are 2-driver/2-receiver devices ideal for portable or hand-held applications. The **SP3222EB** features a 1µA shutdown mode that reduces power consumption and extends battery life in portable systems. Its receivers remain active in shutdown mode, allowing external devices such as modems to be monitored using only 1µA supply current.

THEORY OF OPERATION

The **SP3222EB/SP3232EB** series is made up of three basic circuit blocks:

1. Drivers
2. Receivers
3. The Exar proprietary charge pump

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to $\pm$5.0V EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is $\pm$5.4V with no load and $\pm$5V minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. Driver outputs will meet EIA/TIA-562 levels of +/-3.7V with supply voltages as low as 2.7V.

The drivers can guarantee a data rate of 250kbps fully loaded with 3kΩ in parallel with 1000pF, ensuring compatability with PC-to-PC communication software.

The slew rate of the driver is internally limited to a maximum of 30V/µs in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from HIGH to LOW also meet the monotonicity requirements of the standard.

Figure 10 shows a loopback test circuit used to test the RS-232 Drivers. Figure 11 shows the test results of the loopback circuit with all drivers active at 120kbps with RS-232 loads in parallel with a 1000pF capacitor. Figure 12 shows the test results where one driver was active at 250kbps and all drivers loaded with an RS-232 receiver in parallel with 1000pF capacitors. A solid RS-232 data transmission rate of 250kbps provides compatibility with many designs in personal computer peripherals and LAN applications.

The **SP3222EB** driver's output stages are turned off (tri-state) when the device is in shutdown mode. When the power is off, the **SP3222EB** device permits the outputs to be driven up to +/-12V. The driver's inputs do not have pull-up resistors. Designers should connect unused inputs to Vcc or GND.

In the shutdown mode, the supply current falls to less than 1µA, where $\overline{\text{SHDN}}$ = LOW. When the **SP3222EB** device is shut down, the device's driver outputs are disabled (tri-stated) and the charge pumps are turned off with V+ pulled down to Vcc and V- pulled to GND. The time required to exit shutdown is typically 100µs. Connect $\overline{\text{SHDN}}$ to Vcc if the shutdown mode is not used.

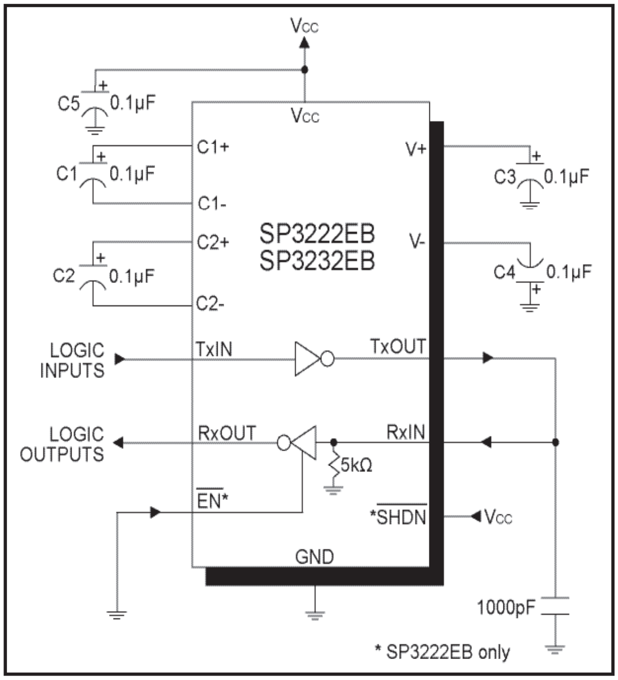


Figure 10. SP3222EB/SP3232EB Driver Loopback Test Circuit

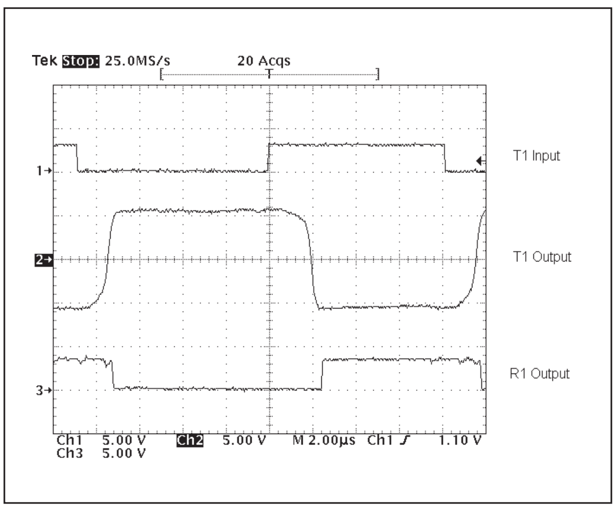


Figure 11. Loopback Test results at 120kbps

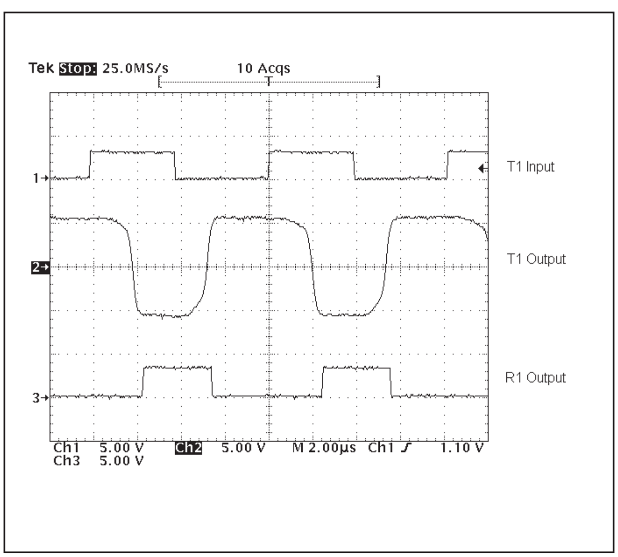


Figure 12. Loopback Test results at 250kbps

Receivers

The Receivers convert EIA/TIA-232 levels to TTL or CMOS logic output levels. The **SP3222EB** receivers have an inverting tri-state output. These receiver outputs (RxOUT) are tri-stated when the enable control $\overline{EN}$ = HIGH. In the shutdown mode, the receivers can be active or inactive. $\overline{EN}$ has no effect on TxOUT. The truth table logic of the **SP3222EB** driver and receiver outputs can be found in Table 2.

$\overline{SHDN}$	$\overline{EN}$	TxOUT	RxOUT
0	0	Tri-state	Active
0	1	Tri-state	Tri-state
1	0	Active	Active
1	1	Active	Tri-state

Table 2. SP3222EB Truth Table Logic for Shutdown and Enable Control

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal 5kΩ pulldown resistor to ground will commit the output of the receiver to a HIGH state.

Charge Pump

The charge pump is an Exar-patended design (U.S. 5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages of +/-5.5V regardless of the input voltage (Vcc) over the +3.0V to +5.5V range.

In most circumstances, decoupling the power supply can be achieved adequately using a 0.1µF bypass capacitor at C5 (refer to figures 8 and 9)

In applications that are sensitive to power-supply noise, decouple Vcc to ground with a capacitor of the same value as charge-pump capacitor C1. Physically connect bypass capcitors as close to the IC as possible.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pump is enabled. If the output voltages exceed a magnitude of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC}. C_l^+ is then switched to GND and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to V_{CC}, the voltage potential across capacitor C_2 is now 2 times V_{CC}.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to GND. This transfers a negative generated voltage to C_3. This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C_3, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces $-V_{CC}$ in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at V_{CC}, the voltage potential across C_2 is 2 times V_{CC}.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to GND, and transfers this positive generated voltage across C_2 to C_4, the V_{DD} storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C_4, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V^+ and V^- are separately generated from V_{CC}, in a no–load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at greater than 250kHz. The external capacitors can be as low as 0.1µF with a 16V breakdown voltage rating.

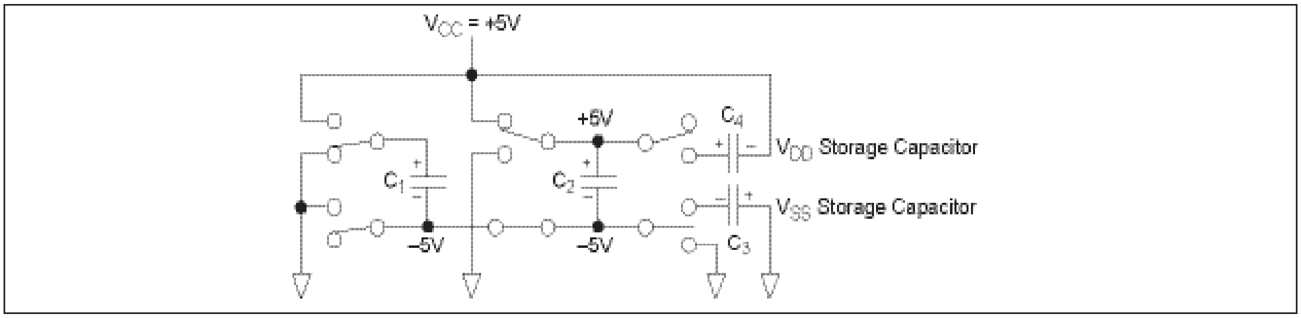


Figure 13. Charge Pump — Phase 1

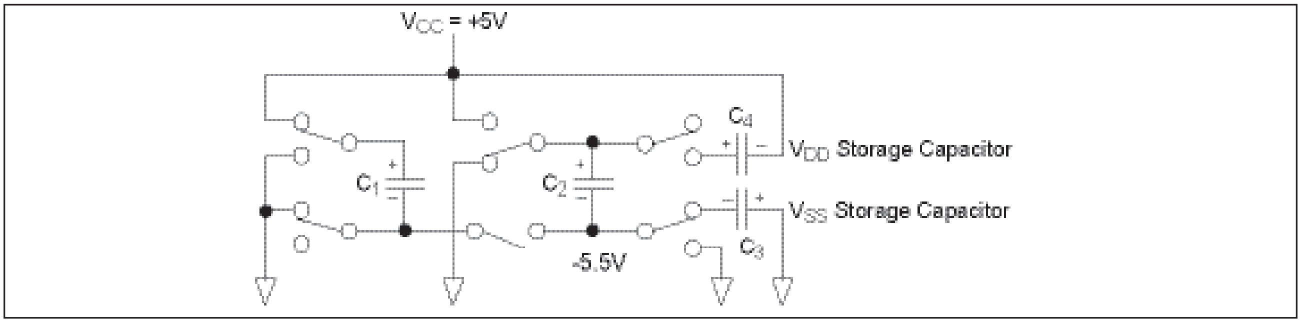


Figure 14. Charge Pump — Phase 2

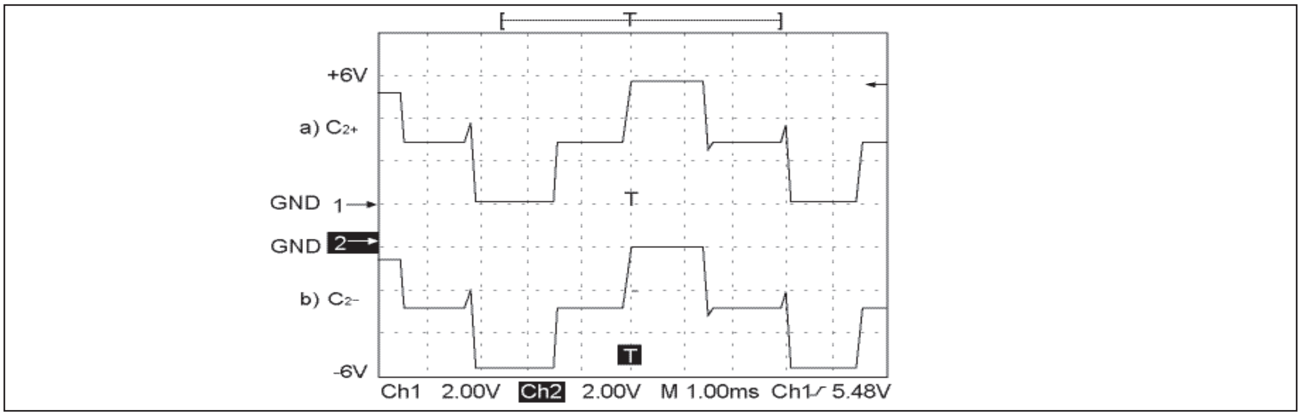


Figure 15. Charge Pump Waveforms

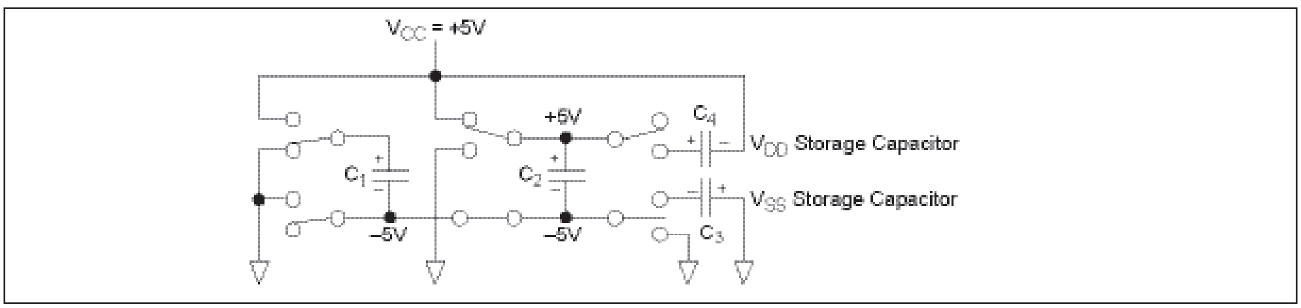


Figure 16. Charge Pump — Phase 3

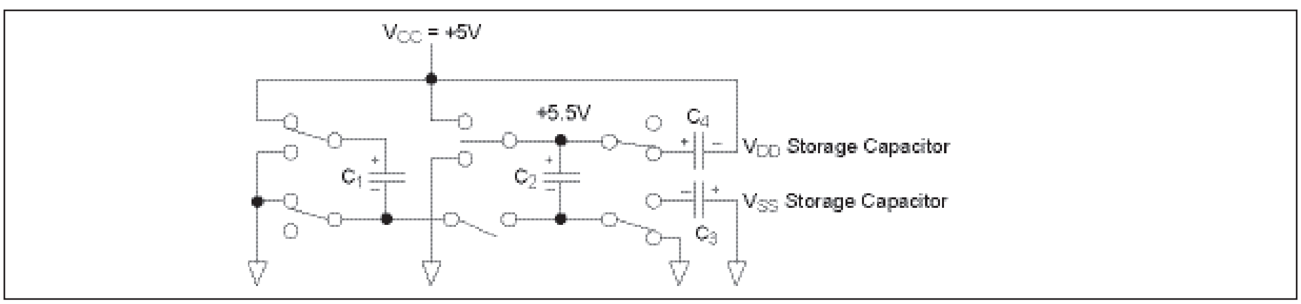


Figure 17. Charge Pump — Phase 4

ESD TOLERANCE

The **SP3222EB/SP3232EB** series incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least $\pm$15kV without damage nor latch-up.

There are different methods of ESD testing applied:

a) MIL-STD-883, Method 3015.7
b) IEC61000-4-2 Air-Discharge
c) IEC61000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semi-conductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 18. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-61000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC61000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC61000-4-2 is shown on Figure 19. There are two methods within IEC61000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the

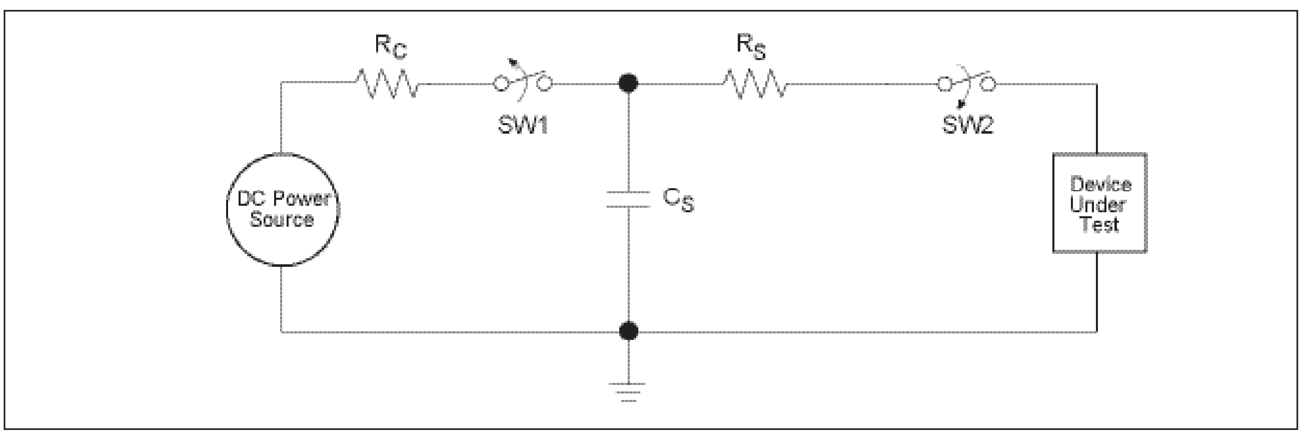


Figure 18. ESD Test Circuit for Human Body Model

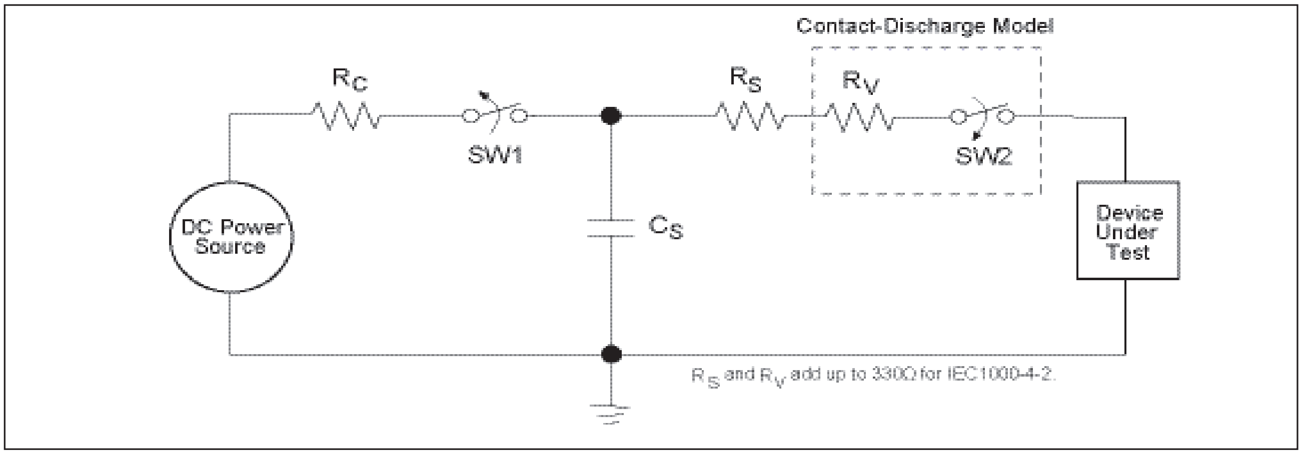


Figure 19. ESD Test Circuit for IEC61000-4-2

equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

The circuit models in Figures 18 and 19 represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S, the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ an 100pF, respectively. For IEC-61000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330Ω an 150pF, respectively.

The higher C_S value and lower R_S value in the IEC61000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

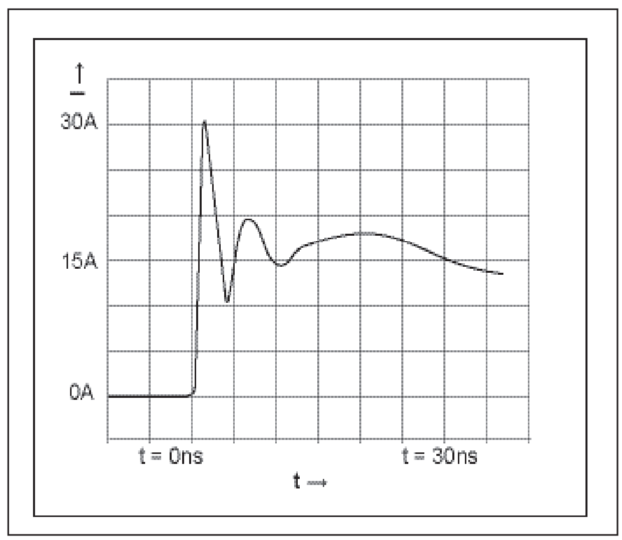
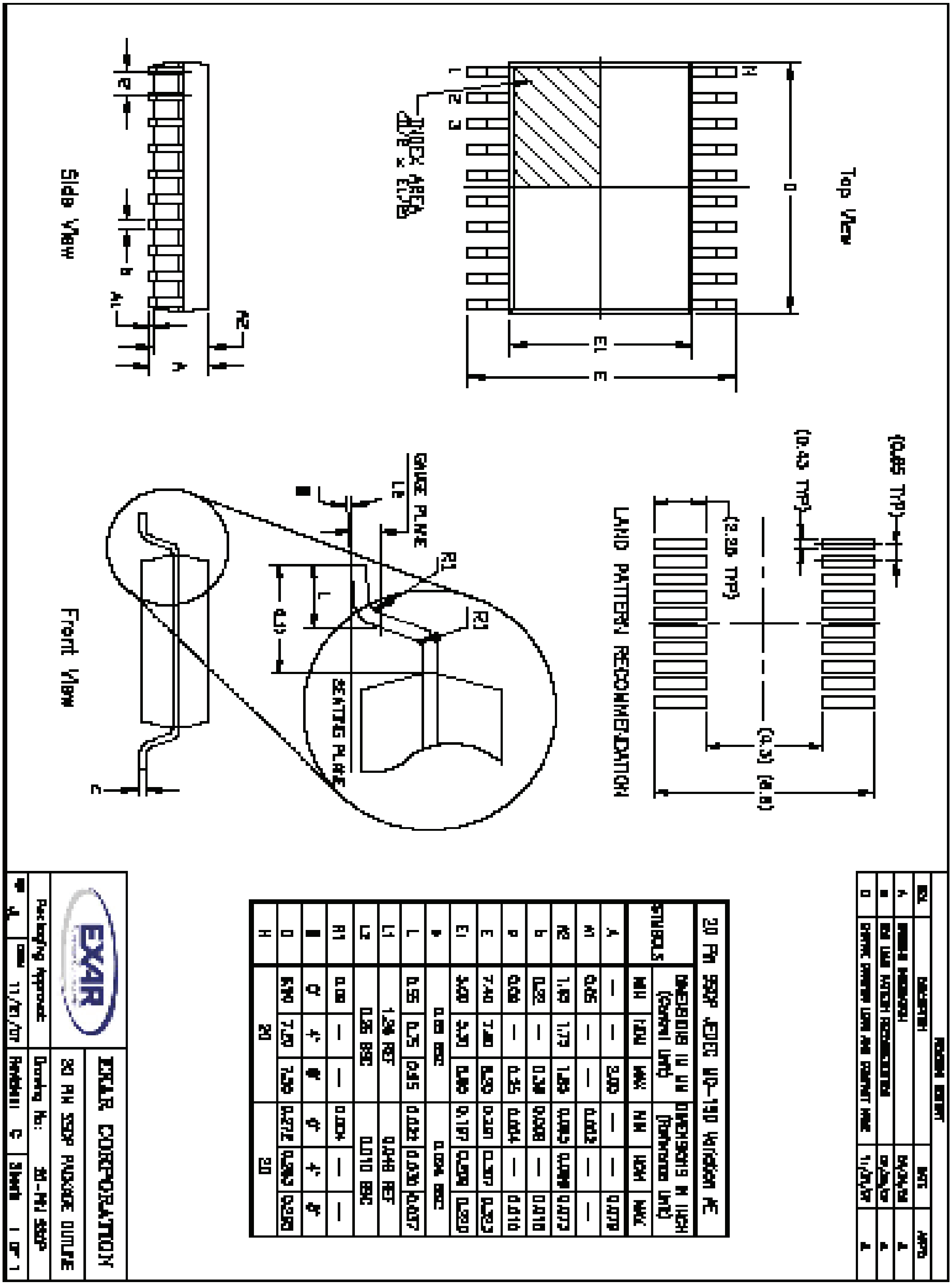


Figure 20. ESD Test Waveform for IEC61000-4-2

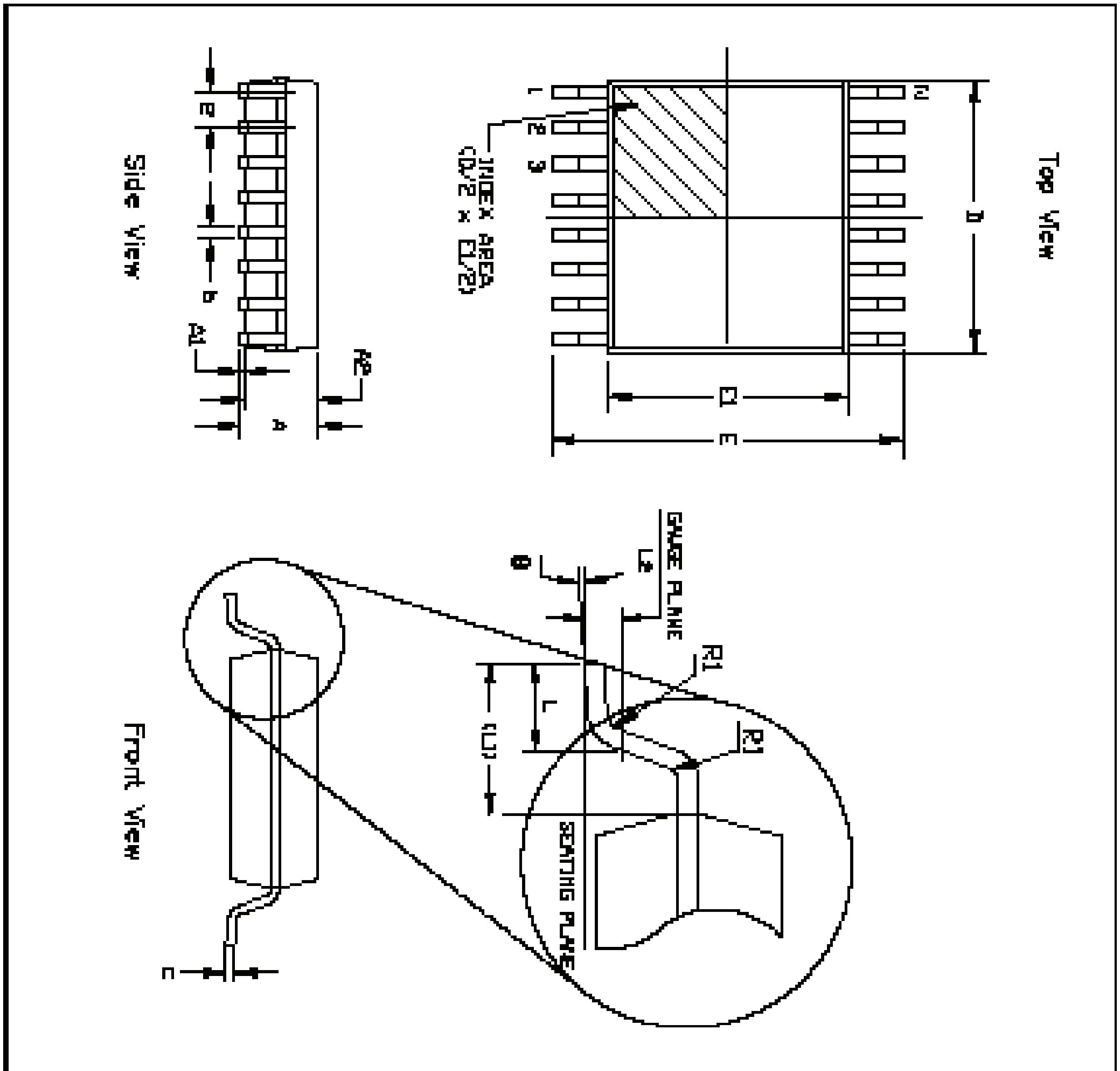
DEVICE PIN TESTED	HUMAN BODY MODEL	IEC61000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	±15kV	±15kV	±8kV	4
Receiver Inputs	±15kV	±15kV	±8kV	4

Table 3. Transceiver ESD Tolerance Levels



20 Pin SSOP JEDEC MO-150 Variation AE

SYMBOLS	DIMENSIONS IN MM (Control Unit) MIN	NOM	MAX	DIMENSIONS IN INCH (Reference Unit) MIN	NOM	MAX
A	—	—	2.00	—	—	0.079
A1	0.05	—	—	0.002	—	—
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	—	0.38	0.009	—	0.015
c	0.09	—	0.25	0.004	—	0.010
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
e	0.65 BSC			0.026 BSC		
L	0.55	0.75	0.95	0.022	0.030	0.037
L1	1.25 REF			0.049 REF		
L2	0.25 BSC			0.010 BSC		
R1	0.09	—	—	0.004	—	—
θ	0°	4°	8°	0°	4°	8°
D	6.90	7.20	7.50	0.272	0.283	0.295
N	20			20		



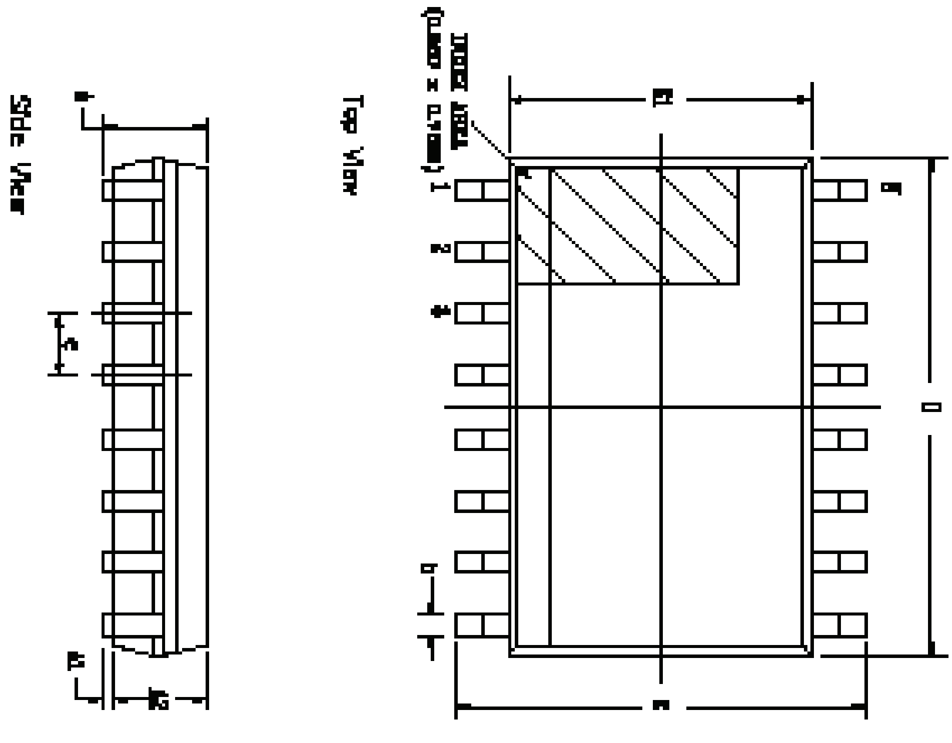
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	2.00	—	—	0.078
A1	0.05	—	—	0.002	—	—
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	—	0.38	0.009	—	0.015
c	0.09	—	0.25	0.004	—	0.010
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
e	0.65 BSC			0.026 BSC		
L	0.55	0.75	0.95	0.022	0.030	0.037
L1	1.25 REF			0.049 REF		
L2	0.25 BSC			0.010 BSC		
R1	0.09	—	—	0.004	—	—
θ	0°	4°	8°	0°	4°	8°
D	5.90	6.20	6.50	0.232	0.244	0.256
N	16			16		

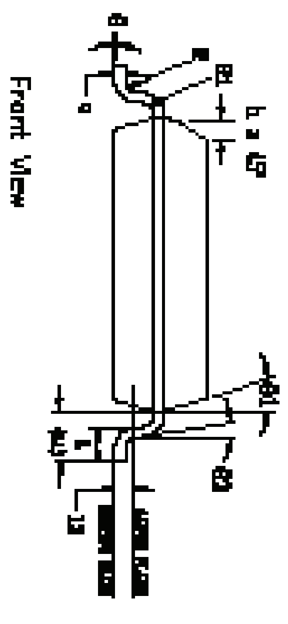
16 Pin SSOP JEDEC MO-150 Variation AC

EXAR CORPORATION

16 PIN SSOP PACKAGE OUTLINE

Packaging Approval: | Drawing No: 16-PIN SSOP | Date 11/21/07 | Revision B | Sheet 1 OF 1





16 Pin SOICW JEDEC MS-013 Variation AA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	—	2.65	0.093	—	0.104
A1	0.10	—	0.30	0.004	—	0.012
A2	2.05	—	2.55	0.081	—	0.100
b	0.31	—	0.51	0.012	—	0.020
c	0.20	—	0.33	0.008	—	0.013
E	10.30 BSC			0.406 BSC		
E1	7.50 BSC			0.295 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.75	0.010	—	0.029
L	0.40	—	1.27	0.016	—	0.050
L1	1.40 REF			0.055 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	10.30 BSC			0.406 BSC		
N	16			16		

EXAR CORPORATION

16 PIN SOICW PACKAGE OUTLINE

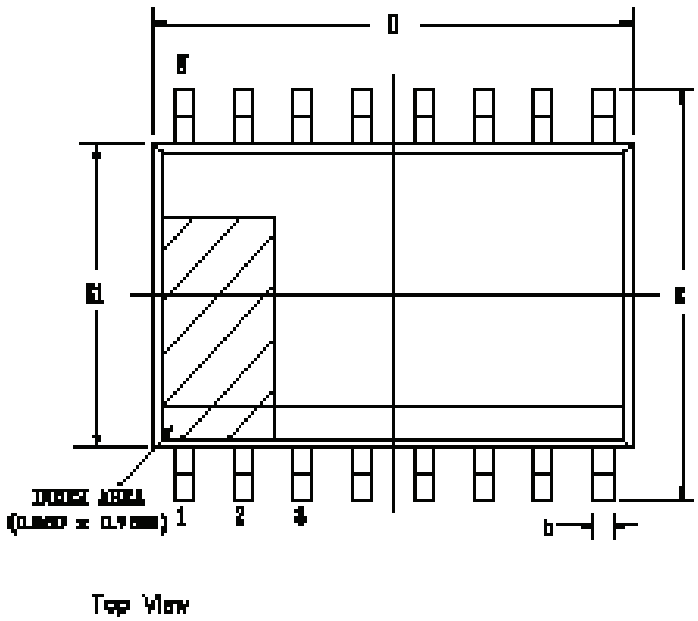
Packaging Approval:

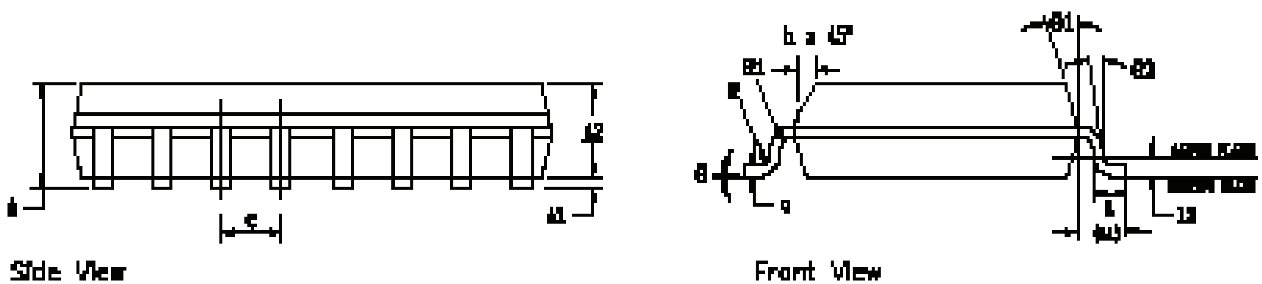
Drawing No: 16-PIN SOICW

Revision: C

Sheet: 1 OF 1

REVISION HISTORY			
REV.	DESCRIPTION	DATE	APP'D
A	INITIAL RELEASE	[illegible]	[illegible]
B	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	[illegible]





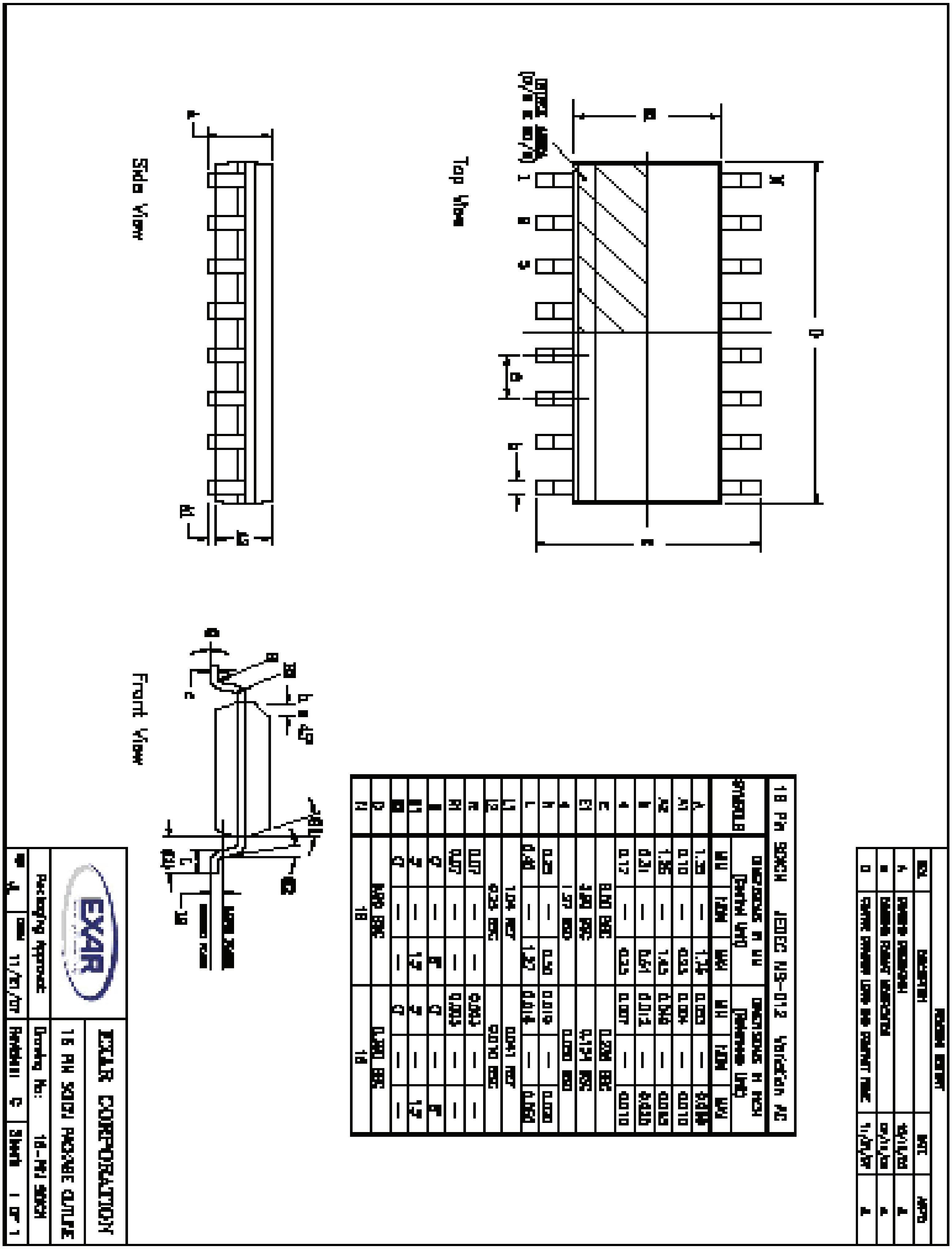
18 Pin SOICW JEDEC MS-013 Variation AB						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	—	2.65	0.093	—	0.104
A1	0.10	—	0.30	0.004	—	0.012
A2	2.05	—	2.55	0.081	—	0.100
b	0.31	—	0.51	0.012	—	0.020
c	0.20	—	0.33	0.008	—	0.013
E	10.30 BSC			0.406 BSC		
E1	7.50 BSC			0.295 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.75	0.010	—	0.030
L	0.40	—	1.27	0.016	—	0.050
L1	1.40 REF			0.055 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	11.55 BSC			0.455 BSC		
N	18			18		

EXAR CORPORATION

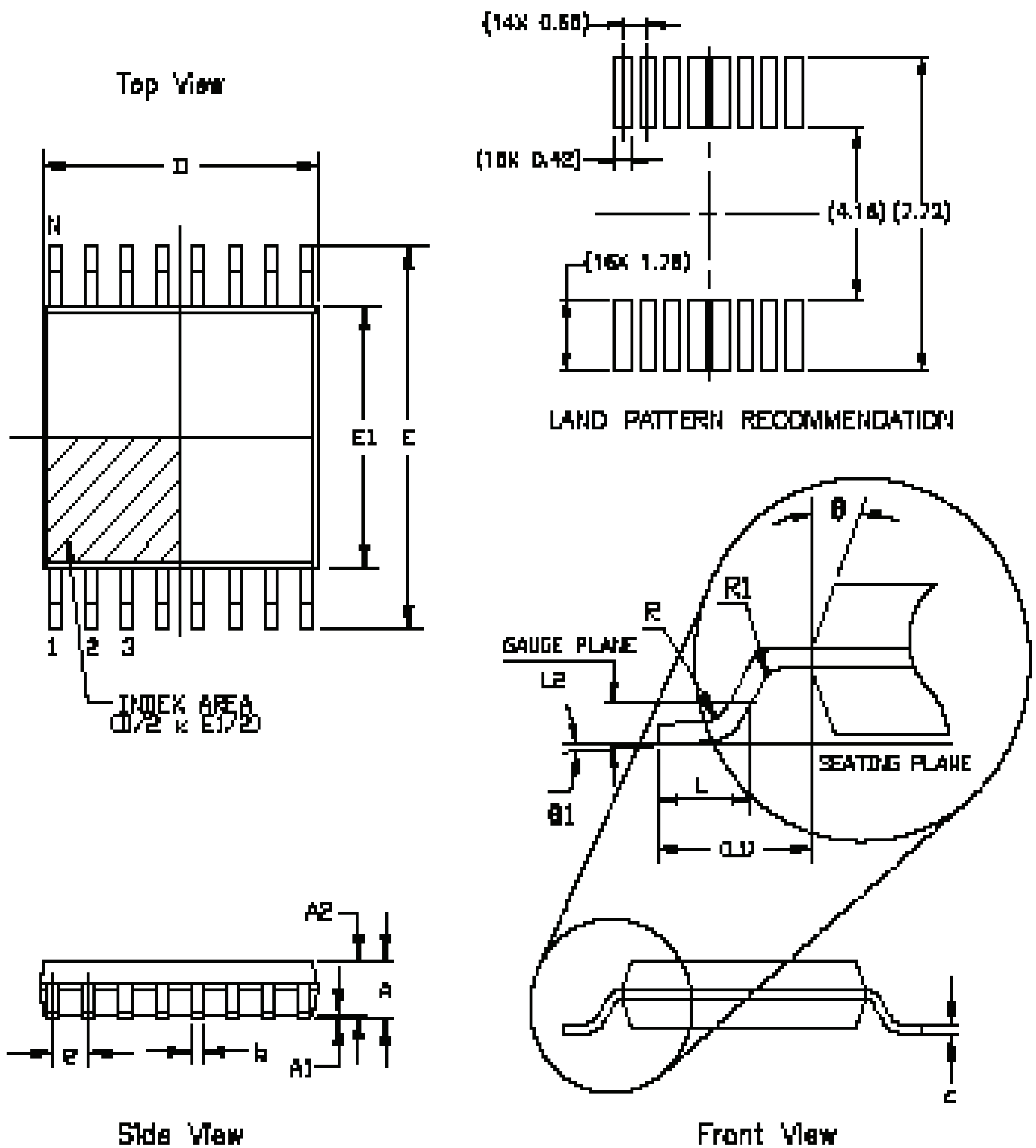
18 PIN SOICW PACKAGE OUTLINE

Packaging Approval: | Drawing No: 18-PIN SOICW

Revision: B | Sheet 1 OF 1 | 11/21/07



16 Pin SOICN JEDEC MS-012 Variation AC						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	9.90 BSC			0.390 BSC		
N	16			16		



REV.	DESCRIPTION	DATE	APPD
A	INITIAL REVISION	[illegible]	[illegible]
B	ADD LAND PATTERN RECOMMENDATION	[illegible]	[illegible]
C	CHANGE DRAWING LOGO AND COMPANY NAME	11/[illegible]/07	[illegible]

16 Pin TSSOP JEDEC MO-153 Variation AB

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	—	0.30	0.007	—	0.012
c	0.09	—	0.20	0.004	—	0.008
E	6.40 BSC			0.252 BSC		
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
L2	0.25 BSC			0.010 BSC		
R	0.09	—	—	0.0035	—	—
R1	0.09	—	—	0.0035	—	—
θ	12° REF			12° REF		
θ1	0°	—	8°	0°	—	8°
D	4.90	5.00	5.10	0.193	0.197	0.201
N	16			16		

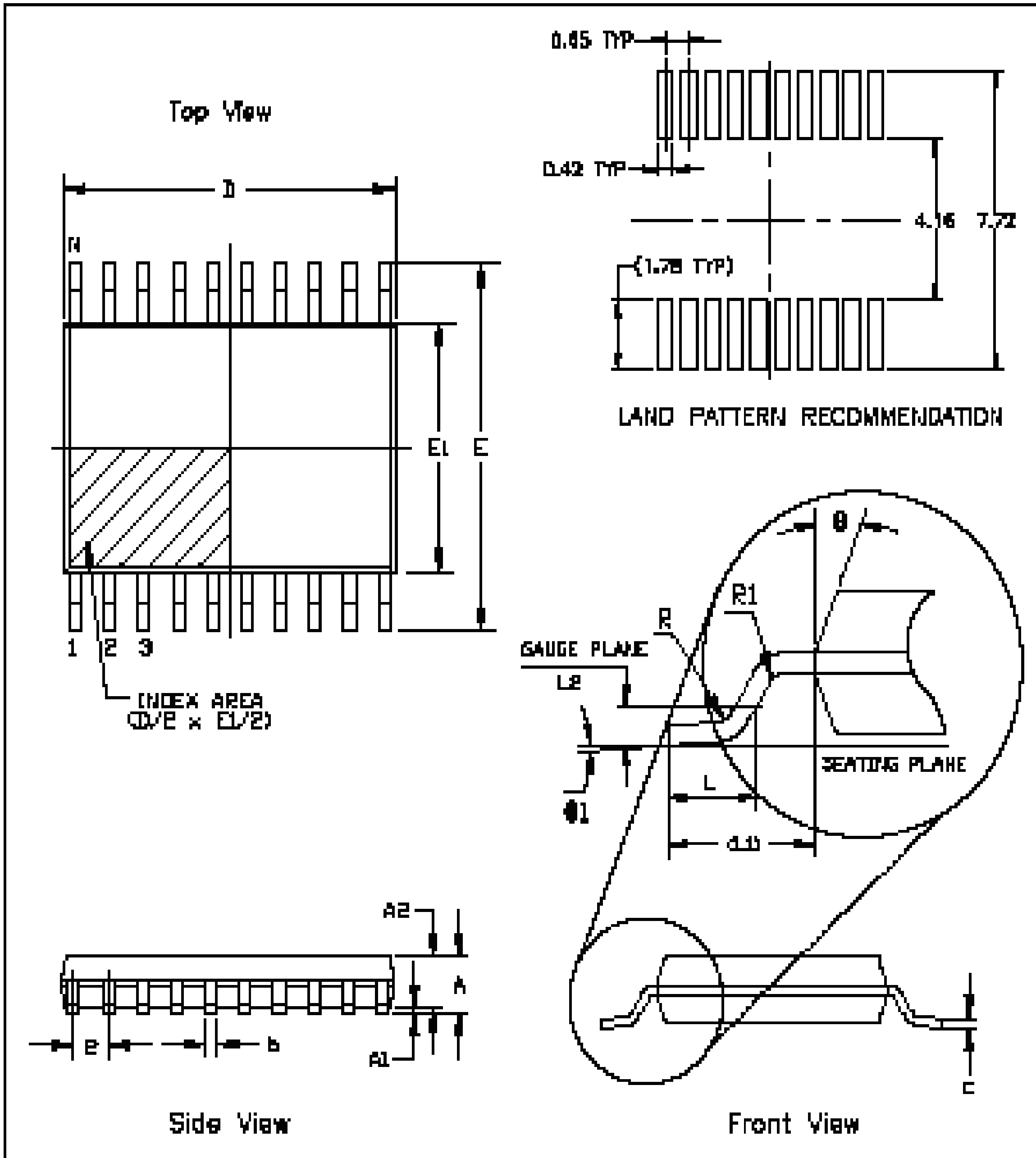
EXAR CORPORATION

16 PIN TSSOP PACKAGE OUTLINE

Packaging Approval

Drawing No: 16-PIN TSSOP

DATE 11/[illegible]/07 | Revision: C | Sheet 1 OF 1



20 Pin TSSOP JEDEC MO-153 Variation AC						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	—	0.30	0.007	—	0.012
c	0.09	—	0.20	0.004	—	0.008
E	6.40 BSC			0.252 BSC		
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
L2	0.25 BSC			0.010 BSC		
R	0.09	—	—	0.004	—	—
R1	0.09	—	—	0.004	—	—
θ	12° REF			12° REF		
θ1	0°	—	8°	0°	—	8°
D	6.40	6.50	6.60	0.252	0.256	0.260
N	20			20		

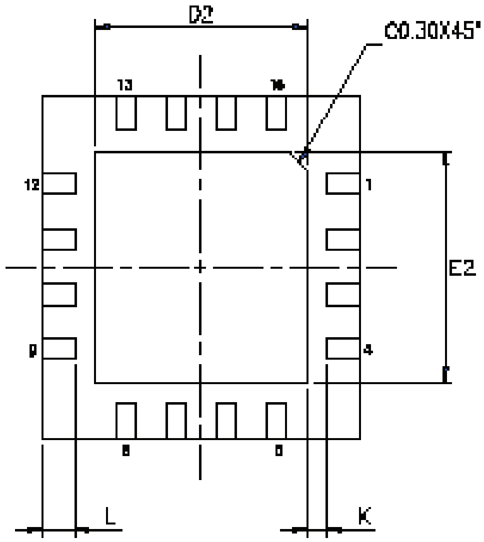
REVISION HISTORY

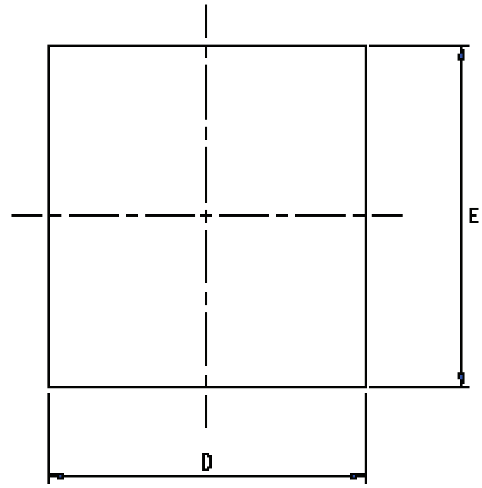
EXAR CORPORATION

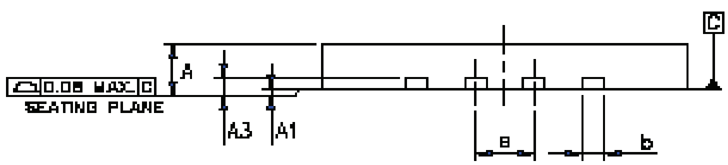
20 PIN TSSOP PACKAGE OUTLINE

Packaging Approval: | Drawing No: 20-PIN TSSOP

Date 11/01/07 | Revision: C | Sheet 1 OF 1







	PACKAGE TYPE		
JEDEC OUTLINE	MO-220		
PKG CODE	VQFN(Y516)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.25	0.30	0.35
D	4.85	5.00	5.05
E	4.95	5.00	5.05
e	0.80 BSC		
L	0.45	0.50	0.55
K	0.20	—	—

	E2			D2			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
142X142 MIL	3.28	3.38	3.43	3.28	3.38	3.43	V	X	N/A

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Part Number	Temp. Range	Package
SP3222EBCA-L	0°C to +70°C	20 Pin SSOP
SP3222EBCA-L/TR	0°C to +70°C	20 Pin SSOP
SP3222EBCT-L	0°C to +70°C	18 Pin WSOIC
SP3222EBCT-L/TR	0°C to +70°C	18 Pin WSOIC
SP3222EBCY-L	0°C to +70°C	20 Pin TSSOP
SP3222EBCY-L/TR	0°C to +70°C	20 Pin TSSOP
SP3222EBEA-L	-40°C to +85°C	20 Pin SSOP
SP3222EBEA-L/TR	-40°C to +85°C	20 Pin SSOP
SP3222EBET-L	-40°C to +85°C	18 Pin WSOIC
SP3222EBET-L/TR	-40°C to +85°C	18 Pin WSOIC
SP3222EBEY-L	-40°C to +85°C	20 Pin TSSOP
SP3222EBEY-L/TR	-40°C to +85°C	20 Pin TSSOP

Part Number	Temp. Range	Package
SP3232EBCA-L	0°C to +70°C	16 Pin SSOP
SP3232EBCA-L/TR	0°C to +70°C	16 Pin SSOP
SP3232EBCN-L	0°C to +70°C	16 Pin NSOIC
SP3232EBCN-L/TR	0°C to +70°C	16 Pin NSOIC
SP3232EBCT-L	0°C to +70°C	16 Pin WSOIC
SP3232EBCT-L/TR	0°C to +70°C	16 Pin WSOIC
SP3232EBCY-L	0°C to +70°C	16 Pin TSSOP
SP3232EBCY-L/TR	0°C to +70°C	16 Pin TSSOP
SP3232EBEA-L	-40°C to +85°C	16 Pin SSOP
SP3232EBEA-L/TR	-40°C to +85°C	16 Pin SSOP
SP3232EBEN-L	-40°C to +85°C	16 Pin NSOIC
SP3232EBEN-L/TR	-40°C to +85°C	16 Pin NSOIC
SP3232EBET-L	-40°C to +85°C	16 Pin WSOIC
SP3232EBET-L/TR	-40°C to +85°C	16 Pin WSOIC
SP3232EBEY-L	-40°C to +85°C	16 Pin TSSOP
SP3232EBEY-L/TR	-40°C to +85°C	16 Pin TSSOP
SP3232EBER-L	-40°C to +85°C	16 Pin QFN
SP3232EBER-L/TR	-40°C to +85°C	16 Pin QFN

Note: "/TR" is for tape and Reel option. "-L" is for lead free packaging

REVISION HISTORY

DATE	REVISION	DESCRIPTION
11/02/05	--	Legacy Sipex Datasheet
09/09/09	1.0.0	Convert to Exar Format, Update ordering information and change revision to 1.0.0.
06/07/11	1.0.1	Remove obsolete devices per PDN 110510-01 and change ESD rating to IEC-61000-4-2.
03/14/13	1.0.2	Correct type error to RX input voltage range and TX transition region slew rate condition.
8/14/14	1.0.3	Add Max Junction temperature and package thermal information.
5/28/15	1.0.4	Update Absolute Max Rating for RxIN input voltage to +/-25V, update logo.
10/27/15	1.0.5	Add SP3232EBER (QFN_16) preliminary package option.
2/23/16	1.0.6	Remove preminary status of QFN_16 package option.

Datasheet February 2016

Send your serial transceiver technical inquiry with technical details to: serialtechsupport@exar.com