Ordering Information

Part Number	Marking	Shipping	Ambient Temperature Range	Package
SM802xxxUMG	802xxx	Tray	–40°C to +85°C	See Package Options
SM802xxxUMGTR	802xxx	Tape and Reel	–40°C to +85°C	See Package Options

Package Options

Package Option[1]	QFN Package	# of Outputs	Crystal	Reference Input	XTAL_SEL	FSEL	OE1 OE2	PLL Bypass
#1	44-pin, 7mm × 7mm	8 diff.	Yes	Yes	Yes	Yes	Yes	Yes
#2	32-pin, 5mm × 5mm	4 diff.	Yes	Yes	Yes	Yes	Yes	Yes
#3	24-pin, 4mm × 4mm	4 diff.	Yes	Yes	Yes	No	No	Yes
#4	24-pin, 4mm × 4mm	2 diff.	Yes	Yes	Yes	Yes	Yes	Yes
#5	16-pin, 3mm × 3.5mm	2 diff.	No	Yes	No	Yes	No	No
#6	16-pin, 3mm × 3.5mm	2 diff.	Yes	No	No	No	No	No

Note:

1. Use the web tool at http://clockworks.micrel.com/micrel/ to determine the desired configuration.

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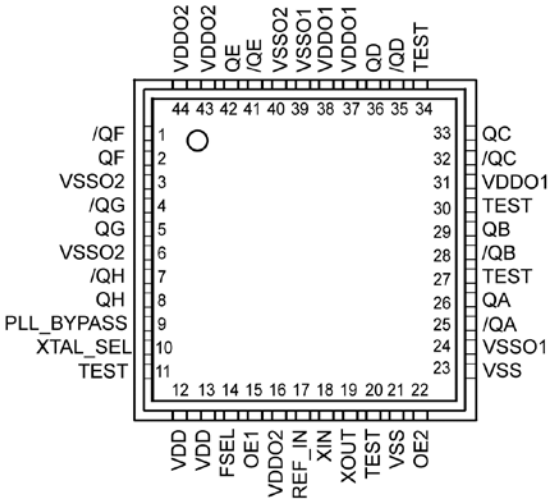
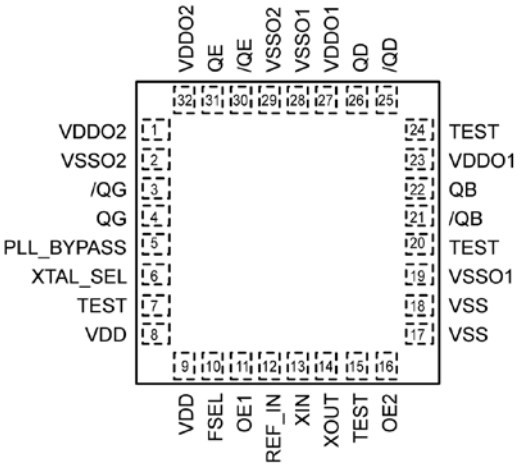
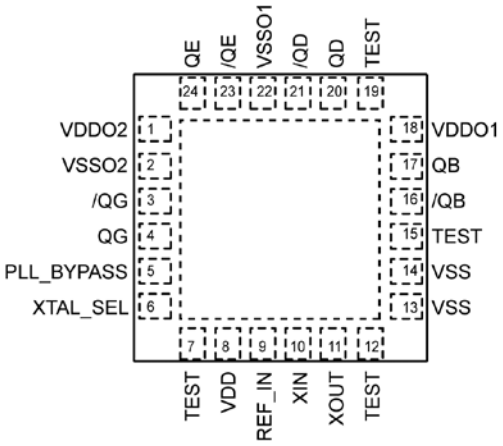
Pin Configurations



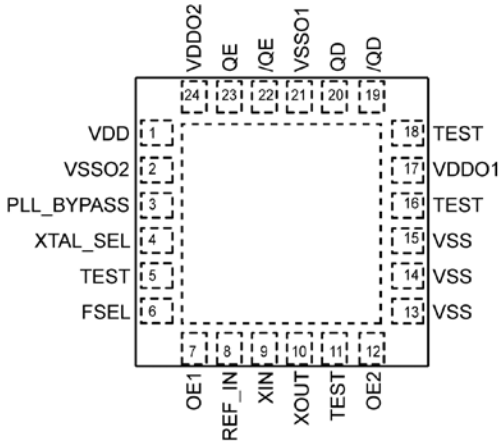
Option #1
44-Pin 7mm x 7mm QFN (QFN-44L)



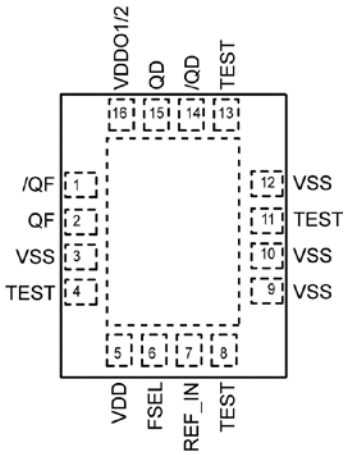
Option #2
32-Pin 5mm x 5mm QFN



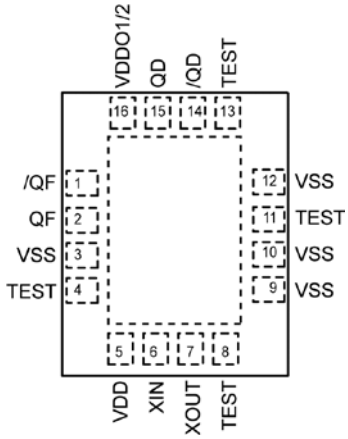
Option #3
24-Pin 4mm x 4mm QFN



Option #4
24-Pin 4mm x 4mm QFN



Option #5
16-Pin 3mm x 3.5mm QFN



Option #6
16-Pin 3mm x 3.5mm QFN

hbwhelp@micrel.com or (408) 955-1690

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Pin Description

Pin Numbers by Package Option						Pin Name	Pin Type	Pin Level	Pin Function
#1 44-Pin	#2 32-Pin	#3 24-Pin	#4 24-Pin	#5 16-Pin	#6 16-Pin				
18 19	13 14	10 11	9 10		6 7	XIN XOUT	I, O (SE)		Crystal connections
17	12	9	8	7		REF_IN	I, (SE)	LVCMOS	Reference Clock input
14	10		6	6		FSEL	I, (SE)	LVCMOS	Frequency Select, divides output frequencies by 2. 0 = FREQ, 1 = FREQ/2, 45kΩ pull-up
10	6	6	4	-	-	XTAL SEL	I, (SE)	LVCMOS	XTAL Select, selects between XTAL and REF_IN 0 = REF_IN, 1 = XTAL, 45kΩ pull-up
9	5	5	3	-	-	PLL BYPASS	I, (SE)	LVCMOS	Bypasses the PLL and switches the XTAL or REF_IN frequency to all outputs 0 = PLL mode, 1 = Bypass mode, 45kΩ pull-down
25 26	-	-	-	-	-	/QA QA	O	Various	Clock Outputs from Bank 1 Each output can be programmed to its own logic type: LVPECL, LVDS, HCSL, or LVCMOS[2]
28 29	21 22	16 17	-	-	-	/QB QB	O	Various	
32 33	-	-	-	-	-	/QC QC	O	Various	
35 36	25 26	20 21	19 20	14 15	14 15	/QD QD	O	Various	
41 42	30 31	23 24	22 23	-	-	/QE QE	O	Various	Clock Outputs from Bank 2 Each output can be programmed to its own logic type: LVPECL, LVDS, HCSL, or LVCMOS[2]
1 2	-	-	-	1 2	1 2	/QF QF	O	Various	
4 5	3 4	3 4	-	-	-	/QG QG	O	Various	
7 8	-	-	-	-	-	/QH QH	O	Various	
31 37 38	23 27	18	17	16	16	VDDO1	PWR		Power Supply for the outputs on Bank 1.
16 43 44	1 32	1	24	16	16	VDDO2	PWR		Power Supply for the outputs on Bank 2.

Note:

2. In the case of LVCMOS, an output pair can provide two single-ended LVCMOS outputs.

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Pin Numbers by Package Option						Pin Name	Pin Type	Pin Level	Pin Function
#1 44-Pin	#2 32-Pin	#3 24-Pin	#4 24-Pin	#5 16-Pin	#6 16-Pin				
24 39	19 28	22	21	-	-	VSSO1	PWR		Power Supply Ground for the outputs on Bank 1.
3 6 40	2 29	2	2	-	-	VSSO2	PWR		Power Supply Ground for the outputs on Bank 2.
11 20 27 30 34	7 15 20 24	7 12 15 19	5 11 16 18	4 8 11 13	4 8 11 13	TEST			Used for production test. Do not connect anything to these pins.
12 13	8 9	8	1	5	5	VDD	PWR		Core Power Supply.
21 23	17 18	13 14	13 14 15	3 9 10 12	3 9 10 12	VSS	PWR		Core Power Supply Ground.
-	-	-	-	-	-	EXPOSED PAD	-		The exposed pad must be connected to the VSS ground plane.
15	11	-	7	-	-	OE1	I, (SE)	LVCMOS	Output Enable 1, OUT1–8 disables to tri-state, 0 = Disabled, 1 = Enabled, 45kΩ pull-up
22	16	-	12	-	-	OE2	I, (SE)	LVCMOS	Output Enable 2, OUT9–16 disables to tri-state, 0 = Disabled, 1 = Enabled, 45kΩ pull-up

Truth Table

Control Pin	Internal Resistor[3]	0 Level (Low)	1 Level (High)
OE1	Pull-Up	Outputs QA~QD disabled to Hi Z (Tri-State)	Outputs QA~QD enabled
OE2	Pull-Up	Outputs QE~QH disabled to Hi Z (Tri-State)	Outputs QE~QH enabled
XTAL_SEL	Pull-Up	External reference clock input is selected	Crystal is selected
FSEL[4]	Pull-Up	Output = Target Frequency X2 or /2	Output = Target Frequency
PLL_BYPASS	Pull-Down	PLL frequency is connected to outputs	PLL is bypassed, Crystal or Ref-in is connected to outputs

Notes:

3. The internal resistor sets the default logic level on the control pin when the pin is left open. Pull up will set default logic 1 and pull down will set default logic 0. When the pin is not available on a specific configuration, the level will be the default logic level.
4. The FSEL pin behavior can be programmed between two types:
   - At FSEL=0 (low), the output frequency changes to multiply by 2.
   - At FSEL=0 (low), the output frequency changes to divide by 2.

   The FSEL function affects all outputs the same way, all outputs change when the FSEL pin level changes.

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Absolute Maximum Ratings[5]

Supply Voltage (V_{DD}, $V_{DDO1/2}$) ..... +4.6V
Input Voltage (V_{IN}) ..... –0.5V to V_{DD} + 0.5V
Lead Temperature (soldering, 20s) ..... 260°C
Case Temperature ..... 115°C
Storage Temperature (Ts) ..... –65°C to +150°C

Operating Ratings[6]

Supply Voltage ($V_{DD,}$ $V_{DDO1/2}$) ..... +2.375V to +3.465V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance[7]
QFN (θ_{JA}), Still-Air
44-pin ..... 24°C/W
32-pin ..... 34°C/W
24-pin ..... 50°C/W
16-pin ..... 60°C/W

DC Electrical Characteristics[8]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%
V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%
T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{DD,}$ $V_{DDO1/2}$	3.3V Operating Voltage	V_{DDO1} = V_{DDO2}	3.135	3.3	3.465	V
	2.5V Operating Voltage	V_{DDO1} = V_{DDO2}	2.375	2.5	2.625	V
I_{DD}	Total supply current, V_{DD} + V_{DDO}	8 LVPECL, 312.5MHz (44-pin QFN) Outputs open		275	345	mA
		4 HCSL (PCIe), 100MHz (32-pin or 24-pin QFN) Outputs 50Ω to V_{SS}		150	185	mA
		2 LVCMOS, 125MHz (16-pin QFN) Outputs open		70	90	mA

LVCMOS Inputs (OE1, OE2, PLL_BYPASS, XTAL_SEL, FSEL) DC Electrical Characteristics[8]

V_{DD} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IN}	Input Low Voltage		–0.3		0.8	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	–150			µA

Notes:

5. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
6. The datasheet limits are not guaranteed if the device is operated beyond the operating ratings.
7. Package thermal resistance assumes the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
8. The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics tables after thermal equilibrium has been established.

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LVDS Output DC Electrical Characteristics[8]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%
V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%
T_A = –40°C to +85°C. R_L = 100Ω across Q1 and /Q1.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OD}	Differential Output Voltage	Figure 6	275	350	475	mV
ΔV_{OD}	V_{OD} Magnitude Change				40	mV
V_{OS}	Offset Voltage		1.15	1.25	1.50	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

HCSL Output DC Electrical Characteristics[8]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%
V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%
T_A = –40°C to +85°C. R_L = 50Ω to V_{SS}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage		660	700	850	mV
V_{OL}	Output Low Voltage		–150	0	27	mV
V_{SWING}	Output Voltage Swing		250	350	550	mV

LVPECL Output DC Electrical Characteristics[8]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%
V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%
T_A = –40°C to +85°C. R_L = 50Ω to V_{DDO} – 2V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage		V_{DDO} – 1.145	V_{DDO} – 0.97	V_{DDO} – 0.845	V
V_{OL}	Output Low Voltage		V_{DDO} – 1.945	V_{DDO} – 1.77	V_{DDO} – 1.645	V
V_{SWING}	Output Voltage Swing		0.6	0.8	1.0	V

LVCMOS Output DC Electrical Characteristics[8]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%
V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%
T_A = –40°C to +85°C. R_L = 50Ω to V_{DDO}/2

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	Figure 7	V_{DDO} – 0.7			V
V_{OL}	Output Low Voltage	Figure 7			0.6	V

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REF_IN DC Electrical Characteristics[8]

V_{DD} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		1.1		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.6	V
I_{IN}	Input Current	XTAL_SEL = V_{IL}, V_{IN} = 0V to V_{DD}	–5		5	µA
		XTAL_SEL = V_{IH}, V_{IN} = V_{DD}		20		µA

Crystal Characteristics

V_{DD} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	10pF load capacitance	Fundamental, parallel resonant			
Frequency		11		30	MHz
Equivalent Series Resistance (ESR)				40	Ω
Shunt Capacitance, C0			2	5	pF
Correlation Drive Level			10	100	µW

LVPECL AC Electrical Characteristics[8, 9, 11, 15]

V_{DDA} = V_{DD} = 3.3V ±5% or 2.5V ±5%, V_{DDO} = 2.5V or 3.3V ±5%, T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency		11		840	MHz
T_R/T_F	LVPECL Output Rise/Fall Time	20% – 80%	80	175	350	ps
ODC	Output Duty Cycle	< 350MHz	48	50	52	%
		≥ 350MHz	45	50	55	%
T_{SKEW}	Output-to-Output Skew	Note 10			45	ps
T_{LOCK}	PLL Lock Time				20	ms
$T_{jit}(\varnothing)$	RMS Phase Jitter @ 156.25MHz	Integration Range (12kHz to 20MHz)		245		fs
		Integration Range (1.875MHz to 20MHz)		115		fs

Notes:

9. See Figures 4 to 7 for load test circuit examples.
10. Defined as skew between outputs at the same supply voltage and with equal load conditions; Measured at the output differential crossing points.
11. All phase noise measurements were taken with an Agilent 5052B phase noise system.

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LVDS AC Electrical Characteristics[8, 9, 11, 12]

V_{DDA} = V_{DD} = 3.3V ±5% or 2.5V ±5%, V_{DDO} = 2.5V or 3.3V ±5%, T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency		11		840	MHz
T_R/T_F	LVDS Output Rise/Fall Time	20% – 80%	100	160	400	ps
ODC	Output Duty Cycle	< 350MHz	48	50	52	%
		≥ 350MHz	45	50	55	%
T_{SKEW}	Output-to-Output Skew	Note 10			45	ps
T_{LOCK}	PLL Lock Time				20	ms
$T_{jit}(\varnothing)$	RMS Phase Jitter @ 156.25MHz	Integration Range (1.875MHz to 20MHz)		99		fs

HCSL AC Electrical Characteristics[8, 9, 11, 13]

V_{DDA} = V_{DD} = 3.3V ±5% or 2.5V ±5%, V_{DDO} = 2.5V or 3.3V ±5%, T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency		11		840	MHz
T_R/T_F	Output Rise/Fall Time	20% – 80%	150	300	450	ps
ODC	Output Duty Cycle	< 350MHz	48	50	52	%
		≥ 350MHz	45	50	55	%
T_{SKEW}	Output-to-Output Skew	Note 10			50	ps
T_{LOCK}	PLL Lock Time				20	ms
$T_{jit}(\varnothing)$	RMS Phase Jitter @ 100MHz	Integration Range (12kHz to 20MHz)		254		fs
		Integration Range (1.875MHz to 20MHz)		115		fs

LVCMOS AC Electrical Characteristics[8, 9, 11, 14]

V_{DDA} = V_{DD} = 3.3V ±5% or 2.5V ±5%, V_{DDO} = 2.5V or 3.3V ±5%, T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency		11		250	MHz
F_{REF}	REF_IN Frequency		11		80	MHz
T_R/T_F	Output Rise/Fall Time	20% – 80%	100		500	ps
ODC	Output Duty Cycle		45	50	55	%
T_{SKEW}	Output-to-Output Skew	Note 10			60	ps
T_{LOCK}	PLL Lock Time				20	ms
$T_{jit}(\varnothing)$	RMS Phase Jitter @ 125MHz	Integration Range: 1.875MHz to 20MHz		114		fs

Notes:

12. Outputs terminated 100Ω between Q and /Q. All unused outputs must be terminated.
13. Output load is 50Ω to V_{SS}.
14. Output load is 50Ω to V_{DD} / 2.
15. Output load is 50Ω to V_{DD} - 2V.

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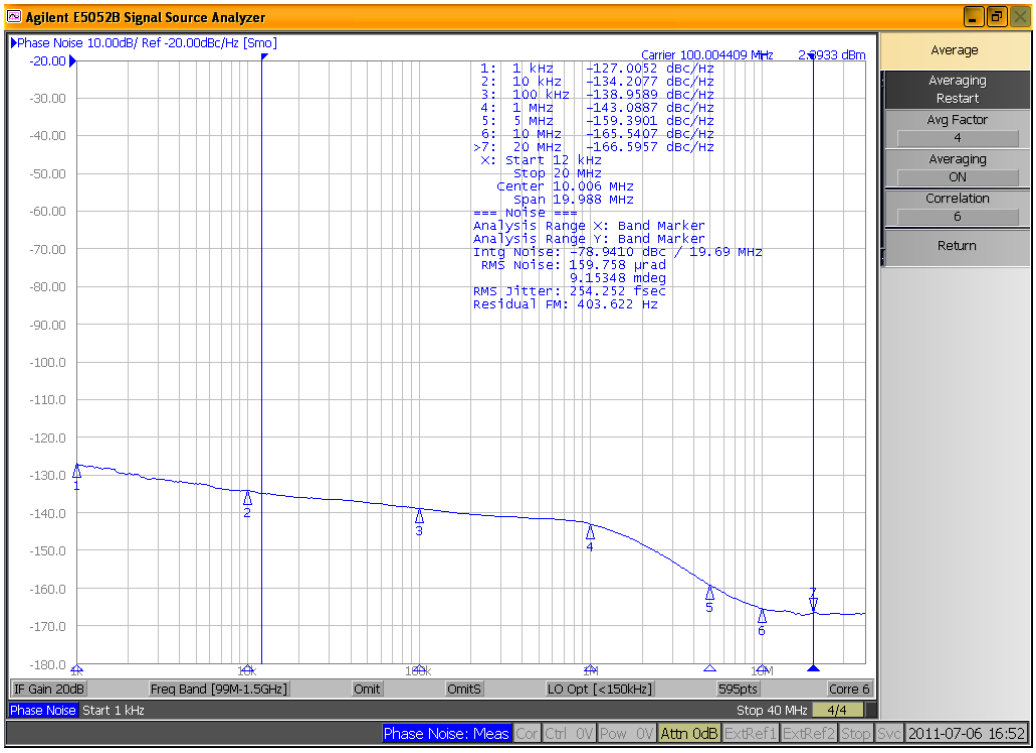
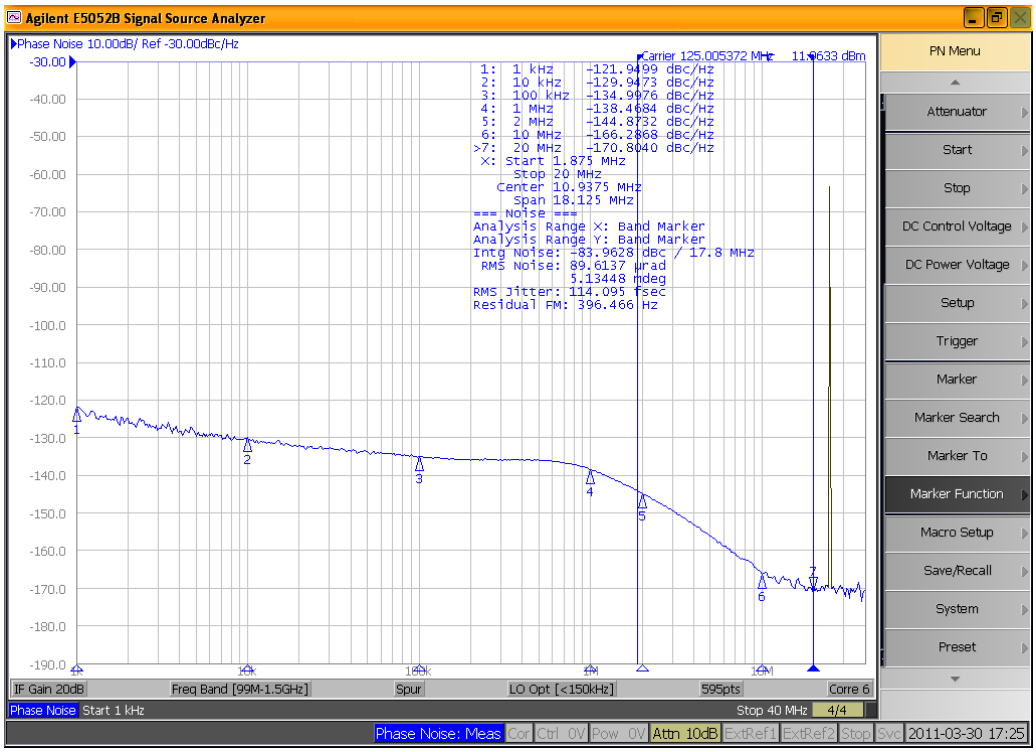
Phase Noise Plots



100MHz HCSL, 254fs rms for 12kHz to 20MHz integration range



125MHz LVCMOS, 114fs rms for 1.875MHz to 20MHz integration range

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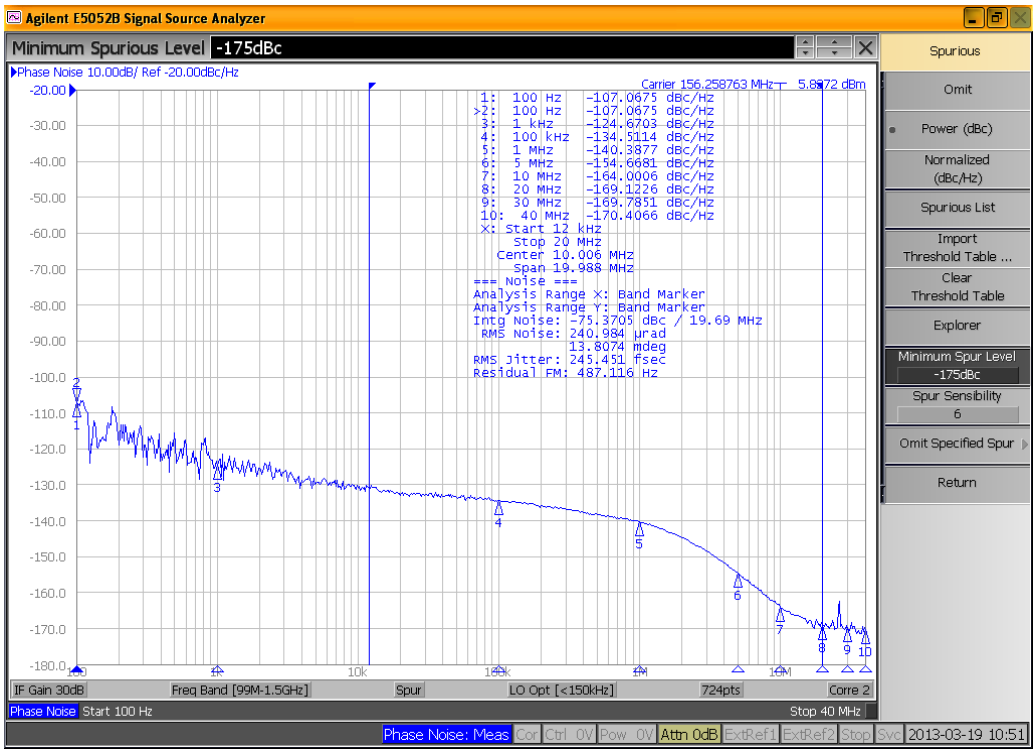
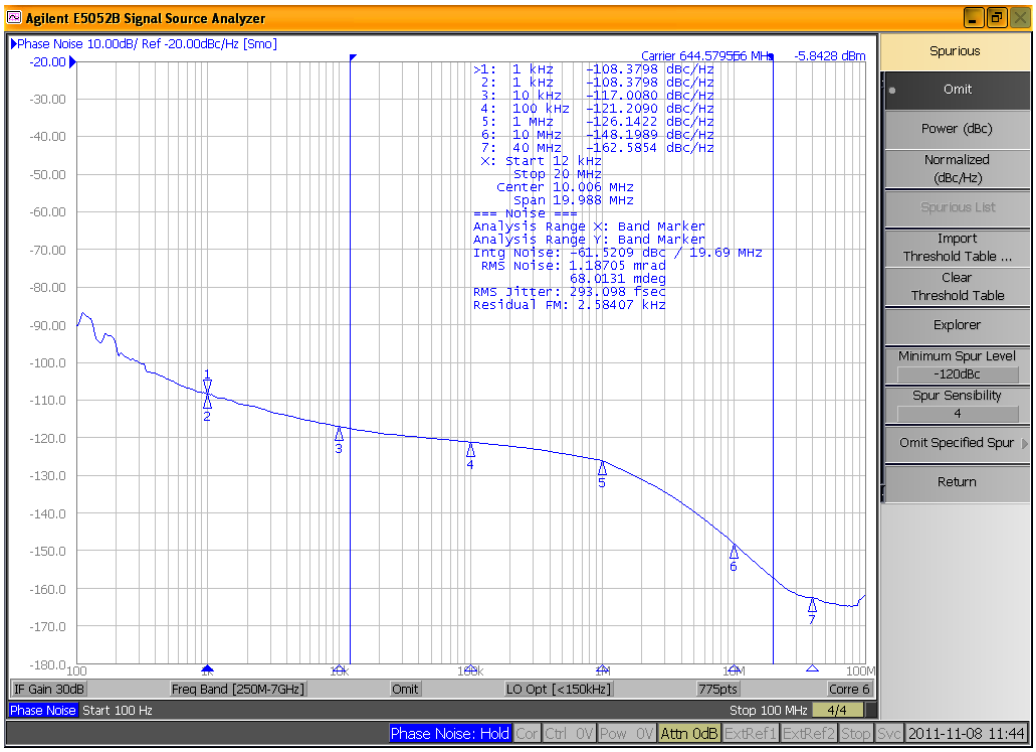


156.25MHz LVPECL, 245fs rms for 12kHz to 20MHz integration range



644.53125MHz LVDS, 293fs rms for 12kHz to 20MHz integration range

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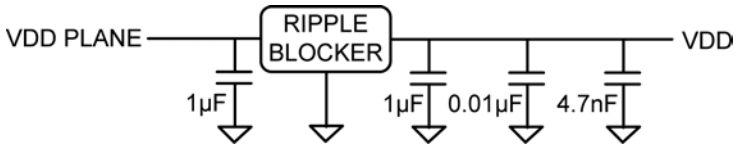
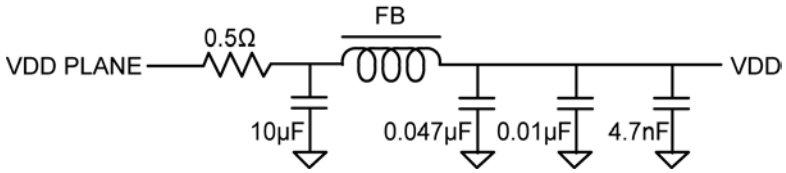
Power Supply Filtering Recommendations

Preferred filter, using Micrel MIC94300 or MIC94310 Ripple Blocker:



Alternative, traditional filter, using a ferrite bead:



Application Information

Input Reference

When operating with a crystal input reference, do not apply a switching signal to REF_IN.

Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal. Crystal load capacitance is built inside the die so no external capacitance is needed. See the *Selecting a Quartz Crystal for the Clockworks Flex I Family of Precision Synthesizers* application note for more details.

If you need help selecting a suitable crystal for your application, contact Micrel's HBW applications group at: hbwhelp@micrel.com.

Power Supply Decoupling

Place the smallest value decoupling capacitor (4.7nF above) between the VDD and VSS pins, as close as possible to those pins and at the same side of the PCB as the IC. The shorter the physical path from VDD to capacitor and back from capacitor to VSS, the more effective the decoupling. Use one 4.7nF capacitor for each VDD pin on the SM802XXX.

The impedance value of the Ferrite Bead (FB) needs to be between 240Ω and 600Ω with a saturation current ≥150mA.

The VDDO1 and VDDO2 pins connect directly to the VDD Plane. All VDD pins on the SM802XXX connect to VDD after the power supply filter.

Output Traces

Design the traces for the output signals according to the output logic requirements. If LVCMOS is unterminated, add a 30Ω resistor in series with the output, as close as possible to the output pin and start a 50Ω trace on the other side of the resistor.

For differential traces you can either use a differential design or two separate 50Ω traces. For EMI reasons it is better to use a differential design.

LVDS can be AC-coupled or DC-coupled to its termination.

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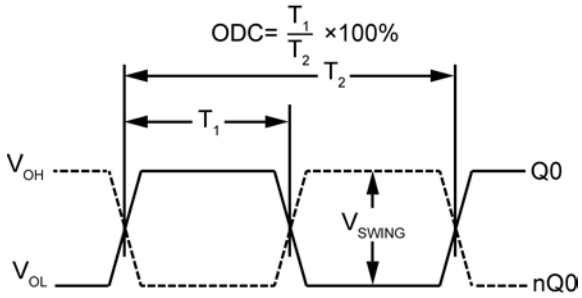

Figure 1. Duty Cycle Timing

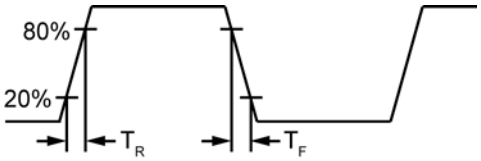

Figure 2. All Outputs Rise/Fall Time

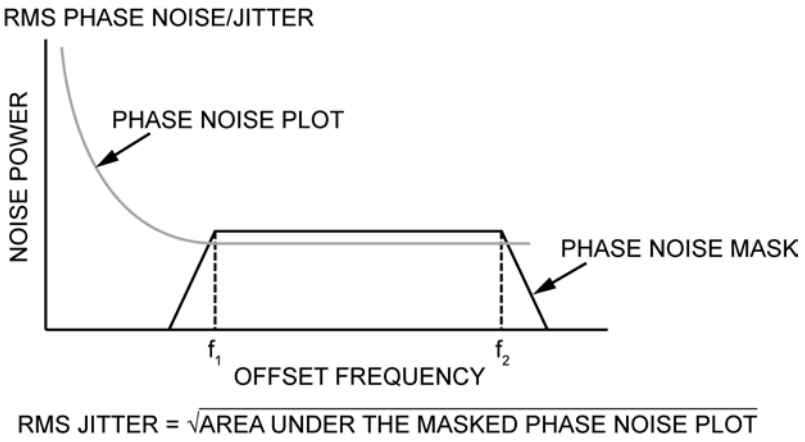

Figure 3. RMS Phase/Noise/Jitter

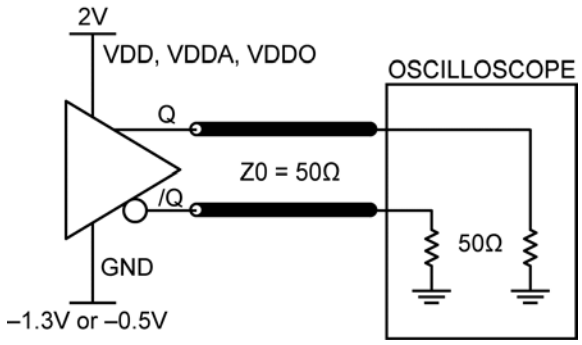

Figure 4. LVPECL Output Load and Test Circuit

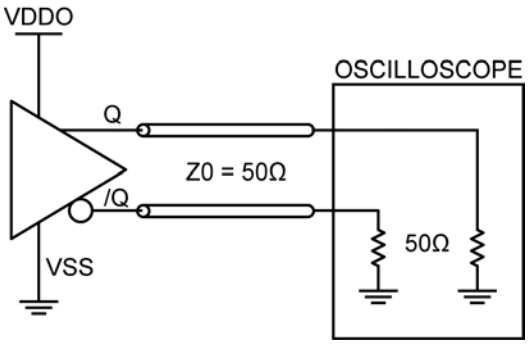

Figure 5. HCSL Output Load and Test Circuit

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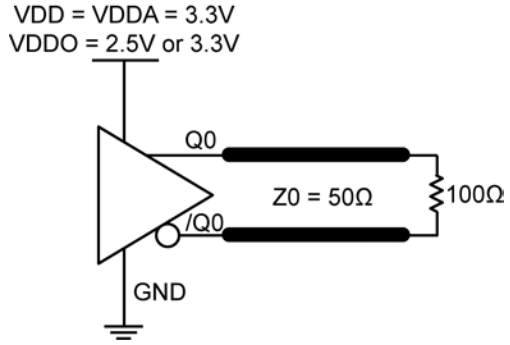

Figure 6. LVDS Output Load and Test Circuit

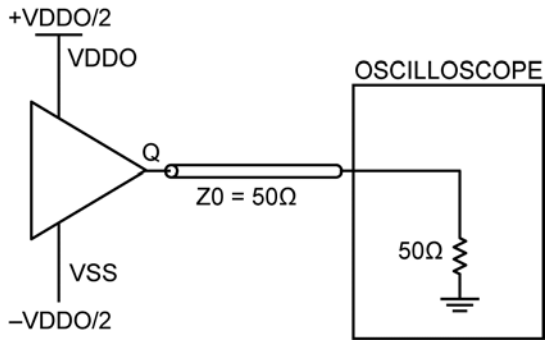

Figure 7. LVCMOS Output Load and Test Circuit

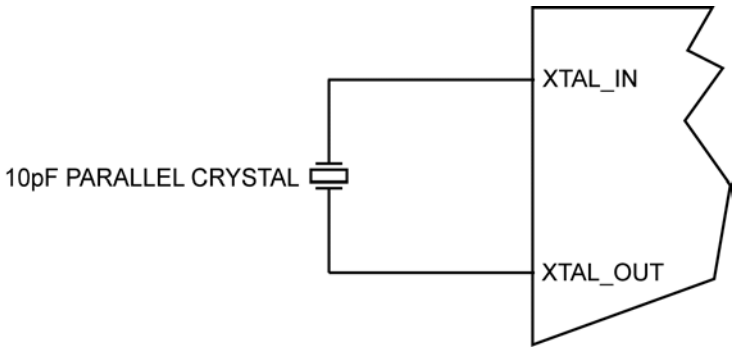

Figure 8. Crystal Input Interface

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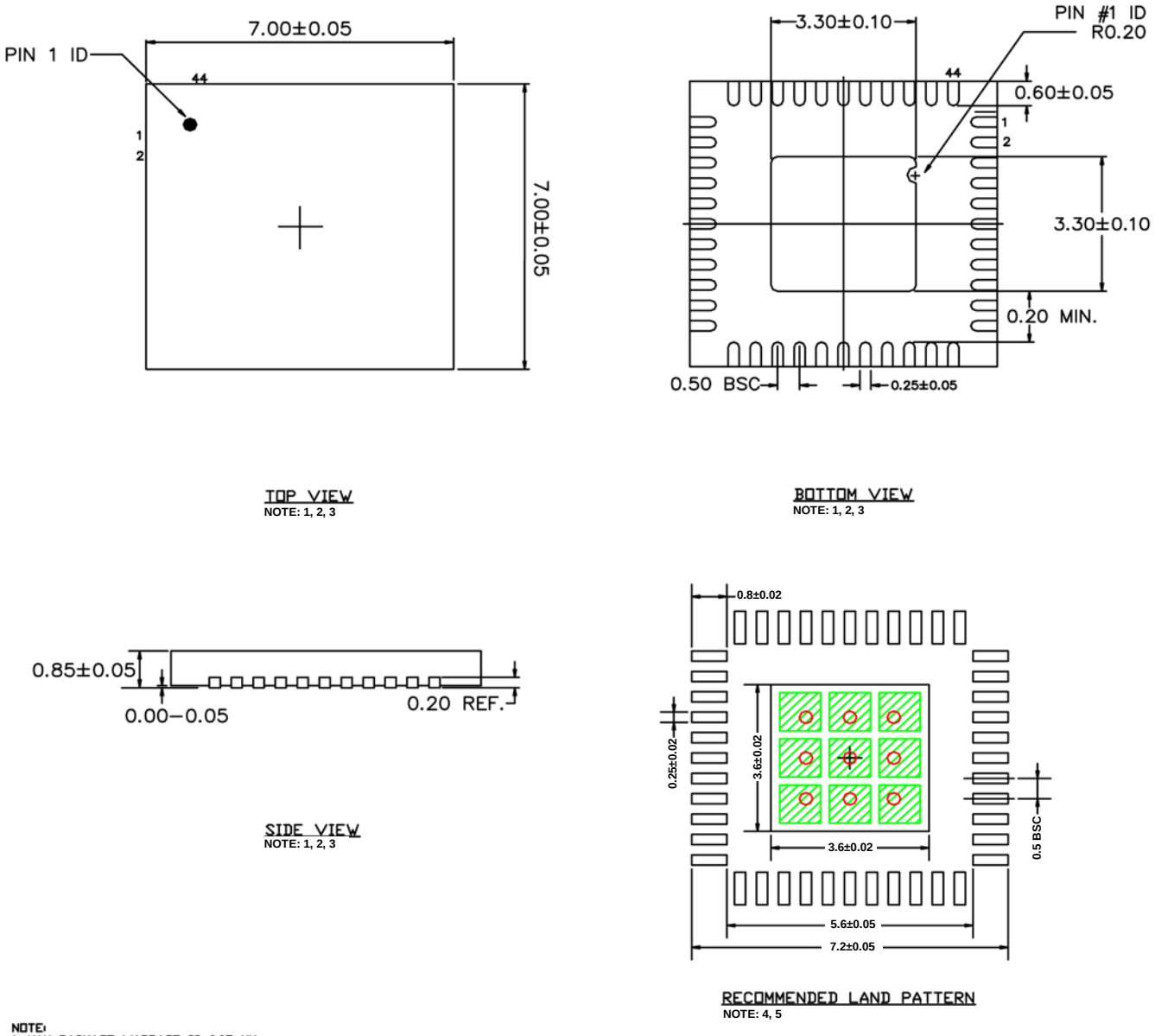
Package Information and Recommended Land Pattern for 44-Pin QFN[15]



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.3MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE. 1.0MM PITCH
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 0.93x0.93MM, SPACING IS 0.2MM

44-Pin QFN

Note:

16. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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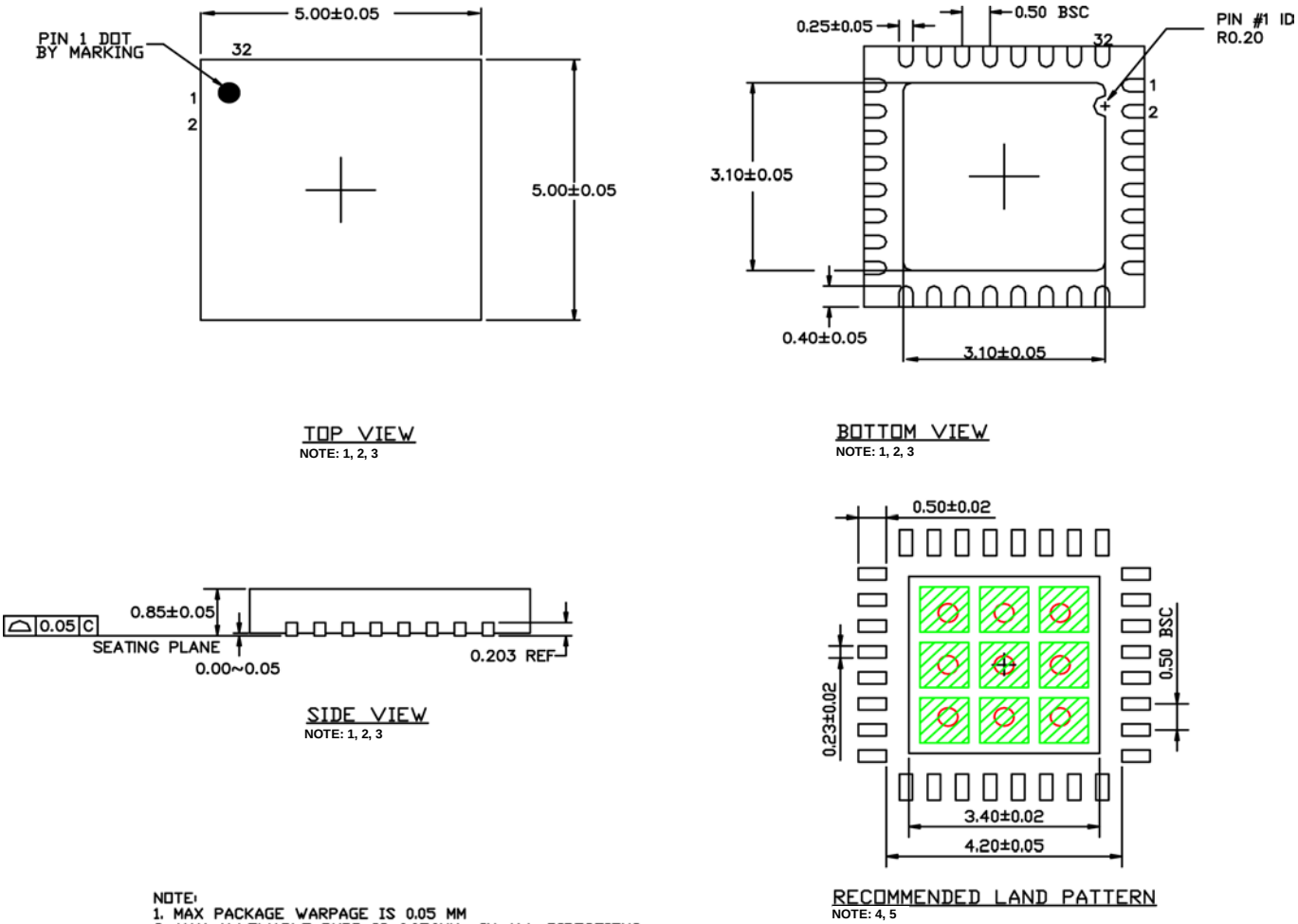
Package Information and Recommended Land Pattern for 32-Pin QFN[15]



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.3M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.87x0.87 MM IN SIZE, 1.07 MM PITCH.

32-Pin QFN

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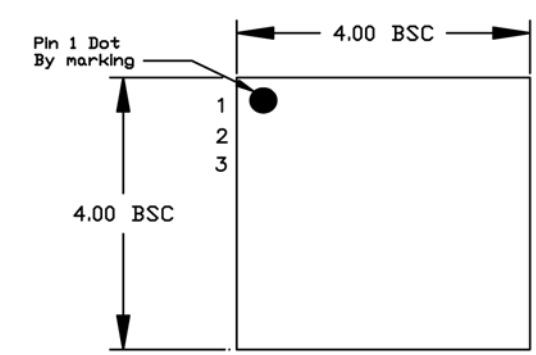
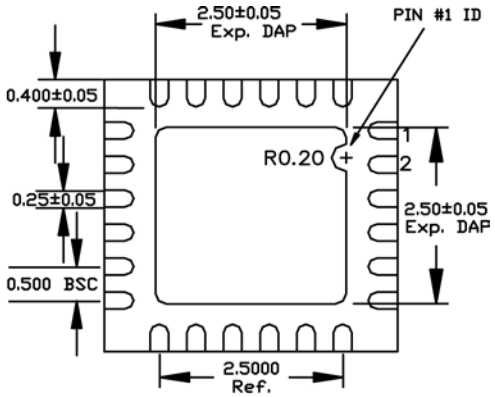
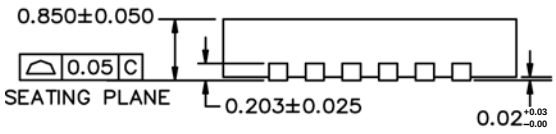
Package Information and Recommended Land Pattern for 24-Pin QFN[15]



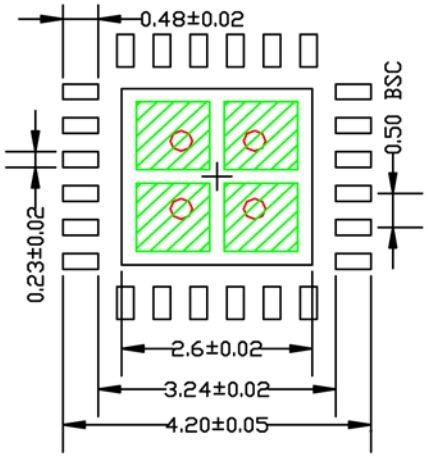
TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



SIDE VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN
NOTE: 4, 5

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.3M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) Indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 1.00x1.00 MM IN SIZE, 1.20 MM PITCH.

24-Pin QFN

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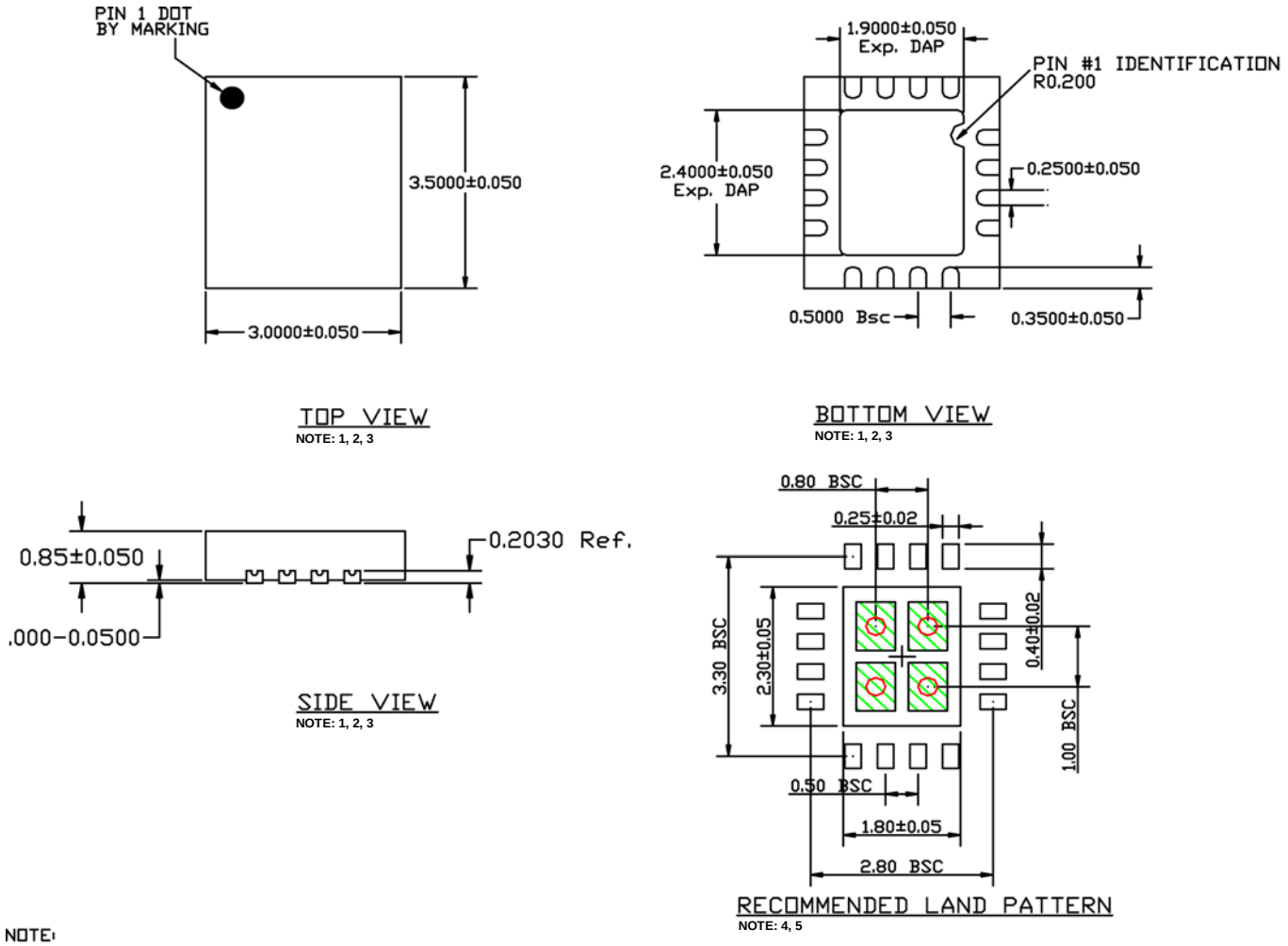
Package Information and Recommended Land Pattern for 16-Pin QFN[15]



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN REPRESENT THERMAL VIA. RECOMMENDED DIAMETER IS 0.30 – 0.35 MM AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.80x0.60 MM, 0.20 MM SPACING.

16-Pin QFN

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