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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		3.0	—	3.6	V
Interface Supply Voltage	V_{IO}		2.7	—	3.6	V
Power Supply Powerup Rise Time	V_{DDRISE}		10	—	—	µs
Interface Power Supply Powerup Rise Time	V_{IORISE}		10	—	—	µs
Ambient Temperature	T_A		–40	25	85	°C

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.5 to 5.8	V
Interface Supply Voltage	V_{IO}	–0.5 to 3.9	V
Input Current[3]	I_{IN}	10	mA
Input Voltage[3]	V_{IN}	–0.3 to (V_{IO} + 0.3)	V
Operating Temperature	T_{OP}	–45 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		0.4	V_{pK}

Notes:
1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4740/41/42/43/44/45-C10 devices are high-performance RF integrated circuits with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of these devices should only be done at ESD-protected workstations.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, GPO1, GPO2, and GPO3.
4. At RF input pins, FMI and AMI.

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Table 3. DC Characteristics

(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FM Mode						
Supply Current	I_{FM}		—	26	28.6	mA
WB Mode (Si4742/43 only)						
Supply Current	I_{FM}		—	20	23	mA
AM Mode						
Supply Current	I_{AM}		—	19	23	mA
Supplies and Interface						
Interface Supply Current	I_{IO}		—	300	400	µA
Powerdown Current[1,2]	I_{PD}		—	6	12	µA
Interface Powerdown Current[1]	I_{IO}	SCLK, DFS, DCLK, RCLK inactive	—	6	12	µA
High Level Input Voltage[3]	V_{IH}		0.7 x V_{IO}	—	—	V
Low Level Input Voltage[3]	V_{IL}		—	—	0.3 x V_{IO}	V
High Level Input Current[3]	I_{IH}	V_{IN} = V_{IO} = 3.6 V	–10	—	10	µA
Low Level Input Current[3]	I_{IL}	V_{IN} = 0 V, V_{IO} = 3.6 V	–10	—	10	µA
High Level Output Voltage[4]	V_{OH}	I_{OUT} = 500 µA	0.8 x V_{IO}	—	—	V
Low Level Output Voltage[4]	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x V_{IO}	V

Notes:
1. Specifications are guaranteed by characterization.
2. Refer to Section "4.19. Control Interface" on page 35.
3. For input pins SCLK, SEN, SDIO, RST, and RCLK.
4. For output pins SDIO, DFS, GPO1, GPO2, and GPO3.

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Table 4. Reset Timing Characteristics[1,2,3]
(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{RST}$ Pulse Width and GPO1, GPO2/$\overline{INT}$ Setup to $\overline{RST}\uparrow$[4]	t_{SRST}	100	—	—	µs
GPO1, GPO2/$\overline{INT}$ Hold from $\overline{RST}\uparrow$	t_{HRST}	30	—	—	ns

Important Notes:

1. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
2. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
3. When selecting 3-wire or SPI modes, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.
4. If GPO1 and GPO2 are actively driven by the user, then minimum t_{SRST} is only 30 ns. If GPO1 or GPO2 is hi-Z, then minimum t_{SRST} is 100 µs, to provide time for on-chip 1 MΩ devices (active while $\overline{RST}$ is low) to pull GPO1 high and GPO2 low.

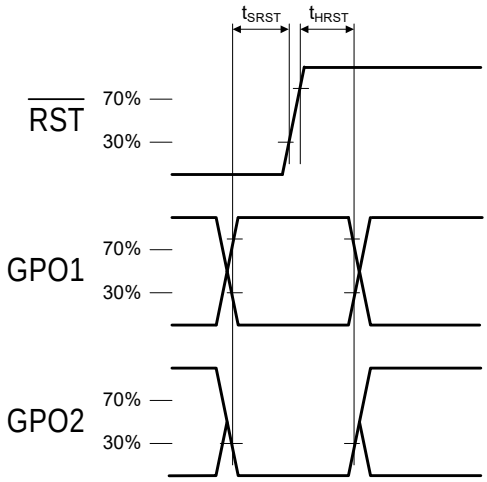

Figure 1. Reset Timing Parameters for Busmode Select Method

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Table 5. 2-Wire Control Interface Characteristics[1,2,3]
(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{SCL}		0	—	400	kHz
SCLK Low Time	t_{LOW}		1.3	—	—	µs
SCLK High Time	t_{HIGH}		0.6	—	—	µs
SCLK Input to SDIO ↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCLK Input to SDIO ↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDIO Input to SCLK ↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDIO Input to SCLK ↓ Hold[4,5]	$t_{HD:DAT}$		0	—	900	ns
SCLK input to SDIO ↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDIO Output Fall Time	$t_{f:OUT}$		$20 + 0.1\frac{C_b}{1pF}$	—	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		$20 + 0.1\frac{C_b}{1pF}$	—	300	ns
SCLK, SDIO Capacitive Loading	C_b		—	—	50	pF
Input Filter Pulse Suppression	t_{SP}		—	—	50	ns

Notes:
1. When V_{IO} = 0 V, SCLK and SDIO are low impedance.
2. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
3. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
4. The Si474x delays SDIO by a minimum of 300 ns from the V_{IH} threshold of SCLK to comply with the minimum $t_{HD:DAT}$ specification.
5. The maximum $t_{HD:DAT}$ has only to be met when f_{SCL} = 400 kHz. At frequencies below 400 kHz, $t_{HD:DAT}$ may be violated as long as all other timing parameters are met.

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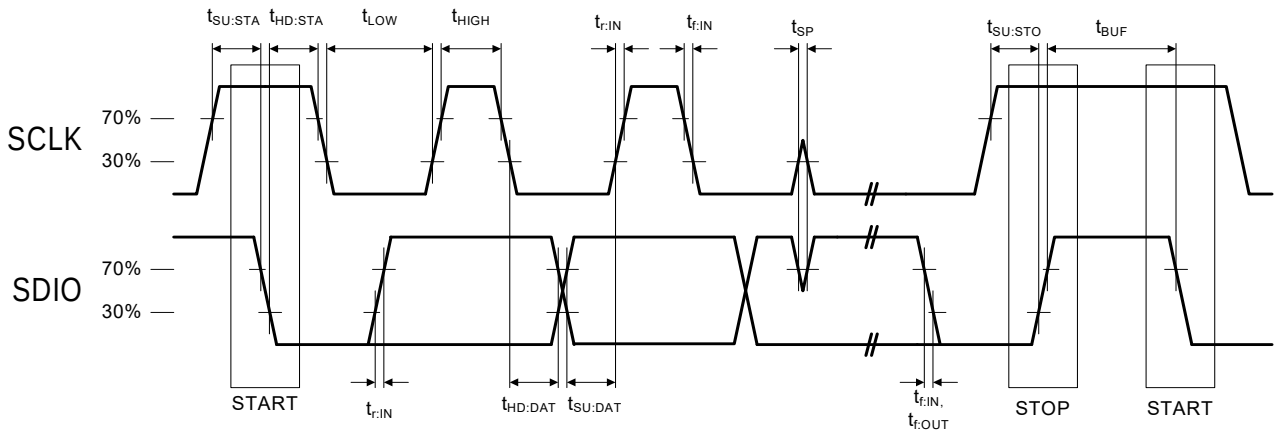

Figure 2. 2-Wire Control Interface Read and Write Timing Parameters

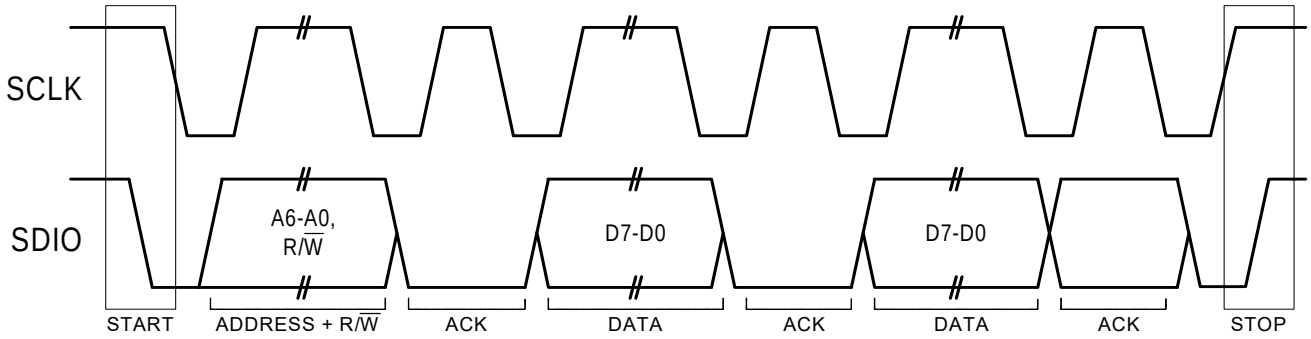

Figure 3. 2-Wire Control Interface Read and Write Timing Diagram

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Table 6. 3-Wire Control Interface Characteristics
(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		20	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		10	—	—	ns
SCLK↑ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↑ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall Time	t_R, t_F		—	—	10	ns

Note: When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.

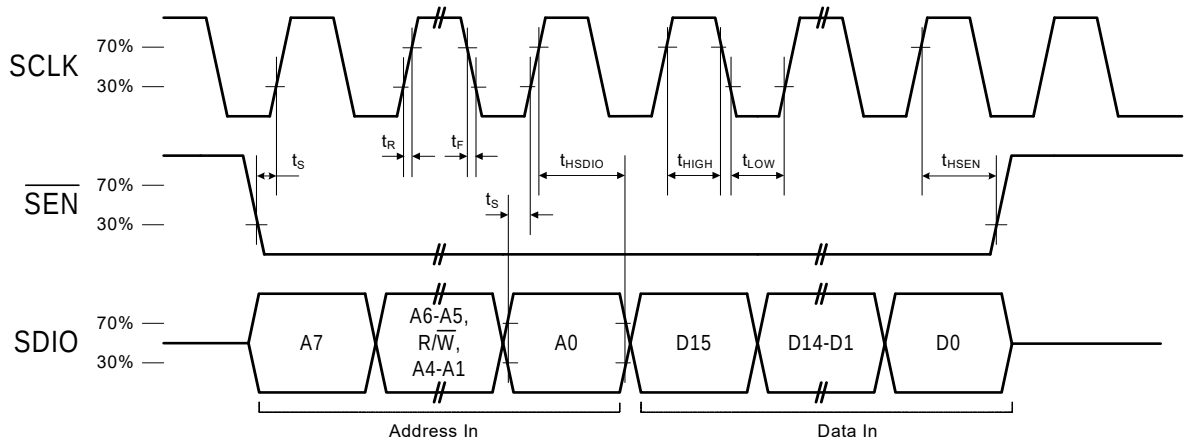

Figure 4. 3-Wire Control Interface Write Timing Parameters

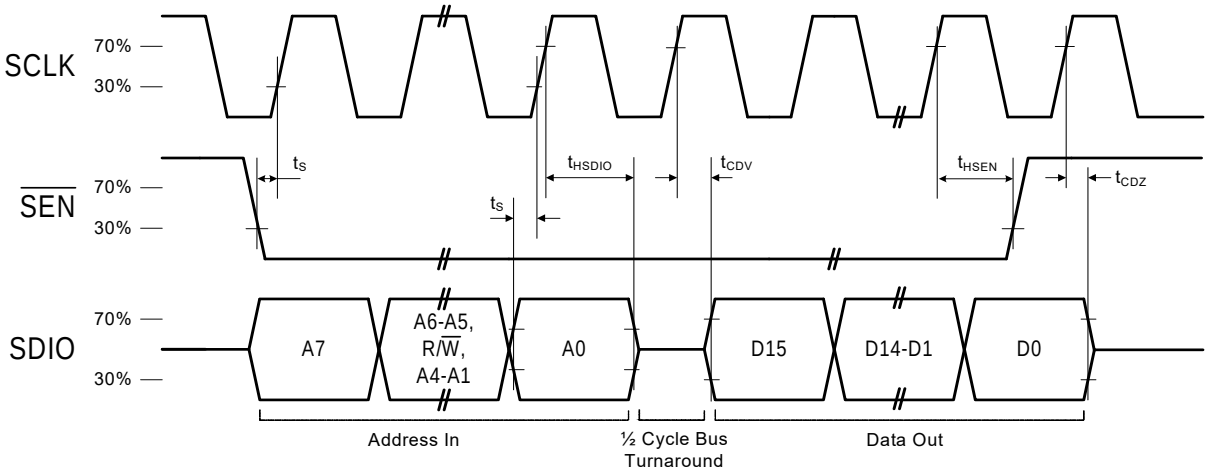

Figure 5. 3-Wire Control Interface Read Timing Parameters

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Table 7. SPI Control Interface Characteristics
(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		15	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		5	—	—	ns
SCLK↓ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↓ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall Time	t_R, t_F		—	—	10	ns

Note: When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.

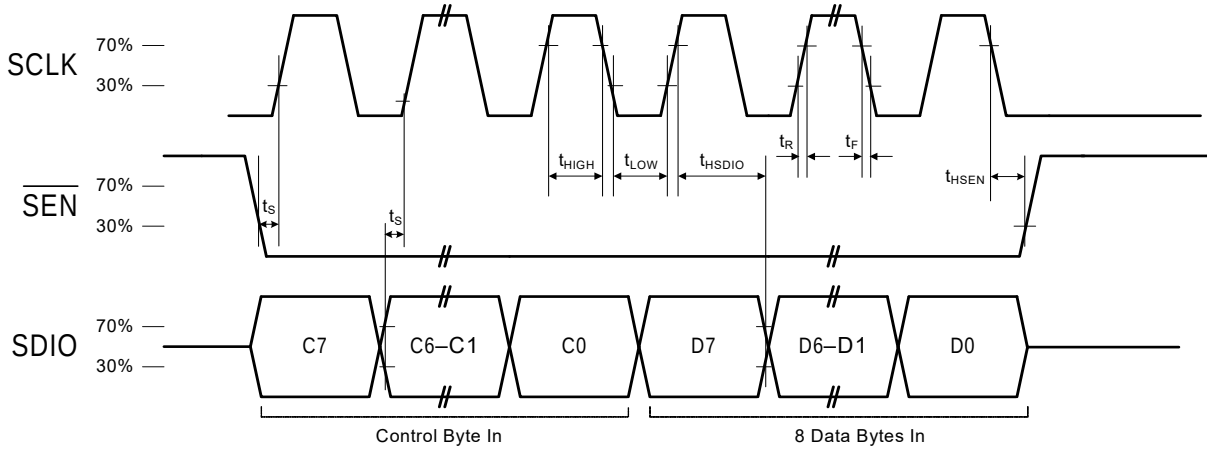

Figure 6. SPI Control Interface Write Timing Parameters

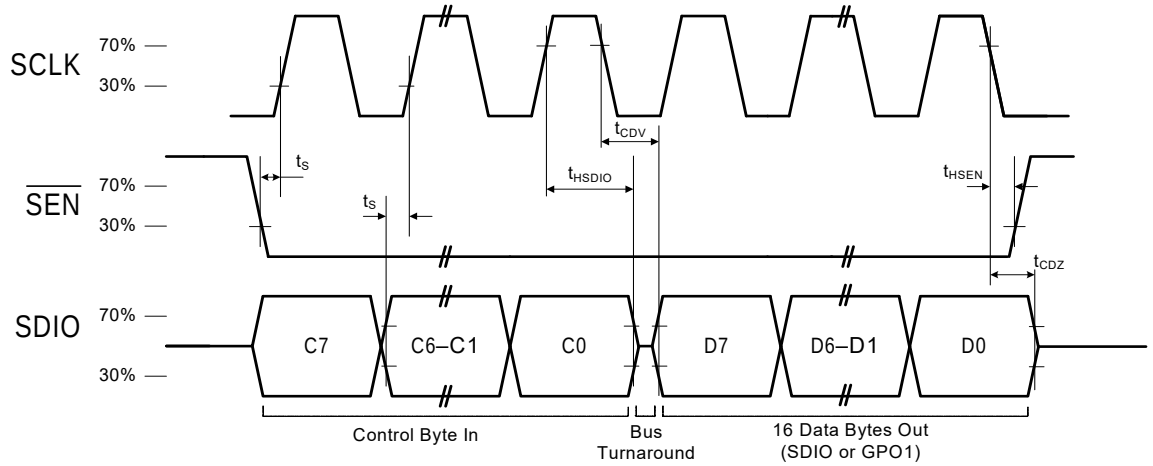

Figure 7. SPI Control Interface Read Timing Parameters

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Table 8. Digital Audio Interface Characteristics
(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK Cycle Time	t_{DCT}		26	—	1000	ns
DCLK Pulse Width High	t_{DCH}		10	—	—	ns
DCLK Pulse Width Low	t_{DCL}		10	—	—	ns
DFS Set-up Time to DCLK Rising Edge	$t_{SU:DFS}$		5	—	—	ns
DFS Hold Time from DCLK Rising Edge	$t_{HD:DFS}$		5	—	—	ns
DOUT Propagation Delay from DCLK Falling Edge	$t_{PD:DOUT}$		0	—	12	ns

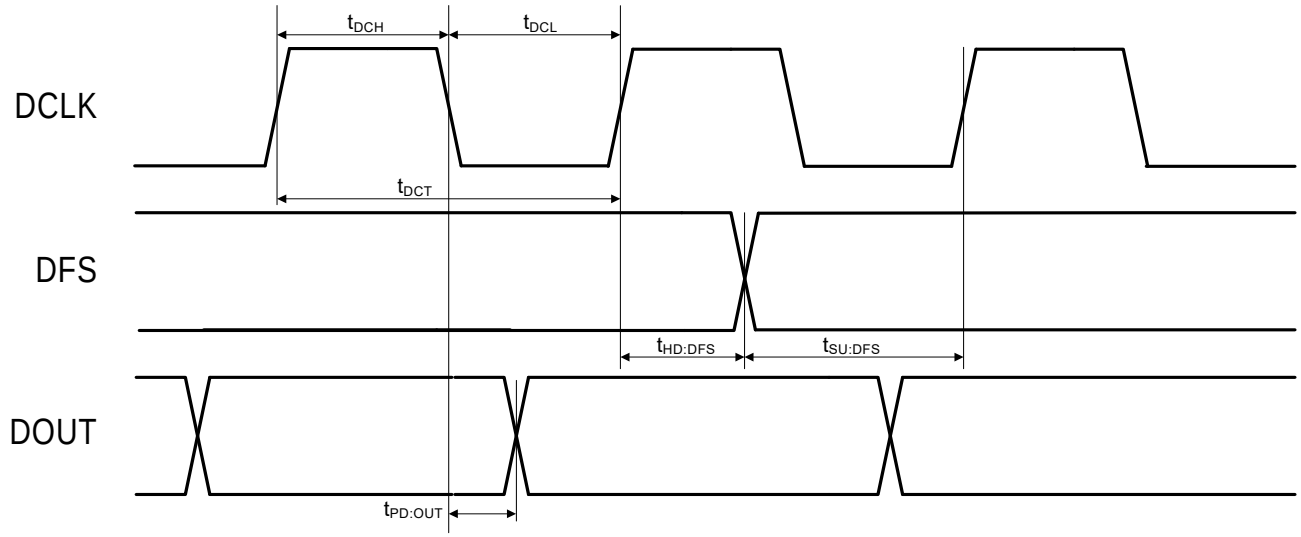

Figure 8. Digital Audio Interface Timing Parameters, I^2S Mode

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Table 9. FM Receiver Characteristics[1,2]

(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = 25 °C)

Parameter	Test Condition	Min	Typ	Max	Unit
FM Receiver					
Specifications Referred to Si4740/41/42/43/44/45-C10 Application Circuit Input					
Input Frequency		64	—	108	MHz
FM Frequency Steps		10	—	200	kHz
Sensitivity[3,4,5,6,7]	(S+N)/N = 26 dB	—	2	3	µV EMF
RDS Sensitivity[8]	Δf = 2 kHz, RDS BLER < 5%	—	6	9	µV EMF
RDS Synchronization Persistence[8]	Δf = 2 kHz RDSSYNC = 1 ≥ 10 sec	—	3.8/60	—	µV EMF/ RDS BLER%
RDS Synchronization Stability[8]	Δf = 2 kHz RDSSYNC = 1 ≥ 10 sec	—	5.9/10	—	µV EMF/ RDS BLER%
RDS Synchronization Time[8]	Δf = 2 kHz RF input = 60 dBµV EMF	—	90	—	ms
RDS PI Lock Time[8]	Δf = 2 kHz RF input = 60 dBµV EMF	—	105	—	ms
LNA Input Resistance[6,8,9]		3	4	—	kΩ
LNA Input Capacitance[6,8,9]		4	5	6	pF
Input IP3[3,4,7]	400 and 800 kHz blockers	100	105	—	dBµV EMF
AM Suppression[3,4,6,8,9]	m = 0.3	40	55	—	dB
Image Rejection[8]	Δf = 22.5 kHz	37	55	—	dB
Adjacent Channel Selectivity	±200 kHz	38	50	—	dB
Alternate Channel Selectivity	±400 kHz	60	70	—	dB
Strong Signal Distortion[3,4,5,6,8]	RF Level 120 dBµV EMF	53	58	—	dB SINAD
Audio Output Voltage[3,4,6,9]		72	80	90	mVRMS
Audio Output L/R Imbalance[3,6,9,10]		–1	—	1	dB

Notes:

1. Additional testing information is available in application note, “AN388:Si470X/1X/2X/3X/4X Evaluation Board Test Procedure.” Volume = maximum for all tests. Tested at F_{RF} = 98 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN400: Si474x AM/FM Receiver Layout Guide.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz.
6. f_{RF} = 76 to 108 MHz.
7. AGC is disabled.
8. Guaranteed by characterization.
9. Measured at V_{EMF} = 60 dBµV_{EMF}.
10. Δf = 75 kHz.
11. L = 1, R = 0.
12. At LOUT and ROUT pins.

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Table 9. FM Receiver Characteristics[1,2] (Continued)

(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = 25 °C)

Parameter	Test Condition	Min	Typ	Max	Unit
Audio Frequency Response Low[8]	–3 dB	—	—	30	Hz
Audio Frequency Response High[8]	–3 dB	15	—	—	kHz
Audio Stereo Separation[3,6,9,10,11]		35	45	—	dB
Audio SNR[3,4,5,6,9]		56	63	—	dB
Audio THD[3,4,5,6,9]		—	0.1	0.5	%
De-emphasis Time Constant[8]	FM_DEEMPHASIS = 2	70	75	80	µs
	FM_DEEMPHASIS = 1	45	50	54	µs
Audio Common Mode Voltage[12]		0.7	0.8	0.9	V
Audio Common Mode Voltage[8]	High-Z mode	—	0.5 x V_{IO}	—	V
Audio Output Load Resistance[8,10,12]	Single-ended	10	—	—	kΩ
Audio Output Load Capacitance[8,10,12]	Single-ended	—	—	50	pF
Seek/Tune Time[8,12]	RCLK tolerance = 100 ppm	—	40	60	ms/ channel
Powerup Time[8]	From powerdown	—	—	110	ms
FM RSSI Offset	Input levels of 8 and 60 dBµV EMF	–3	—	3	dB

Notes:

1. Additional testing information is available in application note, “AN388:Si470X/1X/2X/3X/4X Evaluation Board Test Procedure.” Volume = maximum for all tests. Tested at F_{RF} = 98 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN400: Si474x AM/FM Receiver Layout Guide.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled unless noted otherwise.
4. Δf = 22.5 kHz.
5. B_{AF} = 300 Hz to 15 kHz.
6. f_{RF} = 76 to 108 MHz.
7. AGC is disabled.
8. Guaranteed by characterization.
9. Measured at V_{EMF} = 60 dBµV_{EMF}.
10. Δf = 75 kHz.
11. L = 1, R = 0.
12. At LOUT and ROUT pins.

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Table 10. WB Receiver Characteristics[1] (Si4742/43 only)
(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = 25 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	F_{RF}		162.4	—	162.55	MHz
Sensitivity[2,3,4,5]		SINAD = 12 dB	—	0.65	—	µV EMF
Adjacent Channel Selectivity		±25 kHz	40	55	—	dB
Audio S/N[2,3,4,5,6]		Mono	35	45	—	dB
Audio Frequency Response Low[7]		–3 dB	—	—	300	Hz
Audio Frequency Response High[7]		–3 dB	15	—	—	kHz

Notes:
1. To ensure proper operation and receiver performance, follow the guidelines in "AN400: Si474x AM/FM receiver Layout Guide." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
2. F_{MOD} = 1 kHz.
3. Δf = 3 kHz.
4. BAF = 300 Hz to 15 kHz, A-weighted.
5. F_{RF} = 162.5 MHz.
6. Measured at V_{EMF} = 60 dBµV EMF.
7. Guaranteed by characterization.

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Table 11. AM Receiver Characteristics[1]
(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = 25 °C)

Parameter	Test Condition	Min	Typ	Max	Unit
AM Receiver					
Specifications referred to Si4740/41/42/43/44/45 application circuit with 15pF/62pF antenna dummy, voltages at antenna dummy input.					
Input Frequency	AM/MW	520	—	1710	kHz
	AM/LW	144	—	288	kHz
	AM/SW[2]	2.3	—	30	MHz
Frequency Steps		1	—	10	kHz
Sensitivity [3,5]	(S+N)/N=26 dB	—	25	34	dBuV
IP3[6]	40 and 80 kHz Offset	—	99	—	dBuV
Audio SNR [3,4,7,8]		50	53	—	dB
Audio THD [3,4,6,7,8]		—	0.1	0.5	%
Strong Signal THD [6,7,8]	RF input level 120 dBµV EMF	—	0.2	1	%
Strong Signal SINAD [6,7,8]	RF input level 120 dBµV EMF	53	55	—	dB
Power Supply Rejection Ratio[6]	ΔV_{DD} = 100 mVRMS, 100 Hz	—	40	—	dB
Audio Output Voltage [3,4]		54	60	67	mVRMS
Powerup Time[6]	From powerdown	—	—	110	ms

Notes:
1. To ensure proper operation and receiver performance, follow the guidelines in "AN400: Si474x AM/FM receiver Layout Guide." Silicon Laboratories will evaluate schematics and layouts for qualified customers.
2. Contact Silicon Labs for additional details on shortwave operation and performance.
3. FMOD = 1 kHz, 30% modulation, 2 kHz channel filter.
4. Measured at V = 74 dBµV.
5. fRF = 520 to 1710 kHz.
6. Guaranteed by characterization.
7. BAF = 300 Hz to 15 kHz.
8. fRF = 520 kHz.

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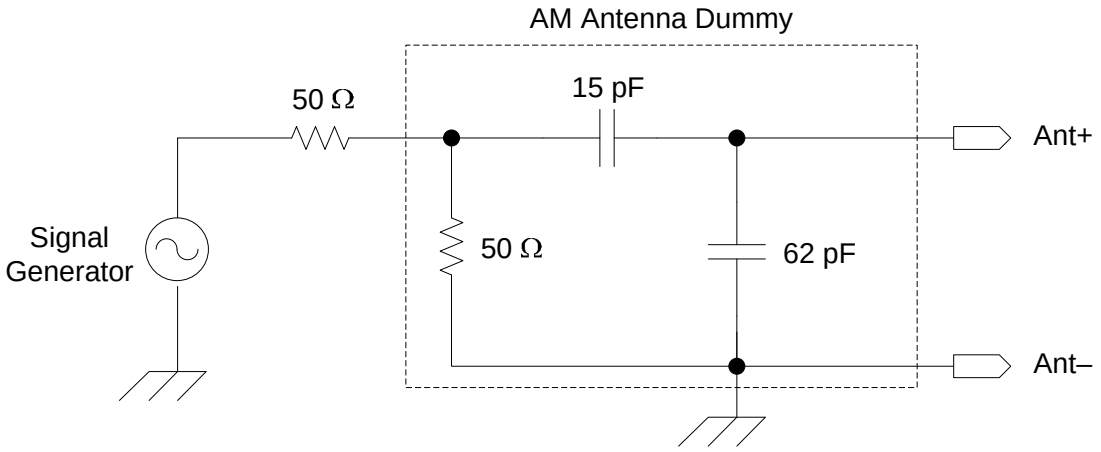

Figure 9. AM Test Circuit

Table 12. Reference Clock

(V_{DD} = 3.0 to 3.6 V, V_{IO} = 2.7 to 3.6 V, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RCLK Supported Frequencies			31.130	32.768	40,000	kHz
RCLK Frequency Tolerance			–100	—	100	ppm

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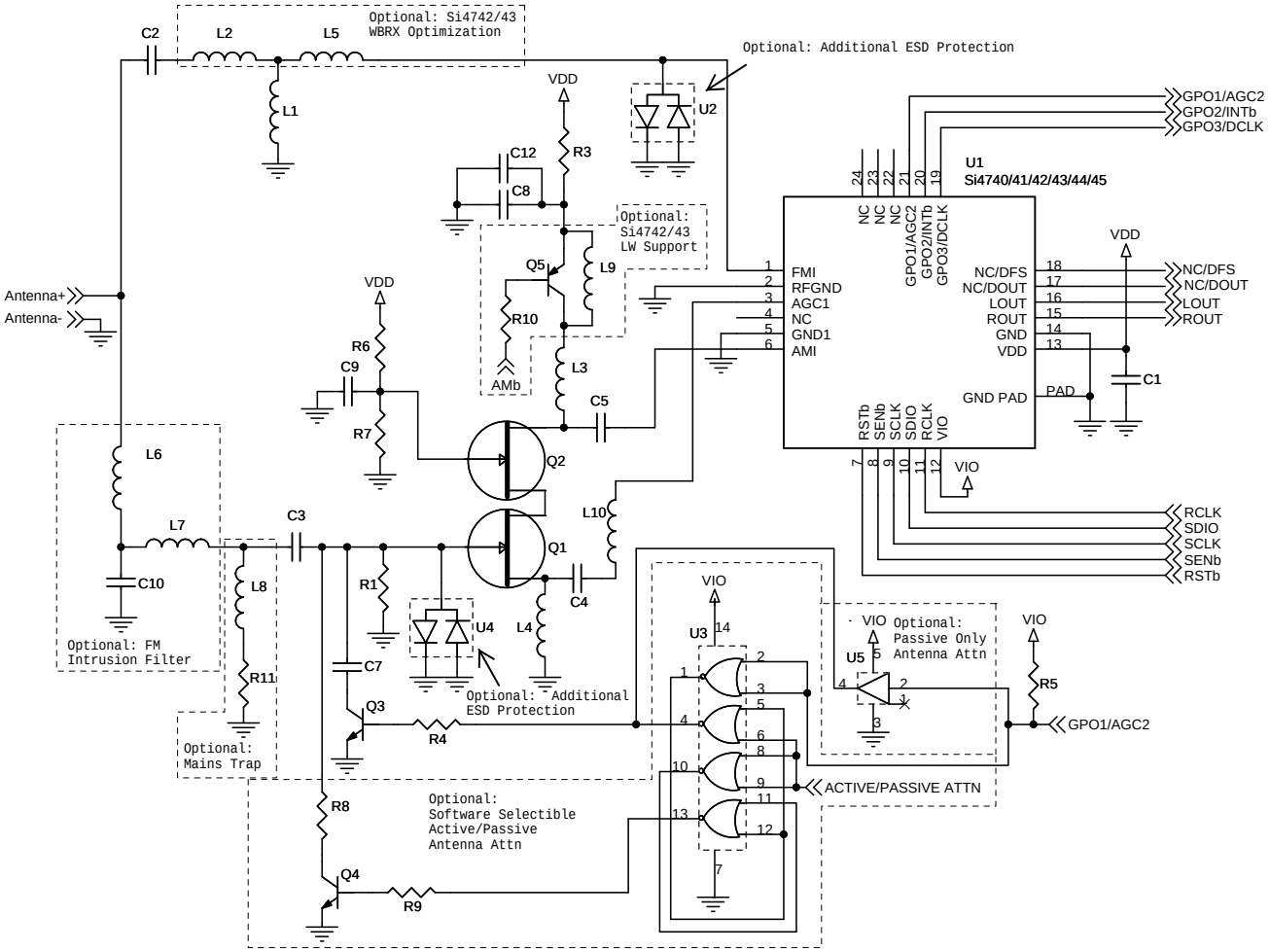
2. Typical Application Schematic



Notes:

1. Place C1 close to V_{DD} pin.
2. All grounds connect directly to GND plane on PCB.
3. To ensure proper operation and receiver performance, follow the guidelines in “AN400: Si474x AM/FM Receiver Layout Guide.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.

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3. Bill of Materials

Table 13. Si4740/41/42/43/44/45-C10 Bill of Materials

Reference	Description	Manufacturer	Part Number
C1	CAP,22 nF, ±5%, 0402,X7R	Venkel	C0402X7R250-223JNE
C2	CAP,18 pF, ±5%, 0402,COG	Venkel	C0402C0G500-180JNE
C3	CAP,270 pF, ±5%, 0402,COG	Venkel	C0402C0G500-271JNE
C4	CAP,18 nF, ±5%, 0402,X7R	Venkel	C0402X7R160-183JNE
C5,C8,C9	CAP,0.47 µF, ±5%, 0603,X7R	Venkel	C0603X7R160-474JNE
C7	CAP,1200 pF, ±5%, 0402,X7R	Venkel	C0402X7R500-122JNE
C12	CAP, 100 µF, ±20%, 1206, X5R	Venkel	C1206X5R063-107MNE
L1	IND, 120 nH, ±5%, 0603	Pulse	PE-0603CD121JTT
L3	IND,220 µH, ±10%, 1008	Coilcraft	1008PS-224KL
L4	IND,1 mH, ±20%, LPS4018	Coilcraft	LPS4018-105ML
L10	IND,33 µH, ±10%, 0805	Coilcraft	0805PS-333KL
Q1,Q2	FET,SM,SOT-23	NXP	BF862
Q3	NPN,SM,SOT-23	Fairchild Semi	MMBTH10
R1	RES,10 MΩ, ±5%, 0603	Venkel	CR0603-16W-106JT
R3	RES,10 Ω, ±1%, 0402	Venkel	CR0402-16W-10R0FT
R4,R6,R7	RES,249 Ω, ±1%, 0402	Venkel	CR0402-16W-2490FT
R5	RES,4.7 kΩ, ±5%, 0402	Venkel	CR0402-16W-472JT
U1	QFN-24, SM	Silicon Laboratories	Si4740/41/42/43/44/45-C10
Optional: Additional ESD Protection			
U2,U4	ESD DIODE ARRAY, SM	California Micro Device	CM1213
Optional: Without WBRX Optimization			
L2	IND, 33 nH, ±5%, 0603	Pulse	PE-0603CD330JTT
L5	RES, 0 Ω, 0603	Venkel	CR0603-16W-000T
Optional: Si4742/43 WBRX Optimization			
L2	IND, 100 nH, ±5%, 0603	Pulse	PE-0603CD101JTT
L5	IND, 150 nH, ±5%, 0603	Pulse	PE-0603CD151JTT
Optional: Passive Only Antenna Attenuation			
U5	BUFFER, SOT-23	TI	SN74LVC1G17DBV
Optional: FM Intrusion on AM			
C10	CAP,3.9 pF, ±0.25 pF, 0402,COG	Venkel	C0402C0G500-3R9CNE
L6,L7	IND, 6.8 µH, ±10%, 0805	Coilcraft	0805PS-682KL
Note: Specific part numbers are provided as a reference to the Si4743-C EVB. Other suppliers may be substituted.			

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Table 13. Si4740/41/42/43/44/45-C10 Bill of Materials (Continued)

Reference	Description	Manufacturer	Part Number
Optional: Mains Trap on AM			
L8	IND,47 mH, ±6%, L7PD	Toko	#388BN-1211Z
R11	RES,10 kΩ,±5%,0402	Venkel	CR0402-16W-103JT
Optional: Software Selectable Active/Passive Antenna Attenuation			
R8	RES,1 Ω, ±1%, 0402	Venkel	CR0402-16W-1R00FT
R9	RES,249 Ω, ±1%, 0402	Venkel	CR0402-16W-2490FT
Q4	NPN,SM,SOT-23	Fairchild Semi	MMBTH10
U3	QUAD GATE, 14TSSOP	TI	SN74LVC02APW
Optional: Si4742/43/44/45 LW Support			
L9	IND, 2.7 mH, ±10%, 0807	Coilcraft	RFB0807-272L
R10	RES,249 Ω, ±1%, 0402	Venkel	CR0402-16W-2490FT
Q5	PNP, SM, SOT-23	Fairchild Semi	MMBTH81
Note: Specific part numbers are provided as a reference to the Si4743-C EVB. Other suppliers may be substituted.			

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4. Description

4.1. Introduction

The Si474x AM/LW/SW/FM/WB receiver family offers 100% CMOS receiver integrated circuits (IC), providing the full receive functionality from antenna to audio for use in the automotive market. The family includes a portfolio of highly integrated receivers for primary AM/FM receivers that support worldwide broadcast audio bands and corresponding attributes including AM/FM and "college bands" down to 64 MHz, long wave, NOAA weather band, and dedicated companion RDS background receivers. The entire portfolio is layout compatible and is offered in a very small 4 x 4 x 0.85 mm 24-pin QFN package. Refer to "7. Ordering Guide" on page 39 for the corresponding part numbers.

The Si474x family implements Silicon Laboratories' proven and internationally patented digital low intermediate frequency (low-IF) receiver architecture. Silicon Labs has shipped over 100 million broadcast audio receivers worldwide using this architecture. The low-IF architecture delivers superior performance while integrating the great majority of external components required by competing solutions.

The Si474x products are feature-rich solutions, providing both highly automated performance, according to Silicon Laboratories' recommended settings, and extensive flexibility for customized audio and system performance. Programmable algorithms include advanced seek with multiple signal qualifiers and thresholds in all supported bands, FM stereo blend rates and thresholds, soft mute characteristics, multi-path detection and mitigation, AM/FM noise blankers, and selectable FM Hi-cut filters. The part accepts programmable reference clock values. The IC provides audio output in standard line-level analog audio using high fidelity stereo DACs or digital audio format.

The Si4741, Si4743, Si4745, and all other family parts ending with an odd number, offer a fully-integrated preprocessor for the European Radio Data System (RDS) and the North American Radio Broadcast Data System (RBDS). The RDS preprocessor includes all symbol decoding, advanced error-correction, detailed visibility to block-error rates (BLER), synchronization status and times, and complete, decoded and error-corrected RDS group presentation. The Si474x RDS-enabled parts also offer several modes of operation for various applications which require more or less visibility to the RDS status and group data.

Table 14. Si4740/41/42/43/44/45 Product Family

Feature	Si4740	Si4741	Si4742	Si4743	Si4744	Si4745
FM band coverage	✓	✓	✓	✓	✓	✓
FM RDS reception		✓		✓		✓
AM band coverage	✓	✓	✓	✓	✓	✓
LW band coverage			✓	✓	✓	✓
SW band coverage			✓	✓	✓	✓
WB (w/o SAME) band coverage			✓	✓		
FM multi-path detection and stereo/mono blend mitigation	✓	✓	✓	✓	✓	✓
Advanced stereo-mono blend	✓	✓	✓	✓	✓	✓
Advanced soft mute	✓	✓	✓	✓	✓	✓
Hi-cut			✓	✓	✓	✓
FM noise blanker			✓	✓	✓	✓
AM noise blanker			✓	✓	✓	✓
Digital audio I^2S		✓		✓		✓

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4.2. Block Diagram and Functional Description

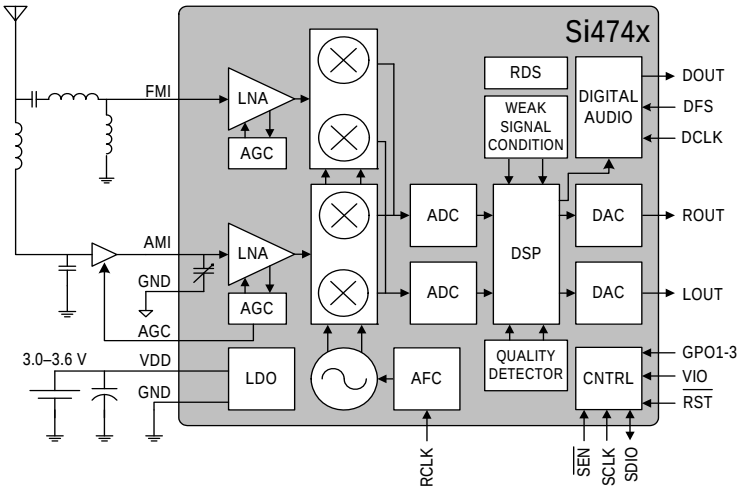

Figure 10. Functional Block Diagram

The Si474x IC family integrates the voltage controlled oscillator (VCO) and frequency synthesizer and accepts a wide range of programmable reference clocks (RCLK). The frequency synthesizer generates the quadrature local oscillator signal used to downconvert the RF input to a low intermediate frequency. The VCO frequency is locked to the RCLK and adjusted with an automatic frequency control (AFC) servo loop during reception. The VCO frequency is modified according to the programmed target frequency.

The Si474x family uses a digital low-IF architecture that integrates the entire receive chain for AM MW, AM LW, AM SW, FM, and weather band, and eliminates the requirement for expensive external ceramic filters found in competing solutions. The IC also integrates the majority of external components and performs all processing in an on-chip digital signal processor (DSP) and 8051 microcontroller (MCU) core.

The analog chains for AM and FM include dedicated low-noise amplifiers (LNA), automatic gain control (AGC), image-reject quadrature mixers, programmable gain amplifiers (PGA), and a set of delta-sigma analog-to-digital converters (ADCs).

The FM and AM LNA blocks receive wide-band frequency inputs at the FMI and AMI input pins respectively. For AM, an on-chip varactor and resistor array control the gain of the external AM antenna network. For FM, the external network is designed to provide a small boost to the FM band.

The LNA gain is dynamically controlled by the AGC loop, contingent on the RF peak detectors and signal strength. Each receive path continues to dedicated quadrature mixers which downconvert the received signal from RF to low-IF, filter for out-of-band interferers, and perform a transfer function to shift the tuned frequency to dc. A pair of PGAs filters the mixer output from interferers and amplifies the signal again before delivering it to two high resolution ADCs. The ADCs generate high dynamic range signals and deliver them to the digital core for additional processing.

The digital core consists of a DSP, 8051 MCU core, memory access controller, control interface circuitry, and general programming interface functionality.

The MCU works in conjunction with the DSP to provide access to signal quality indicators and system behavior, as well as managing the IC control interface and communication with the host processor.

The Si474x digital core performs channel selection and filtering for all supported worldwide bands. The digital core calibrates tuning and performs AM/FM demodulation and FM stereo MPX audio processing. The digital core also performs signal quality processing including received signal strength indicators, impulse detection, SNR calculations, volume control, mute, and additional digital filtering. The Si4740 supports FM de-emphasis of 50 or 75 µs.

The stereo digital audio signal is then converted back to Left (L) and Right (R) analog with a pair of high resolution, digital-to-analog converters (DACs) and is available as line-level audio on the LOUT and ROUT pins. Additionally, the stereo digital audio is also provided via an I^2S interface (Si4741/43/45 only). The device supports I^2C-compatible 2-wire control interface and SPI 3-wire control interface.

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4.3. FM Receiver Front-end

The Si474x family integrates the entire FM receive chain from antenna to audio out. The FM band is received on the FMI pin via an input coupling network with the recommended application circuit. This input coupling network isolates the FM band for best performance. The LNA supports US, Europe, Japan, OIRT, and Rest of World FM broadcast bands (64 to 108 MHz). The AGC circuit automatically controls the LNA gain to optimize sensitivity and rejection of strong interferers. For testing purposes, the AGC can be disabled. Refer to “AN388: Si470X/1X/2X/3X/4X Evaluation Board Test Procedure” for Si474x testing procedures.

4.4. AM Receiver Front-end

The Si474x family provides an integrated LNA, which works in conjunction with an external cascode amplifier to provide an AM receive chain from antenna to audio out. There are very few external components and no manual alignment required. The AM signal is received on the AMI pin via a cascode amplifier external circuit. The cascode circuit degeneration is automatically adjusted via the AGC pin as shown in Section "2. Typical Application Schematic" on page 17. The amount of degeneration depends on the signal strength. An additional GPO1 signal is used to attenuate the signal via a shunt for very strong signal handling when the signal exceeds the AGC pin degenerative control of the cascode amplifier stage.

4.5. Received Signal Qualifiers

A tuned signal's quality can vary with the environmental conditions, time of day, and position of the antenna among many other factors. To adequately manage the audio output and avoid unpleasant audible effects to the end-user, the Si474x monitors and provides indicators of the signal quality, allowing the host processor to perform additional processing if required by the customer. The Si474x monitors and reports a set of standard industry signal quality metrics including RSSI, SNR, and multi-path interference on FM signals.

As with other Si474x features, how these variables are used to improve audio performance can be left to the Silicon Labs on-chip algorithms (recommended), or they can be brought out for host-processor instructions.

4.6. Digital Audio Interface (Si4741/43/45 only)

The digital audio interface operates in slave mode and supports three different audio data formats:

- I^2S
- Left-Justified
- DSP Mode

4.6.1. Audio Data Formats

In I^2S mode, by default the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is low, and the right channel is transferred when the DFS is high.

In Left-Justified mode, by default the MSB is captured on the first rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is high, and the right channel is transferred when the DFS is low.

In DSP mode, the DFS becomes a pulse with a width of one DCLK period. The left channel is transferred first, followed right away by the right channel. There are two options in transferring the digital audio data in DSP mode: the MSB of the left channel can be transferred on the first rising edge of DCLK following the DFS pulse or on the second rising edge.

In all audio formats, depending on the word size, DCLK frequency and sample rates, there may be unused DCLK cycles after the LSB of each word before the next DFS transition and MSB of the next word. In addition, if preferred, the user can configure the MSB to be captured on the falling edge of DCLK via properties.

The number of audio bits can be configured for 8, 16, 20, or 24 bits.

4.6.2. Audio Sample Rates

The device supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz.

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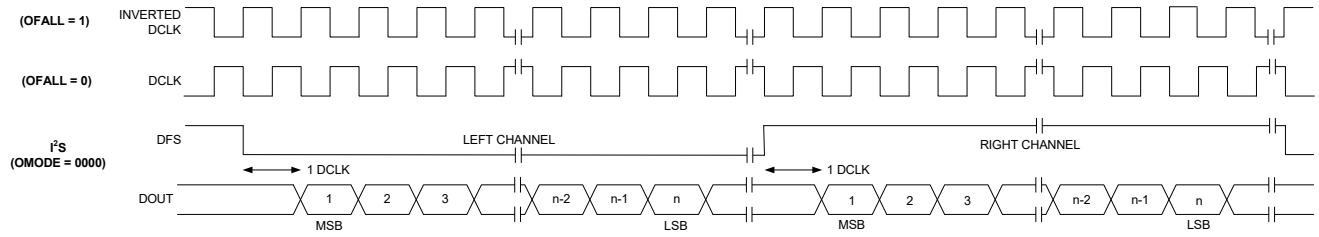

Figure 11. I²S Digital Audio Format

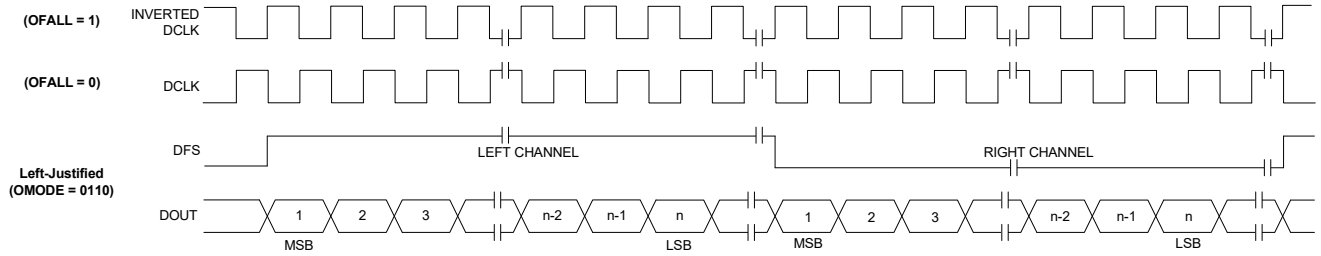

Figure 12. Left-Justified Digital Audio Format

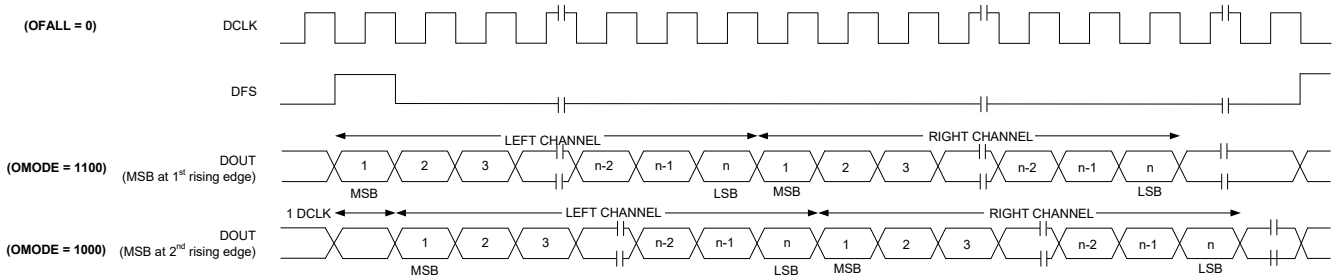

Figure 13. DSP Digital Audio Format

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4.7. Stereo Audio Processing

The output of the FM demodulator is a stereo multiplexed (MPX) signal. The MPX standard was developed in 1961, and is used worldwide. Today's MPX signal format consists of left + right (L+R) audio, left – right (L–R) audio, a 19 kHz pilot tone, and RDS/RBDS data as shown in Figure 14 below.

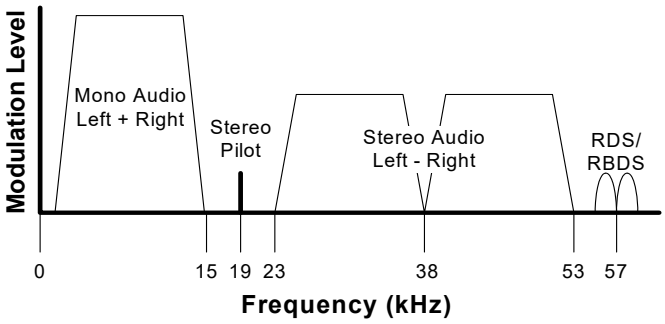

Figure 14. MPX Signal Spectrum

4.7.1. Stereo Decoder

The Si4740/41/42/43/44/45-C10's integrated stereo decoder automatically decodes the MPX signal using DSP techniques. The 0 to 15 kHz (L+R) signal is the mono output of the FM tuner. Stereo is generated from the (L+R), (L–R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L–R) signal. The left and right channels are obtained by adding and subtracting the (L+R) and (L–R) signals, respectively.

4.7.2. Stereo-Mono Blending

Adaptive noise suppression is employed to gradually combine the stereo (L–R) audio signal to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. Three metrics, received signal strength indicator (RSSI), signal-to-noise ratio (SNR), and multi-path interference, are monitored simultaneously in forcing a blend from stereo to mono. The metric which reflects the minimum signal quality takes precedence and the signal is blended appropriately.

All three metrics have programmable stereo/mono thresholds and attack/release rates as shown in the Table 15 and Table 16.

If a metric falls below its mono threshold, the signal is blended from stereo to full mono. If all metrics are above their respective stereo thresholds, then no action is taken to blend the signal. If a metric falls between its mono and stereo thresholds, then the signal is blended to the level proportional to the metric's value between its mono and stereo thresholds, with an associated attack and release rate. Figure 15, "Stereo-Mono Blend Based on Active Monitoring of RSSI, SNR, and Multi-Path Interference," on page 25 illustrates the stereo-mono blend. Stereo/mono status can be monitored with the FM_RSQ_STATUS command.

Table 15. Blend Threshold Properties

RSSI	FM_BLEND_RSSI_STEREO_THRESHOLD	FM_BLEND_RSSI_MONO_THRESHOLD
SNR	FM_BLEND_SNR_STEREO_THRESHOLD	FM_BLEND_SNR_MONO_THRESHOLD
Multi-path interference	FM_BLEND_MULTIPATH_STEREO_THRESHOLD	FM_BLEND_MULTIPATH_MONO_THRESHOLD

Table 16. Blend Attack/Release Rate Properties

RSSI	FM_BLEND_RSSI_ATTACK_RATE	FM_BLEND_RSSI_RELEASE_RATE
SNR	FM_BLEND_SNR_ATTACK_RATE	FM_BLEND_SNR_RELEASE_RATE
Multi-path interference	FM_BLEND_MULTIPATH_ATTACK_RATE	FM_BLEND_MULTIPATH_RELEASE_RATE

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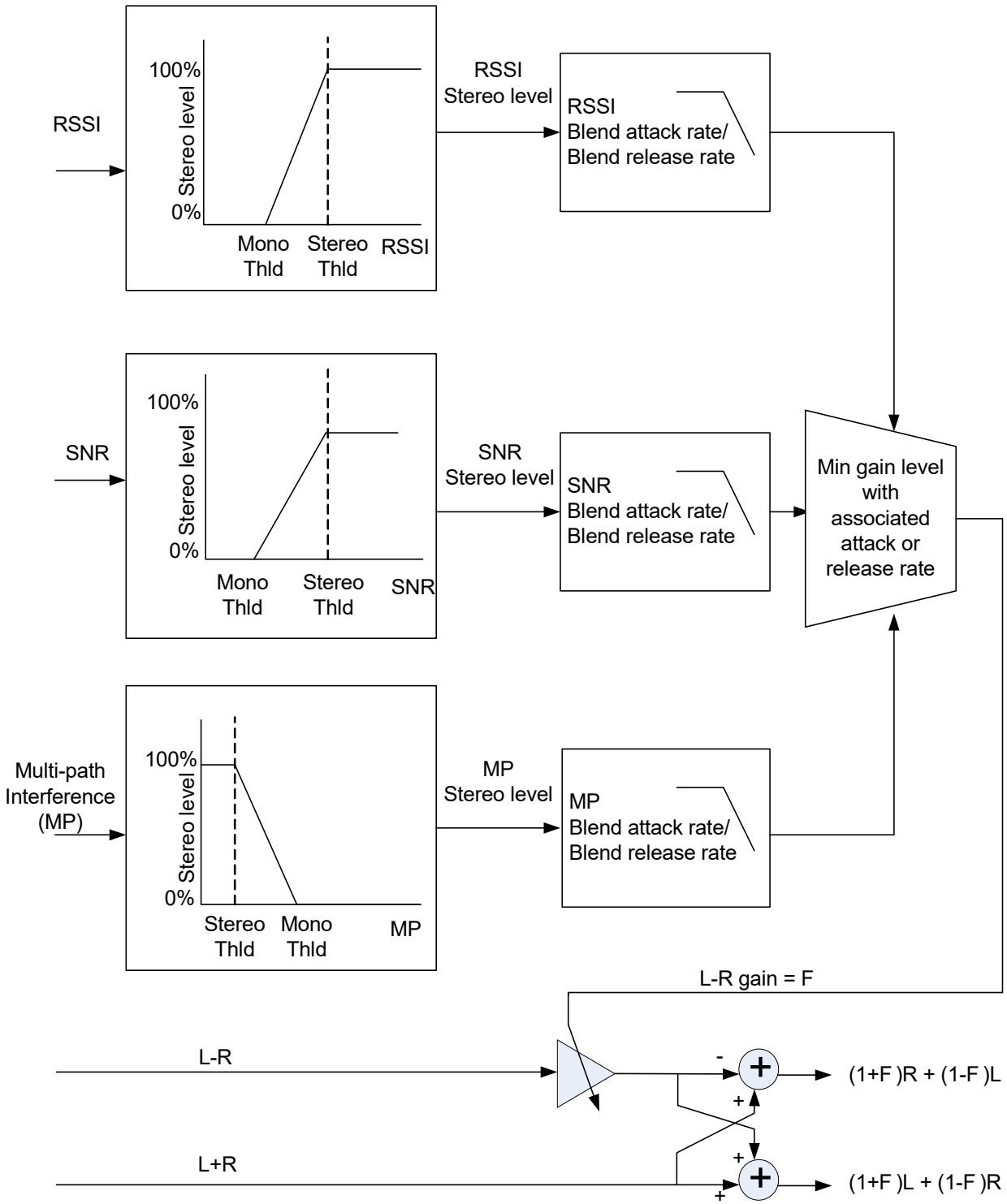

Figure 15. Stereo-Mono Blend Based on Active Monitoring of RSSI, SNR, and Multi-Path Interference

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4.8. De-emphasis

De-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high-frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. The Si474x incorporates a de-emphasis filter which attenuates high frequencies to restore a flat frequency response. Two time constants are used in various regions. The de-emphasis time constant is programmable to 50 or 75 µs and is set by the FM_DEEMPHASIS property.

4.9. Stereo DACs

High-fidelity stereo digital-to-analog converters (DACs) drive analog audio signals onto the LOUT and ROUT pins. The audio output may be muted. Volume is adjusted digitally with the RX_VOLUME property. It is necessary that the volume be maintained at maximum levels to ensure the highest dynamic range audio outputs to the external audio processing stage in a car radio.

4.10. Soft Mute

The soft mute feature is available to attenuate the audio outputs and minimize audible noise in very weak signal conditions. This process is shown conceptually in Figure 16. The Si474x triggers soft mute feature by monitoring the SNR metric. The SNR threshold for activating soft mute is programmable, as are soft mute attenuation levels and attack and release rates. The Si474x provides the soft mute feature in FM and AM bands.

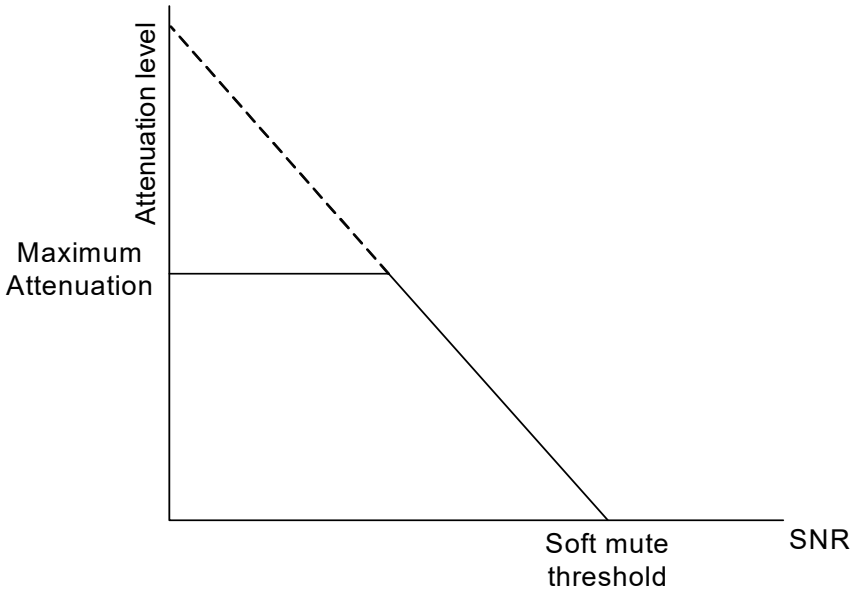

Figure 16. Soft Mute Based on Active Monitoring of SNR

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4.11. Seek and Valid Station Qualification

The seek function will search up or down the selected frequency band for a valid channel. A valid channel is qualified according to a series of programmable signal indicators and thresholds. The seek function can be made to stop at the band edge and provide an interrupt, or wrap the band and continue seeking until arriving at the original departure frequency. The device sets interrupts with found valid stations, or if the seek results in zero found valid stations, the device indicates failure and again sets an interrupt.

The Si474x seek functionality is performed completely on-chip or can be brought out to a companion processor. The Si474x can provide base values for signal quality variables to a companion processor for qualification or can further process the base values to qualify valid or invalid stations.

The Si474x uses RSSI, SNR, and AFC to qualify stations. Most of these metrics have programmable thresholds to tailor the seek function to the subjective tastes of customers.

RSSI is employed first to screen all possible candidate stations. SNR and AFC are subsequently used in screening the RSSI qualified stations. The more thresholds the system engages, the higher the confidence that any found stations will indeed be valid broadcast stations; however, the more challenging levels the thresholds are set to, the longer the overall seek time as more stations and more qualifiers will be assessed. It is recommended that RSSI be set to a mid-level threshold in conjunction with an SNR threshold set to a level delivering acceptable audio performance. This trade-off will eliminate very low RSSI stations whilst keeping the seek time to acceptable levels. Generally, the time to auto-scan and store valid channels for an entire AM or FM band with all thresholds engaged is very short depending on the band content.

Seek is initiated using the FM_SEEK_START or AM_SEEK_START commands. The RSSI and SNR threshold settings are adjustable using properties.

4.12. FM Hi-Cut Control (Si4742/43/44/45 only)

Hi-cut control is employed on audio outputs with degradation of the signal due to low SNR and/or multi-path interference. Two metrics, SNR and multi-path interference, are monitored concurrently in forcing hi-cut of the audio outputs. Programmable minimum and maximum thresholds are available for both metrics. The transition frequency for hi-cut is also programmable with up to seven hi-cut filter settings. A single set of attack and release rates for hi-cut are programmable for both metrics from a range of 2 ms to 64 s. Figure 17, “FM Hi-Cut Based on Active Monitoring of SNR and Multi-Path Interference,” illustrates hi-cut. The level of hi-cut applied can be monitored with the FM_RSQ_STATUS command. Hi-cut can be disabled by setting the hi-cut filter setting to the default audio bandwidth of 15 kHz.

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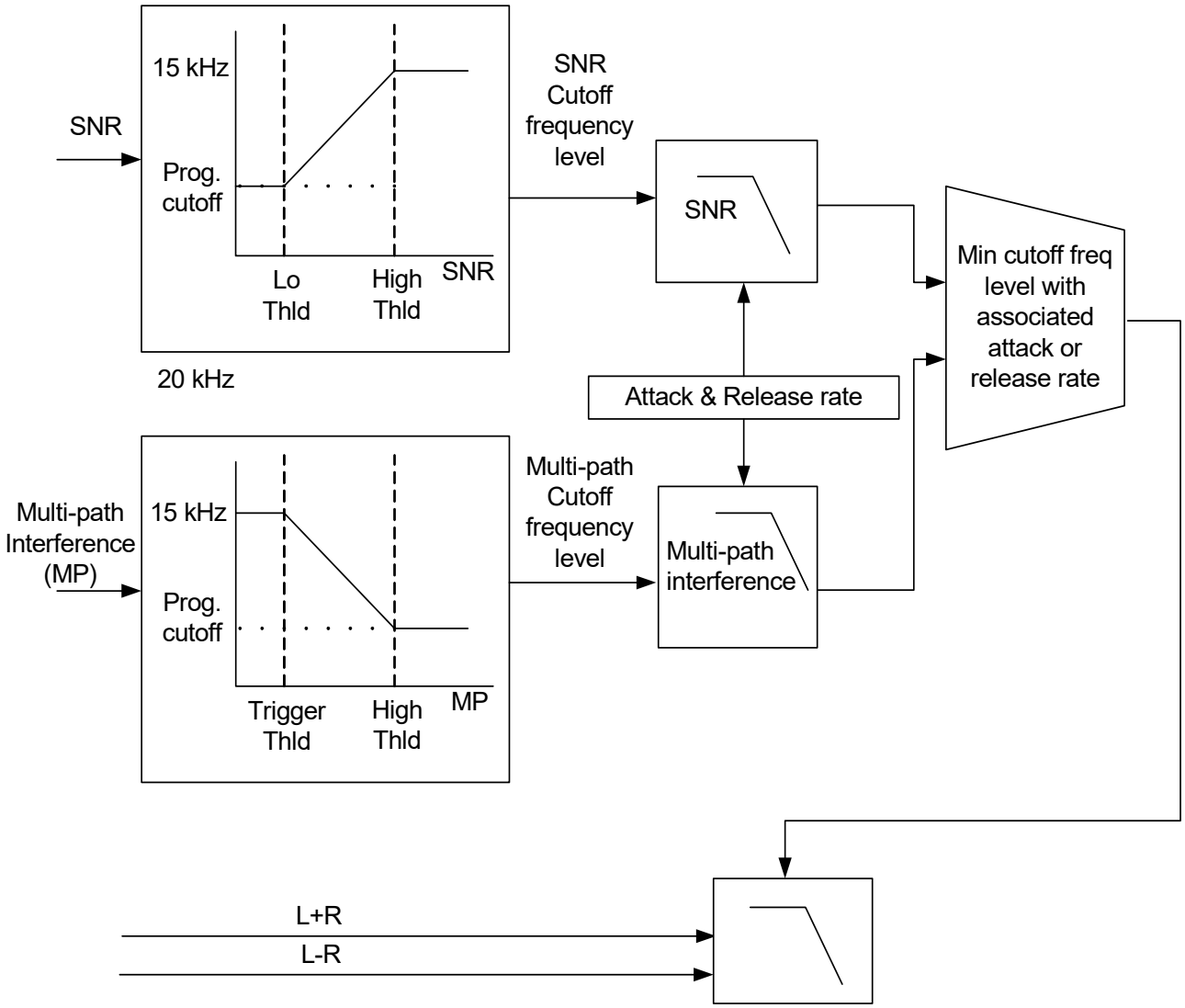

Figure 17. FM Hi-Cut Based on Active Monitoring of SNR and Multi-Path Interference

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4.13. AM/FM Noise Blanker (Si4742/43/44/45 only)

In an automotive environment, noise spikes from engine ignition and/or various other electrical sources can significantly impair and disrupt the audio output. The Si4742/43/44/45 includes a noise blanker to mitigate or eliminate these noise spikes and audible artifacts. Figure 18 shows a conceptual flow chart for the Si4742/43/44/45 noise blanking function. The Si4742/43/44/45 offers five properties for configuring the AM and FM noise blankers including detection threshold, blanking interval, trigger rate, noise-floor bandwidth, and delay. Each property is configurable for adopting customers to refine and apply unique noise-blank behavior.

4.13.1. FM Noise Blanker Property Settings

The FM noise blanker detection threshold property sets the level threshold for detection of the noise impulses/spikes in dB from a range of 1 dB to 90 dB above the noise floor. The FM noise blank rate property sets the maximum rate in Hz at which the noise blanker is triggered from a range of 100 Hz to 6400 Hz. The FM noise blank interval property sets the noise blanking interval in microseconds at which the original samples are replaced by interpolated "clean" samples from a range of 8 µs to 48 µs. The FM noise blanker IIR filter property sets the noise floor bandwidth from a range of 390 Hz to 2480 Hz. This property sets the rms noise floor above which the noise impulse level detect threshold is set for noise impulse detection. The FM noise blank delay property sets the delay in microseconds in applying impulse blanking to the original samples, which allows for insertion and alignment of the blanked samples with the original sampled signal. The range of values for FM noise blanker delay is 125 µs to 219 µs.

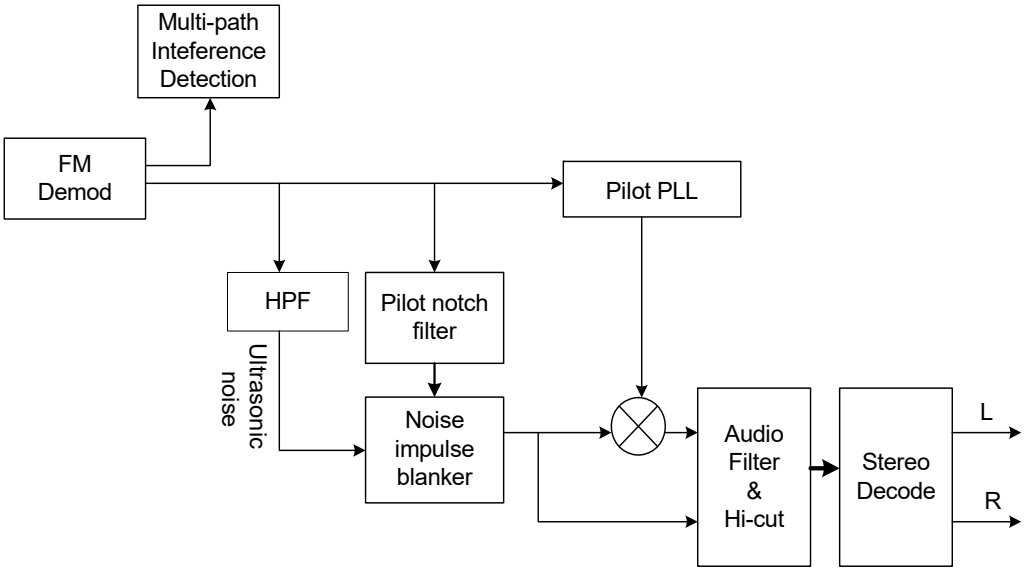

Figure 18. Illustration of Noise Blanker in FM Signal Path

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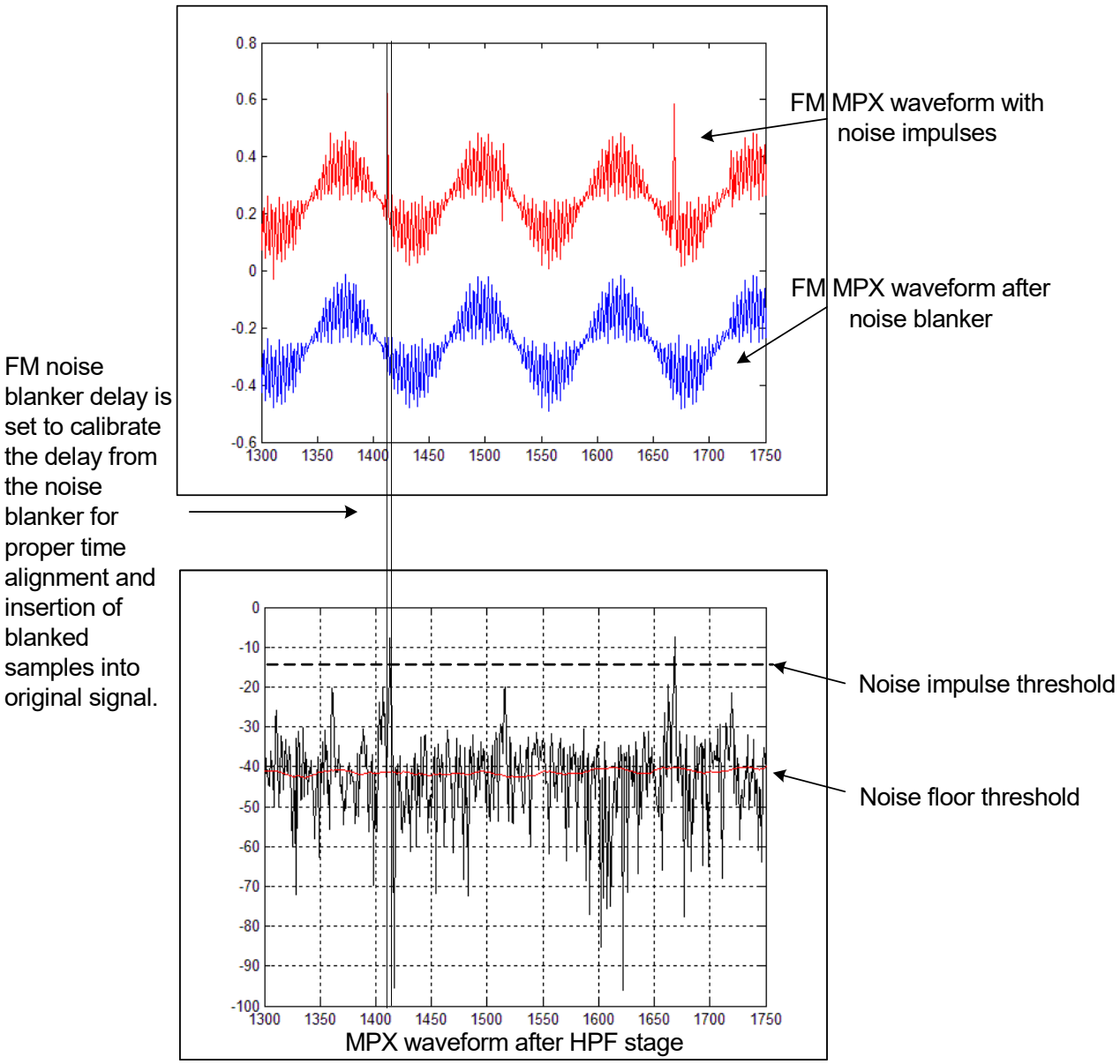

Figure 19. Illustration of FM Noise Blanker Property Settings for Proper Detection of Noise Impulses (FM MPX waveforms are offset vertically for illustration purposes)

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4.13.2. AM Noise Blanker Property Settings

The AM noise blanker detection threshold property sets the level threshold for detection of the noise impulses/spikes in dB from a range of 1 dB to 90 dB above the noise floor. The AM noise blank rate property sets the maximum rate in Hz at which the noise blanker is triggered from a range of 100 Hz to 6400 Hz. The AM noise blank interval property sets the blanking interval in microseconds at which the original samples are replaced by previous samples using a "sample and hold" scheme from a range of 15 µs to 110 µs. The AM noise blanker IIR filter property sets the noise floor bandwidth from a range of 300 Hz to 2480 Hz. This property sets the rms noise floor above which the noise impulse level detect threshold is set for noise impulse detection. The AM noise blank delay property sets the delay in microseconds in applying impulse blanking to the original samples, which allows for insertion and alignment of the blanked samples with the original sampled signal. The range of values for the AM noise blanker delay is 125 µs to 219 µs.

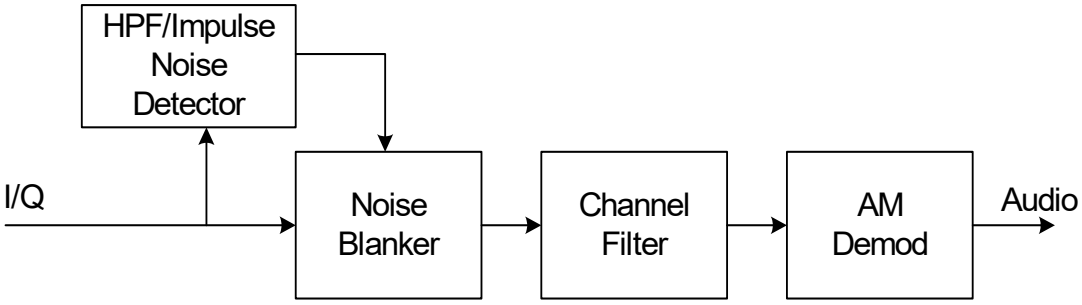

Figure 20. Illustration of Noise Blanker in AM Signal Path.

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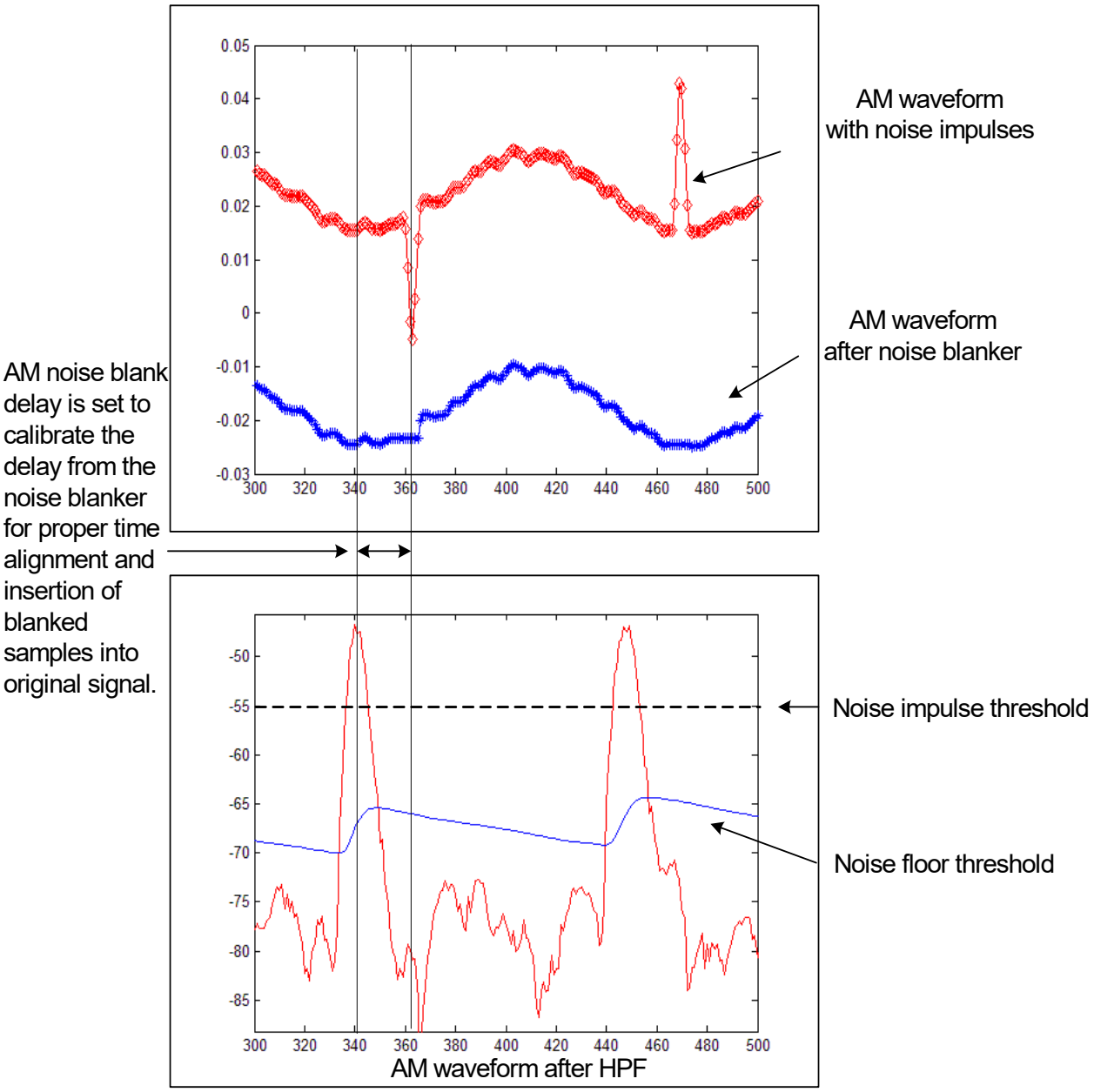

Figure 21. Illustration of AM Noise Blanker Property Settings for Proper Detection of Noise Impulses (AM Waveforms are Offset Vertically for Illustration Purposes)

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4.14. Programming Section

To ease development time and offer maximum customization, the Si474x provides a simple and powerful software interface to program the receiver. The device is programmed using commands, arguments, properties, and responses.

To perform an action, the user writes a command byte and associated arguments causing the chip to execute the given command. Commands control actions such as powerup, powerdown, or tune to a station. Arguments are specific to a given command and are used to modify the command.

Properties are a special command + argument used to modify the default chip operation and are generally configured immediately after powerup. Examples of properties are de-emphasis, RSSI seek threshold, and soft mute attenuation.

Responses provide information and are echoed after a command + arguments are issued and processed. All commands provide a one-byte status update indicating interrupt and clear-to-send status information.

For a detailed description of the commands and properties for the Si474x, see "AN332: Si47xx Programming Guide" and “AN344: Si4706/07/4x Programming Guide.”

4.15. Reset, Powerup, and Powerdown

Setting the RST pin low will disable analog and digital circuitry, reset the registers to their default settings, and disable the bus. Setting the RST pin high will bring the device out of reset. The powerup mode powers up the device and provides mode selection. Mode selections include AM, FM, or WB receiver and analog or digital audio output. A powerdown mode is available to reduce power consumption when the part is idle. Putting the device in powerdown mode will disable analog and digital circuitry while keeping the bus active.

4.16. GPO 1–3

The GPO 1–3 pins can be set to output a constant low or high output, or optionally be set to provide a hardware interrupt to the controller such as scan complete, stereo/mono indicator, and RDS/RBDS. After reset and POWER_UP into AM receiver mode, GPO1 is reserved for AM AGC external attenuator control.

4.17. RDS/RBDS Advanced Processor

The Si4741/43/45 implements an advanced, patented, high-performance RDS processor for demodulation, symbol decoding, block synchronization, error detection, and error correction. The RDS decoder applies advanced decoding and statistical decision techniques to provide very high-performance synchronization at very noisy signal levels, and excellent sensitivity at industry-standard block error rate (BLER) levels (5%).

The Si4741/43/45’s strong synchronization performance in very noisy/low SNR environments minimizes the number of instances of lost synchronization. Other less robust tuners must attempt to resynchronize in low SNR environments, resulting in lost data and lengthy delays in reestablishing data reception. The Si4741/43/45 maintains synchronization to the RDS transmission, despite high BLER. This results in fewer dropped connections, minimal resynchronization time, and greater data reliability in low SNR environments. Figure 22 illustrates the benefits of the Si4741/43/45 robust synchronization persistence.

The Si4741/43/45 decoder additionally provides more reliable data decoding performance in low carrier to noise (CNR) environments. This results in very low decoder implementation loss figures and substantial improvements over other RDS standard implementations.

Figure 23 illustrates the Si4741/43/45 RDS decoder performance. The decoder failure probability drops significantly when compared to a standard RDS decision-based decoder for given energy per bit/noise density (E_b/N_o).

The Si4741/43/45 report RDS decoder synchronization status and detailed bit errors for each RDS block. The range of reportable bit errors detected and corrected are 0, 1-2, 3-5, and “not correctable.” More than five errors indicates that the corresponding block information word is non-correctable.

The Si4741/43/45 also provides highly configurable interrupts based on RDS-driven events and conditions. The default settings provide an interrupt when RDS is synchronized and when RDS group data has been received. The configurable interrupts can be set to provide frequent interrupts down to a single received block with BLER. The configurable interrupts also can be set to provide very infrequent interrupts, buffering up to 25 complete RDS groups (100 blocks) with BLER by block in the on-chip FIFO. The Si4741/43/45 also provides configurable interrupts on changes or receipt of the key RDS blocks A and B. This flexibility allows adopters to either conduct extensive RDS data processing on the host or reserve the host processor in power-saving modes with minimal RDS interrupts, allowing the Si4741/43/45 to perform RDS processing on-chip. Interrupt configuration and thresholds are covered in “AN332: Si47xx Programming Guide” and “AN344: Si4706/07/4x Programming Guide,” offered under NDA.

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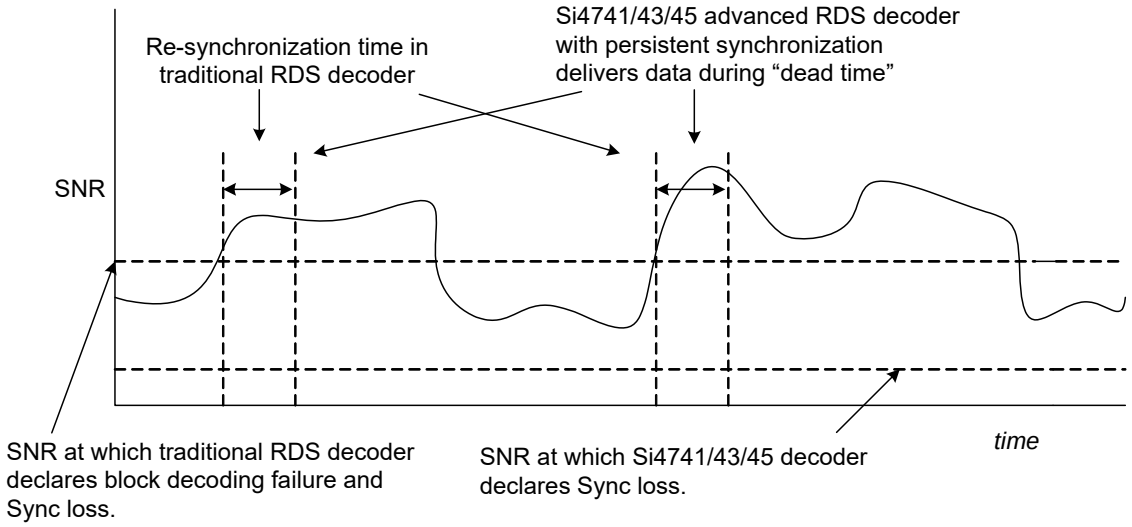

Figure 22. Illustrative Si4741/43/45 Advanced RDS Synchronization

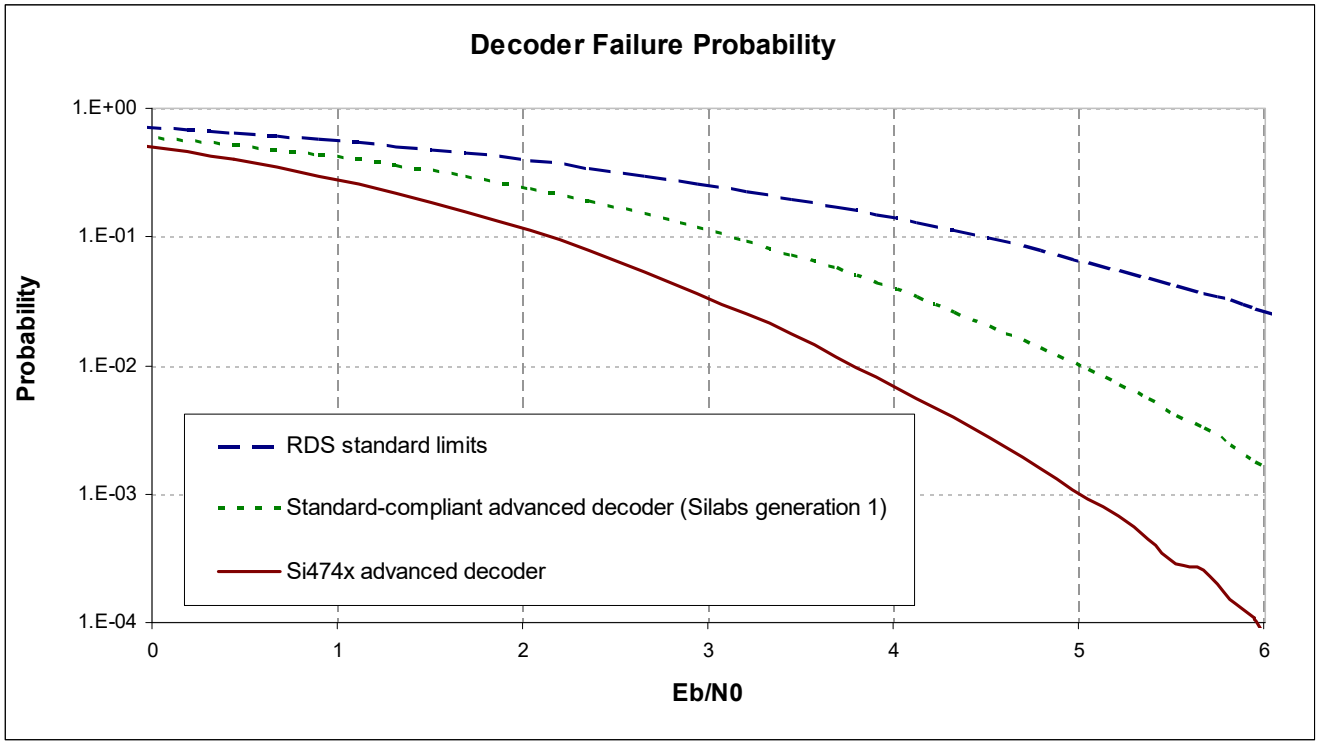

Figure 23. Si4741/43/45 Decoder Performance

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4.18. Reference Clock

The Si4740/41/42/43/44/45-C10 reference clock is programmable, supporting RCLK frequencies in Table 12. Refer to Table 3, “DC Characteristics,” on page 5 for switching voltage levels and Table 9, “FM Receiver Characteristics,” on page 12 for frequency tolerance information.

4.19. Control Interface

A serial port slave interface is provided, which allows an external controller to send commands to the Si474x and receive responses from the device. The serial port can operate in three bus modes: 2-wire mode, 3-wire mode, or SPI mode. The Si474x selects the bus mode by sampling the state of the GPO1 and GPO2 pins on the rising edge of RST. The GPO1 pin includes an internal pull-up resistor, which is connected while RST is low. The GPO2 pin includes an internal pull-down resistor, which is connected while RST is low. Therefore, it is only necessary for the user to actively drive pins which differ from these states. See Table 17.

Table 17. Bus Mode Select on Rising Edge of RST

Bus Mode	GPO1	GPO2
2-Wire	1	0
SPI	1	1 (must drive)
3-Wire	0 (must drive)	0

After the rising edge of RST, the pins GPO1 and GPO2 are used as general purpose output (O) pins. After reset and POWER_UP into AM receiver mode, GPO1 is reserved for AM AGC external attenuator control. In any bus mode, commands may only be sent after VIO and VDD supplies are applied.

In any bus mode, before sending a command or reading a response, the user must first read the status byte to ensure that the device is ready (CTS bit is high).

4.19.1. 2-Wire Control Interface Mode

When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of RST, and stays high until after the first start condition. Also, a start condition must not occur within 300 ns before the rising edge of RST.

The 2-wire bus mode uses only the SCLK and SDIO pins for signaling. A transaction begins with the START condition, which occurs when SDIO falls while SCLK is high. Next, the user drives an 8-bit control word serially on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a 7-bit device address, followed by a read/write bit (read = 1, write = 0). The Si474x acknowledges the control word by driving SDIO low on the next falling edge of SCLK.

Although the Si474x will respond to only a single device address, this address can be changed with the SEN pin (note that the SEN pin is not used for signaling in 2-wire mode). When SEN = 0, the 7-bit device address is 0010001b. When SEN = 1, the address is 1100011b.

For write operations, the user then sends an 8-bit data byte on SDIO, which is captured by the device on rising edges of SCLK. The Si474x acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. The user may write up to 8 data bytes in a single 2-wire transaction. The first byte is a command, and the next seven bytes are arguments.

For read operations, after the Si474x has acknowledged the control byte, it will drive an 8-bit data byte on SDIO, changing the state of SDIO on the falling edge of SCLK. The user acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. If a data byte is not acknowledged, the transaction will end. The user may read up to 16 data bytes in a single, 2-wire transaction. These bytes contain the response data from the Si474x.

A 2-wire transaction ends with the STOP condition, which occurs when SDIO rises while SCLK is high.

For details on timing specifications and diagrams, refer to Table 5, “2-Wire Control Interface Characteristics,” on page 7; Figure 2, “2-Wire Control Interface Read and Write Timing Parameters,” on page 8, and Figure 3, “2-Wire Control Interface Read and Write Timing Diagram,” on page 8.

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4.19.2. 3-Wire Control Interface Mode

When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

The 3-wire bus mode uses the SCLK, SDIO and SEN pins. A transaction begins when the user drives SEN low. Next, the user drives a 9-bit control word on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a 3-bit device address (A7:A5 = 101b), a read/write bit (read = 1, write = 0), and a 5-bit register address (A4:A0).

For write operations, the control word is followed by a 16-bit data word, which is captured by the device on rising edges of SCLK.

For read operations, the control word is followed by a delay of one-half SCLK cycle for bus turn-around. Next, the Si474x will drive the 16-bit read data word serially on SDIO, changing the state of SDIO on each rising edge of SCLK.

A transaction ends when the user sets SEN high, then pulses SCLK high and low one final time. SCLK may either stop or continue to toggle while SEN is high.

In 3-wire mode, commands are sent by first writing each argument to register(s) 0xA1–0xA3, then writing the command word to register 0xA0. A response is retrieved by reading registers 0xA8–0xAF.

For details on timing specifications and diagrams, refer to Table 6, “3-Wire Control Interface Characteristics,” on page 9; Figure 4, “3-Wire Control Interface Write Timing Parameters,” on page 9, and Figure 5, “3-Wire Control Interface Read Timing Parameters,” on page 9.

4.19.3. SPI Control Interface Mode

When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

SPI bus mode uses the SCLK, SDIO, and SEN pins for read/write operations. The system controller can choose to receive read data from the device on either SDIO or GPO1. In AM Receiver mode, only SIDIO is available; GPO1 is reserved for AM AGC external attenuator control. A transaction begins when the system controller drives SEN = 0. The system controller then pulses SCLK eight times, while driving an 8-bit control byte serially on SDIO. The device captures the data on rising edges of SCLK. The control byte must have one of five values:

- 0x48 = write a command (controller drives 8 additional bytes on SDIO).
- 0x80 = read a response (device drives one additional byte on SDIO).
- 0xC0 = read a response (device drives 16 additional bytes on SDIO).
- 0xA0 = read a response (device drives one additional byte on GPO1).
- 0xE0 = read a response device drives 16 additional bytes on GPO1).

For write operations, the system controller must drive exactly eight data bytes (a command and seven arguments) on SDIO after the control byte. The data is captured by the device on the rising edge of SCLK.

For read operations, the controller must read exactly 1 byte (STATUS) after the control byte or exactly 16 data bytes (STATUS and RESP1–RESP15) after the control byte. The device changes the state of SDIO (or GPO1, if specified) on the falling edge of SCLK. Data must be captured by the system controller on the rising edge of SCLK.

Keep SEN low until all bytes have transferred. A transaction may be aborted at any time by setting SEN high and toggling SCLK high and then low. Commands will be ignored by the device if the transaction is aborted.

For details on timing specifications and diagrams, refer to Figure 6 and Figure 7 on page 10.

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5. Commands and Properties

Refer to "AN332: Si47xx Programming Guide" and “AN344: Si4706/07/4x Programming Guide.”

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6. Pin Descriptions: Si4740/41/42/43/44/45-C10-GM

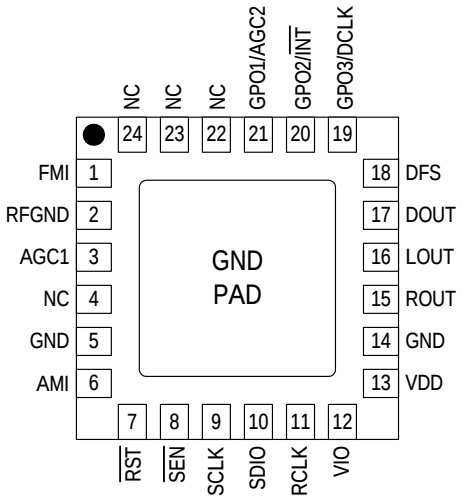

Table 18. Si4740/41/42/43/44/45-C10-GM Pin Descriptions

Pin Number(s)	Name	Description
1	FMI	FM RF inputs. FMI should be connected to the antenna trace.
2	RFGND	RF ground. Connect to ground plane on PCB.
3	AGC1	Automatic gain control. See "2. Typical Application Schematic" on page 17.
4, 22–24	NC	No connect. Leave floating.
5, 14, GND PAD	GND	Ground. Connect to ground plane on PCB.
6	AMI	AM RF input.
7	$\overline{\text{RST}}$	Device reset (active low) input.
8	$\overline{\text{SEN}}$	Serial enable input (active low).
9	SCLK	Serial clock input.
10	SDIO	Serial data input/output.
11	RCLK	External reference oscillator input.
12	V_{IO}	I/O supply voltage.
13	V_{DD}	Supply voltage. May be connected directly to battery.
15	ROUT	Right audio line output.
16	LOUT	Left audio line output.
17	DOUT	Digital output data in digital output audio mode (Si4741/43/45 only). No connect if not used.
18	DFS	Digital frame synchronization input in digital output mode (Si4741/43/45 only). No connect if not used.
19	GPO3/DCLK	General purpose output/Digital bit synchronous clock input in digital output mode (Si4741/43/45 only).
20	GPO2/$\overline{\text{INT}}$	General purpose output/interrupt pin.
21	GPO1/AGC2	General purpose output/AM external attenuator control.

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7. Ordering Guide

Part Number[1,2]	Description	Package Type	Operating Temperature
Si4740-C10-AM	AM/FM Broadcast Automotive Radio Receiver 4 x 4 x 0.825 24-pin QFN, AEC-Q100 qualification, IMDS Registration, PPAP documentation	QFN Pb-free	–40 to 85 °C
Si4741-C10-AM	AM/FM Broadcast Automotive Radio Receiver with RDS/RBDS 4 x 4 x 0.825 24-pin QFN, AEC-Q100 qualification, IMDS Registration, PPAP documentation	QFN Pb-free	–40 to 85 °C
Si4742-C10-AM	AM/FM/LW/SW/WB Broadcast Automotive Radio Receiver 4 x 4 x 0.825 24-pin QFN, AEC-Q100 qualification, IMDS Registration, PPAP documentation	QFN Pb-free	–40 to 85 °C
Si4743-C10-AM	AM/FM/LW/SW/WB Broadcast Automotive Radio Receiver with RDS/RBDS 4 x 4 x 0.825 24-pin QFN, AEC-Q100 qualification, IMDS Registration, PPAP documentation	QFN Pb-free	–40 to 85 °C
Si4744-C10-AM	AM/FM/SW/LW Broadcast Automotive Radio Receiver 4 x 4 x 0.825 24-pin QFN, AEC-Q100 qualification, IMDS Registration, PPAP documentation	QFN Pb-free	–40 to 85 °C
Si4745-C10-AM	AM/FM/SW/LW Broadcast Automotive Radio Receiver with RDS/RBDS 4 x 4 x 0.825 24-pin QFN, AEC-Q100 qualification, IMDS Registration, PPAP documentation	QFN Pb-free	–40 to 85 °C
Si4740-C10-GM	AM/FM Broadcast Automotive Radio Receiver 4 x 4 x 0.825 24-pin QFN	QFN Pb-free	–40 to 85 °C
Si4741-C10-GM	AM/FM Broadcast Automotive Radio Receiver with RDS/RBDS 4 x 4 x 0.825 24-pin QFN	QFN Pb-free	–40 to 85 °C
Si4742-C10-GM	AM/FM/LW/SW/WB Broadcast Automotive Radio Receiver 4 x 4 x 0.825 24-pin QFN	QFN Pb-free	–40 to 85 °C

Notes:

1. Add an “(R)” at the end of the device part number to denote tape and reel option; 2500 quantity per reel.
2. AM numbered devices receive full automotive quality production status, including AEC-Q100 qualification, registration with International Material Data System (iMDS), and Part Production Approval Process (PPAP) documentation. PPAP documentation is available at www.silabs.com with a registered and NDA approved user account.

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Part Number[1,2]	Description	Package Type	Operating Temperature
Si4743-C10-GM	AM/FM/LW/SW/WB Broadcast Automotive Radio Receiver with RDS/RBDS 4 x 4 x 0.825 24-pin QFN	QFN Pb-free	–40 to 85 °C
Si4744-C10-GM	AM/FM/SW/LW Broadcast Automotive Radio Receiver 4 x 4 x 0.825 24-pin QFN	QFN Pb-free	–40 to 85 °C
Si4745-C10-GM	AM/FM/SW/LW Broadcast Automotive Radio Receiver with RDS/RBDS 4 x 4 x 0.825 24-pin QFN	QFN Pb-free	–40 to 85 °C

Notes:

1. Add an “(R)” at the end of the device part number to denote tape and reel option; 2500 quantity per reel.
2. AM numbered devices receive full automotive quality production status, including AEC-Q100 qualification, registration with International Material Data System (iMDS), and Part Production Approval Process (PPAP) documentation. PPAP documentation is available at www.silabs.com with a registered and NDA approved user account.

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8. Package Markings

8.1. Si4740/41/42/43/44/45-C10 Top Mark

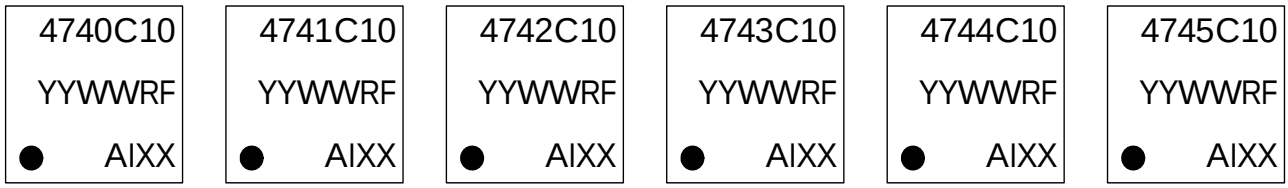

Figure 24. Si4740/41/42/43/44/45-C10 Top Mark

8.2. Top Mark Explanation

Mark Method:	YAG Laser	
Line 1 Marking:	Customer Part Number (Right-justify)	4740 = Si4740 4741 = Si4741 4742 = Si4742 4743 = Si4743 4744 = Si4744 4745 = Si4745 C = Part revision C 10 = Firmware revision 1.0
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	R = Die Rev F = Wafer Fab	First two characters of the Manufacturing Code from the Assembly Purchase Order form.
Line 3 Marking:	Circle = 0.5 mm Diameter (Bottom-Left Justified)	Pin 1 Identifier.
	A = Assembly House I = Internal Code XX = Serial Lot Number	Last four characters of the Manufacturing Code from the Assembly Purchase Order form.

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9. Package Outline: Si4740/41/42/43/44/45-C10 QFN

Figure 25 illustrates the package details for the Si4740/41/42/43/44/45-C10. Table 19 lists the values for the dimensions shown in the illustration.

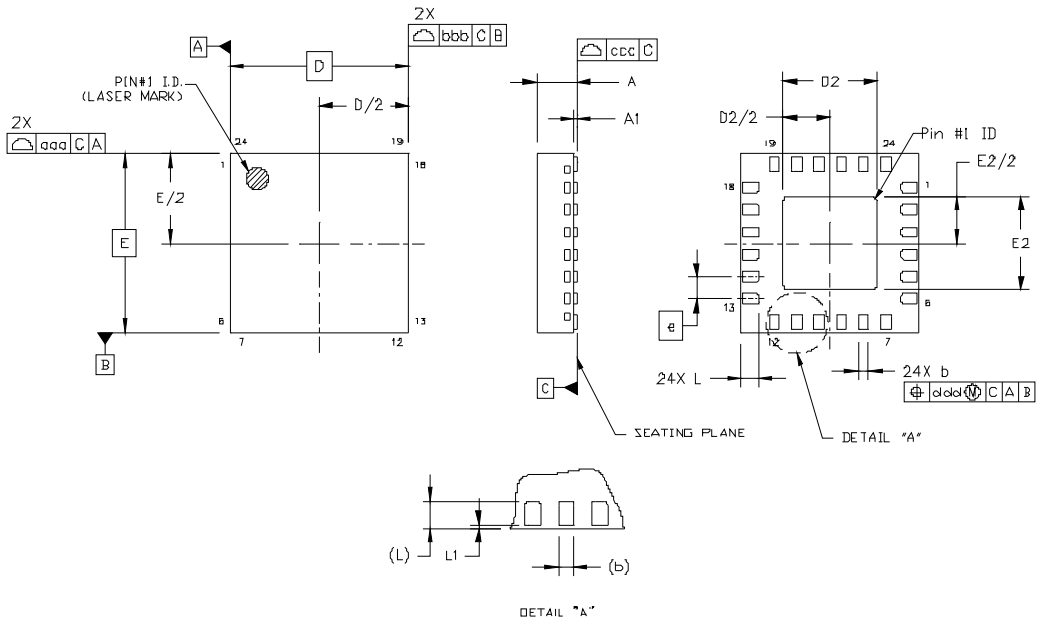

Figure 25. 24-Pin Quad Flat No-Lead (QFN)

Table 19. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC	
D2	2.00	2.10	2.20
e		0.50 BSC	
E		4.00 BSC	
E2	2.00	2.10	2.20
L	0.30	0.40	0.50
L1	0.03	0.05	0.08
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

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10. PCB Land Pattern: Si4740/41/42/43/44/45-C10 QFN

Figure 26 illustrates the PCB land pattern details for the Si4740/41/42/43/44/45-C10-GM. Table 20 lists the values for the dimensions shown in the illustration.

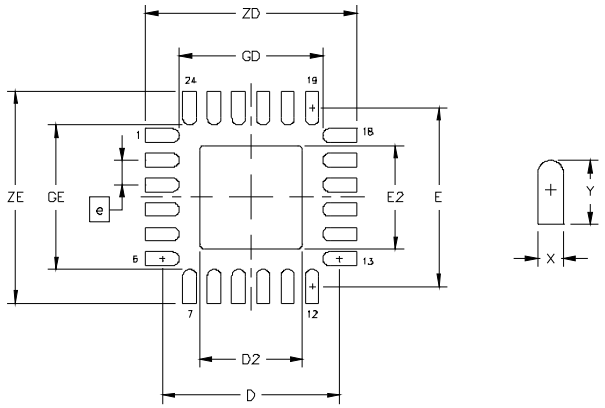

Figure 26. PCB Land Pattern

Table 20. Dimensions for PCB Land Pattern

Dimension	Min	Max
e	0.50 BSC.	
E	3.62 REF.	
D	3.62 REF.	
E2	2.00	2.20
D2	2.00	2.20

Dimension	Min	Max
GE	2.93	—
GD	2.93	—
X	—	0.28
Y	0.69 REF	
ZE	—	4.31
ZD	—	4.31

Notes: General
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes: Solder Mask Design
1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Notes: Stencil Design
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 2 x 2 array of 0.90 mm square openings on 1.15 mm pitch should be used for the center ground pad.

Notes: Card Assembly
1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

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11. Additional Reference Resources

- Si47xx Customer Support Site:
  http://www.mysilabs.com
  This site contains all application notes, evaluation board schematics and layouts, and evaluation software. NDA is required for access. To request access, register at http://www.mysilabs.com and send user's first and last name, company, NDA reference number, and mysilabs user name to fminfo@silabs.com. Silicon Labs recommends an all lower case user name.

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Document Change List

Revision 0.1 to Revision 0.2

- Added FM Hi-cut description.
- Added AM/FM Noise Blanker description.
- Updated “2. Typical Application Schematic”.
- Updated “3. Bill of Materials”.
- Added Digital Audio Output section.
- Removed crystal oscillator support.
- Updated block diagram.
- Updated pinout diagram.
- Updated “7. Ordering Guide”.
- Added package marking sections.
- Updated package outline section.
- Updated PCB land pattern section.

Revision 0.2 to Revision 0.3

- Updated Table 1 and updated Figures 3 and 12 to reflect supply voltage change to 3.6 V max.
- Updated Table 11.
- Updated Section “3. Bill of Materials”.
- Updated Section “7. Ordering Guide”
- Updated Section “8.1. Si4740/41/42/43/44/45-C10 Top Mark”
- Updated Section “8.2. Top Mark Explanation”.

Revision 0.3 to Revision 0.5

- Added SW band support to Features list.
- Updated Table 1 and all other figures and tables to reflect supply voltage change to 3.6 V max.
- Added Si4744/45 details.
- Updated Table 14
- Updated Table 3, Table 9, and Table 11

Revision 0.5 to Revision 0.8

- Updated Table 1 and all figures and tables to reflect. VIO change to 2.7 V min.
- Updated Table 9, Table 10, and Table 13.

Revision 0.8 to Revision 1.0

- Numerous updates and corrections.

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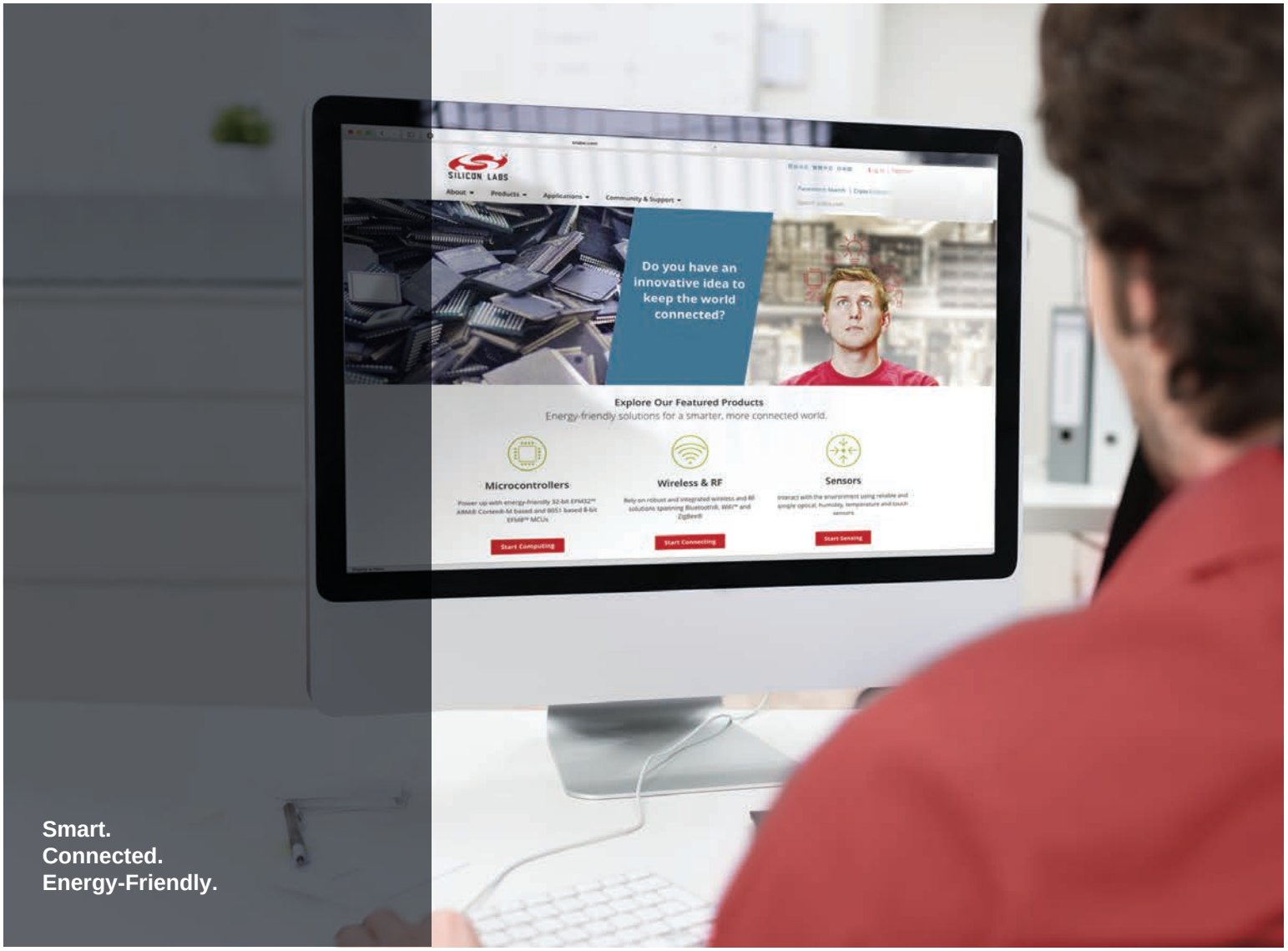

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