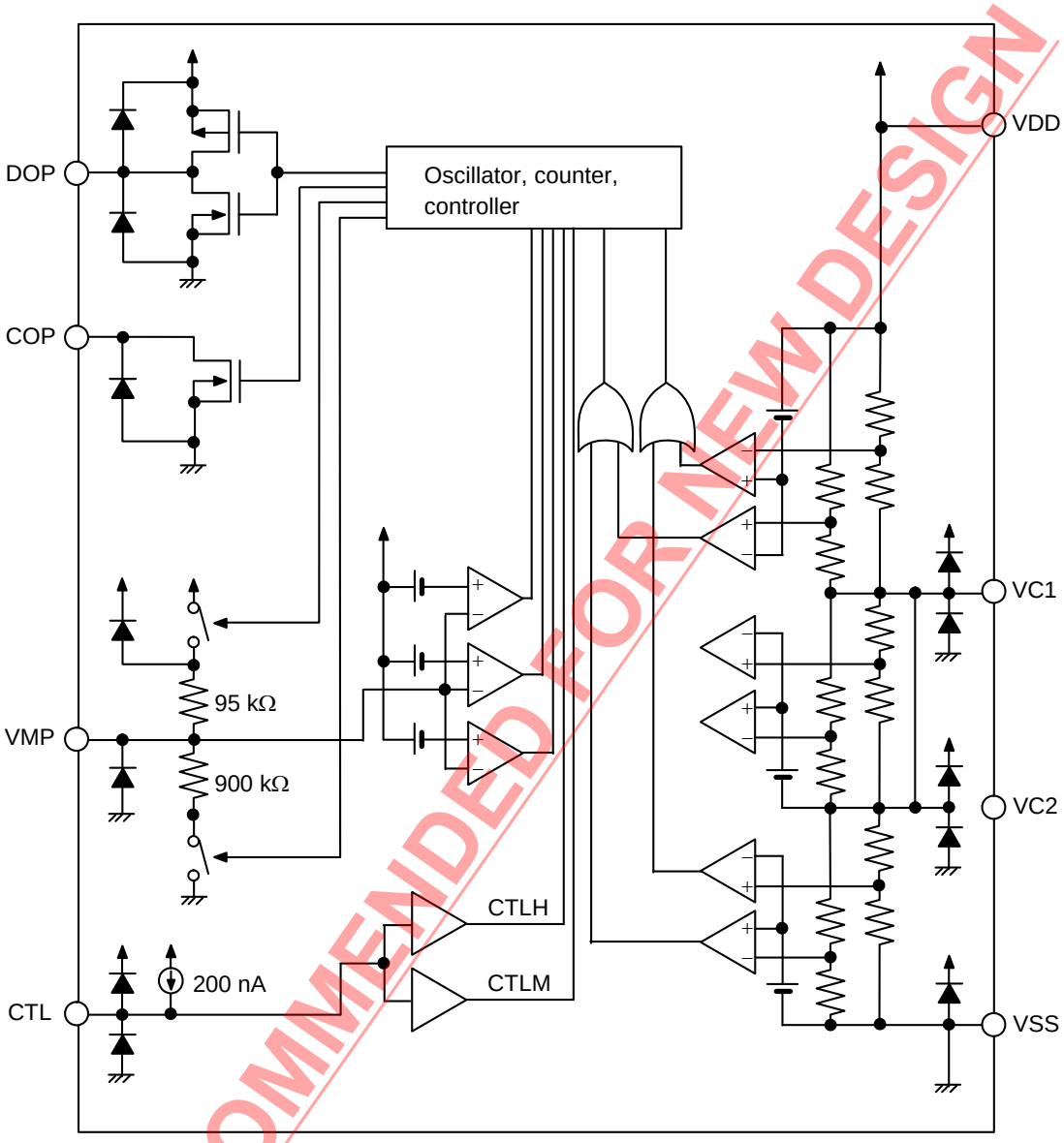
■ Block Diagrams

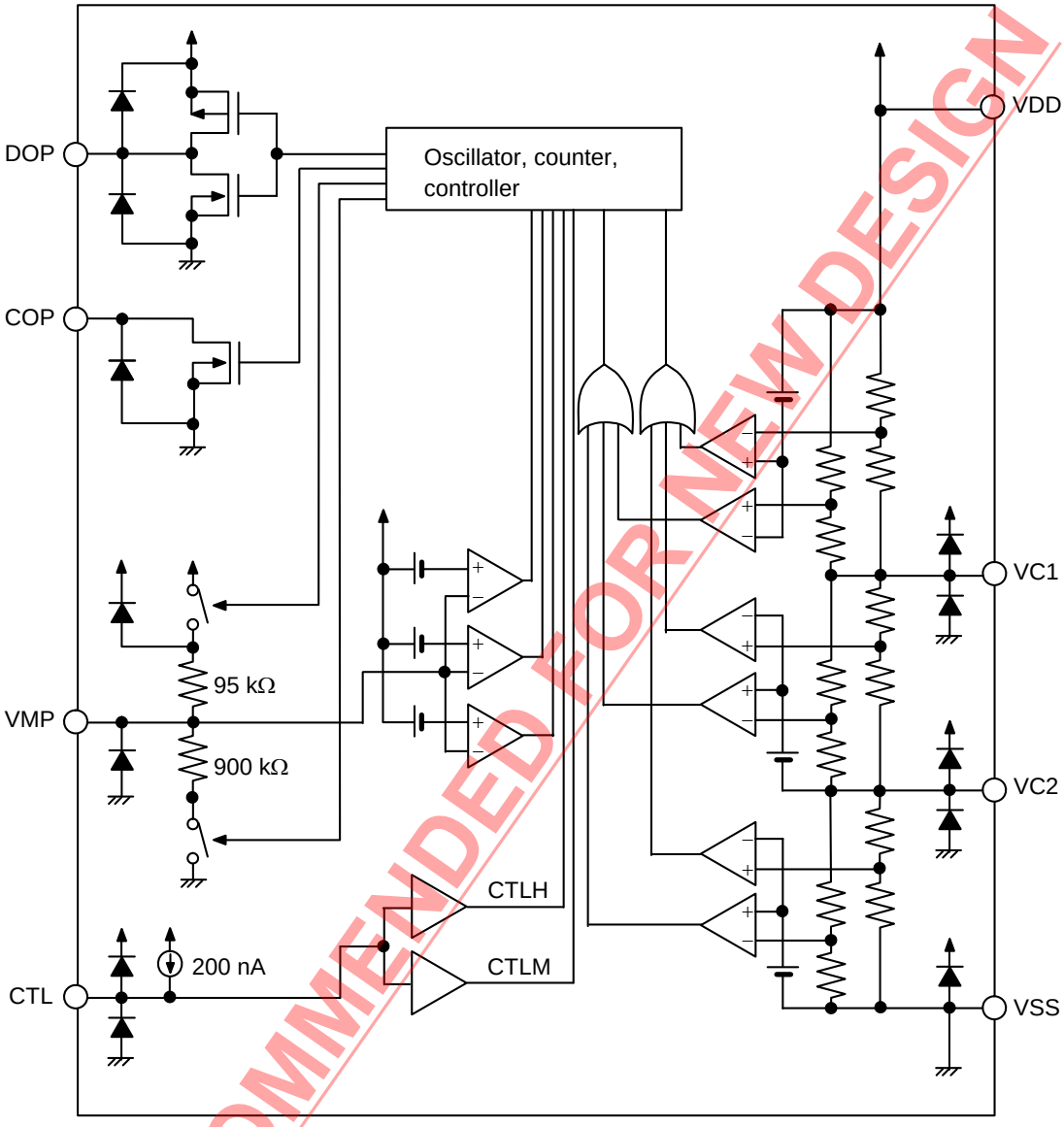
1. S-8253A Series



Remark All diodes shown in figure are parasitic diodes.

Figure 1

2. S-8253B Series



Remark All diodes shown in figure are parasitic diodes.

Figure 2

■ Product Name Structure

1. Product Name

1. 1 Environmental code = U

S-8253 x xx – T8T1 U

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- Package abbreviation and IC packing specifications*1
  - T8T1: 8-Pin TSSOP, Tape
- Serial code*2
  - Sequentially set from AA to ZZ
- Product series name
  - A: 2-cell
  - B: 3-cell

***1.** Refer to the tape specifications.
***2.** Refer to the "**3. Product Name List**".

1. 2 Environmental code = G

S-8253 x xx – T8T1 G Z

- Fixed
- Environmental code
  - G: Lead-free (for details, please contact our sales office)
- Package abbreviation and IC packing specifications*1
  - T8T1: 8-Pin TSSOP, Tape
- Serial code*2
  - Sequentially set from AA to ZZ
- Product series name
  - A: 2-cell
  - B: 3-cell

***1.** Refer to the tape specifications.
***2.** Refer to the "**3. Product Name List**".

2. Package

Package Name		Drawing Code		
		Package	Tape	Reel
8-Pin TSSOP	Environmental code = G	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-SD
	Environmental code = U	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-S1

3. Product Name List

Table 1 S-8253A Series (For 2-Serial Cell)

Model No.	Overcharge detection voltage [V_{CU}]	Overcharge release voltage [V_{CL}]	Overdischarge detection voltage [V_{DL}]	Overdischarge release voltage [V_{DU}]	Overcurrent detection voltage 1 [V_{IOV1}]	0 V battery charge function
S-8253AAA-T8T1□□	4.350 ±0.025 V	4.050 ±0.050 V	2.40 ±0.080 V	2.70 ±0.100 V	0.300 ±0.025 V	Available
S-8253AAB-T8T1□□	4.350 ±0.025 V	4.050 ±0.050 V	2.70 ±0.080 V	2.70 ±0.080 V	0.300 ±0.025 V	Available
S-8253AAC-T8T1□□	4.350 ±0.025 V	4.050 ±0.050 V	2.40 ±0.080 V	2.70 ±0.100 V	0.080 ±0.025 V	Available
S-8253AAD-T8T1□□	4.250 ±0.025 V	4.050 ±0.050 V	2.40 ±0.080 V	2.70 ±0.100 V	0.120 ±0.025 V	Available
S-8253AAE-T8T1□□	4.350 ±0.025 V	4.050 ±0.050 V	2.80 ±0.080 V	3.00 ±0.100 V	0.300 ±0.025 V	Available
S-8253AAF-T8T1□□	4.350 ±0.025 V	4.050 ±0.050 V	2.40 ±0.080 V	2.60 ±0.100 V	0.300 ±0.025 V	Unavailable
S-8253AAG-T8T1□□	4.280 ±0.025 V	4.080 ±0.050 V	2.40 ±0.080 V	2.70 ±0.100 V	0.150 ±0.025 V	Unavailable
S-8253AAH-T8T1□□	4.350 ±0.025 V	4.150 ±0.050 V	2.30 ±0.080 V	2.30 ±0.080 V	0.090 ±0.025 V	Available

Table 2 S-8253B Series (For 3-Serial Cell)

Model No.	Overcharge detection voltage [V_{CU}]	Overcharge release voltage [V_{CL}]	Overdischarge detection voltage [V_{DL}]	Overdischarge release voltage [V_{DU}]	Overcurrent detection voltage 1 [V_{IOV1}]	0 V battery charge function
S-8253BAA-T8T1□□	4.350 ±0.025 V	4.050 ±0.050 V	2.40 ±0.080 V	2.70 ±0.100 V	0.300 ±0.025 V	Available
S-8253BAB-T8T1□□	4.325 ±0.025 V	4.075 ±0.050 V	2.20 ±0.080 V	2.90 ±0.100 V	0.200 ±0.025 V	Unavailable
S-8253BAC-T8T1□□	4.350 ±0.025 V	4.050 ±0.050 V	2.40 ±0.080 V	2.70 ±0.100 V	0.080 ±0.025 V	Available
S-8253BAD-T8T1□□	4.250 ±0.025 V	4.050 ±0.050 V	2.40 ±0.080 V	2.70 ±0.100 V	0.120 ±0.025 V	Available
S-8253BAE-T8T1□□	4.350 ±0.025 V	4.150 ±0.050 V	2.20 ±0.080 V	2.40 ±0.100 V	0.100 ±0.025 V	Available
S-8253BAF-T8T1□□	4.280 ±0.025 V	4.180 ±0.050 V	2.20 ±0.080 V	2.50 ±0.100 V	0.190 ±0.025 V	Unavailable
S-8253BAG-T8T1□□	4.280 ±0.025 V	4.180 ±0.050 V	2.20 ±0.080 V	2.50 ±0.100 V	0.125 ±0.025 V	Unavailable
S-8253BAH-T8T1□□	4.350 ±0.025 V	4.150 ±0.050 V	2.20 ±0.080 V	2.40 ±0.100 V	0.250 ±0.025 V	Available
S-8253BAI-T8T1□□	4.350 ±0.025 V	4.150 ±0.050 V	2.20 ±0.080 V	2.40 ±0.100 V	0.160 ±0.025 V	Available

Remark 1. Please contact the ABLIC Inc. marketing department for the products with the detection voltage value other than those specified above.
2. □□: GZ or U
3. Please select products of environmental code = U for Sn 100%, halogen-free products.

■ Pin Configuration

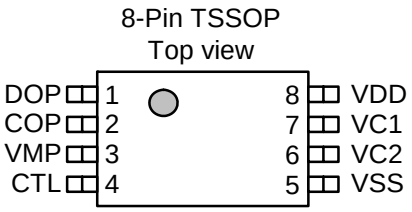


Figure 3

Table 3 S-8253A Series

Pin No.	Symbol	Description
1	DOP	Connection pin for discharge control FET gate (CMOS output)
2	COP	Connection pin for charge control FET gate (Nch open-drain output)
3	VMP	Pin for voltage detection between VDD and VMP (Detection pin for overcurrent)
4	CTL	Input pin for charge / discharge control signal, Pin for shortening test time (L : Normal operation, H : inhibit charge / discharge M ($V_{DD} \times 1 / 2$) : shorten test time)
5	VSS	Input pin for negative power supply, Connection pin for negative voltage of battery 2
6	VC2	No connection *1
7	VC1	Connection pin for negative voltage of battery 1, for positive voltage of battery 2
8	VDD	Input pin for positive power supply, Connection pin for positive voltage of battery 1

***1.** No connection is electrically open. This pin can be connected to VDD or VSS.

Remark Refer to the package drawings for the external views.

Table 4 S-8253B Series

Pin No.	Symbol	Description
1	DOP	Connection pin for discharge control FET gate (CMOS output)
2	COP	Connection pin for charge control FET gate (Nch open-drain output)
3	VMP	Pin for voltage detection between VDD and VMP (Detection pin for overcurrent)
4	CTL	Input pin for charge / discharge control signal, pin for shortening test time (L : Normal operation, H : inhibit charge / discharge, M ($V_{DD} \times 1 / 2$) : shorten test time)
5	VSS	Input pin for negative power supply, Connection pin for negative voltage of battery 3
6	VC2	Connection pin for negative voltage of battery 2, for positive voltage of battery 3
7	VC1	Connection pin for negative voltage of battery 1, for positive voltage of battery 2
8	VDD	Input pin for positive power supply, Connection pin for positive voltage of battery 1

Remark Refer to the package drawings for the external views.

■ Absolute Maximum Ratings

Table 5

(Ta = 25°C unless otherwise specified)

Item	Symbol	Applicable Pins	Absolute Maximum Ratings	Unit
Input voltage between VDD and VSS	V_{DS}	—	V_{SS} − 0.3 to V_{SS} + 26	V
Input pin voltage	V_{IN}	VC1, VC2	V_{SS} − 0.3 to V_{DD} + 0.3	V
VMP pin input voltage	V_{VMP}	VMP	V_{SS} − 0.3 to V_{SS} + 26	V
DOP pin output voltage	V_{DOP}	DOP	V_{SS} − 0.3 to V_{DD} + 0.3	V
COP pin output voltage	V_{COP}	COP	V_{SS} − 0.3 to V_{VMP} + 0.3	V
CTL input pin voltage	V_{IN_CTL}	CTL	V_{SS} − 0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	—	300 (When not mounted on board)	mW
			700[*1]	mW
Operating ambient temperature	T_{opr}	—	− 40 to + 85	°C
Storage temperature	T_{stg}	—	− 40 to + 125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

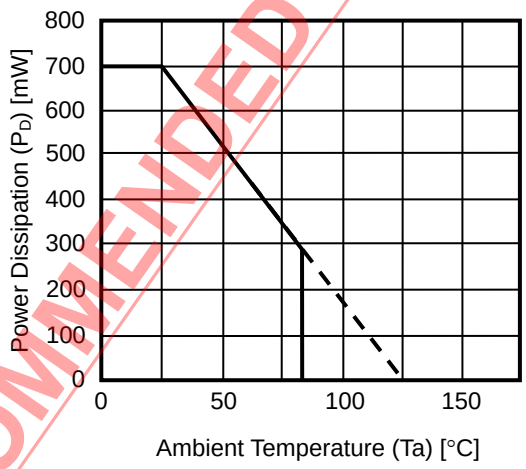


Figure 4 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

1. Except Detection Delay Time

Table 6 (1 / 2)

(Ta = 25°C unless otherwise specified)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test condi-tion	Test circuit
DETECTION VOLTAGE									
Overcharge detection voltage n	V_{CUn}	3.90 V to 4.40 V, Adjustable		V_{CUn} −0.025	V_{CUn}	V_{CUn} +0.025	V	1	1
Overcharge release voltage n	V_{CLn}	3.80 V to 4.40 V, Adjustable	$V_{CL} \neq V_{CU}$	V_{CLn} −0.05	V_{CLn}	V_{CLn} +0.05	V	1	1
			$V_{CL} = V_{CU}$	V_{CLn} −0.025	V_{CLn}	V_{CLn} +0.025	V	1	1
Overdischarge detection voltage n	V_{DLn}	2.0 V to 3.0 V, Adjustable		V_{DLn} −0.080	V_{DLn}	V_{DLn} +0.080	V	1	1
Overdischarge release voltage n	V_{DUn}	2.0 V to 3.40 V, Adjustable	$V_{DL} \neq V_{DU}$	V_{DUn} −0.10	V_{DUn}	V_{DUn} +0.10	V	1	1
			$V_{DL} = V_{DU}$	V_{DUn} −0.08	V_{DUn}	V_{DUn} +0.08	V	1	1
Overcurrent detection voltage 1	V_{IOV1}	0.05 V to 0.30 V, Adjustable Based on V_{DD}		V_{IOV1} −0.025	V_{IOV1}	V_{IOV1} +0.025	V	2	1
Overcurrent detection voltage 2	V_{IOV2}	Based on V_{DD}		0.40	0.50	0.60	V	2	1
Overcurrent detection voltage 3	V_{IOV3}	Based on V_{DD}		0.9	1.2	1.5	V	2	1
Temperature coefficient 1 *1	T_{COE1}	Ta = 0°C to 50°C*3		−1.0	0	1.0	mV / °C	—	—
Temperature coefficient 2 *2	T_{COE2}	Ta = 0°C to 50°C*3		−0.5	0	0.5	mV / °C	—	—
0 V BATTERY CHARGE FUNCTION									
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charging available		—	0.8	1.5	V	12	5
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charging unavailable		0.4	0.7	1.1	V	12	5
INTERNAL RESISTANCE									
Resistance between VMP and VDD	R_{VMD}	V1 = V2 = V3*4 = 3.5 V, $V_{VMP} = V_{SS}$		70	95	120	kΩ	6	2
Resistance between VMP and VSS	R_{VMS}	V1 = V2 = V3*4 = 1.8 V, $V_{VMP} = V_{DD}$		450	900	1800	kΩ	6	2

Table 6 (2 / 2)

(Ta = 25°C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test condi-tion	Test circuit
INPUT VOLTAGE								
Operating voltage between VDD and VSS	V_{DSOP}	Output voltage of DOP and COP fixed	2	—	24	V	—	—
CTL input voltage "H"	V_{CTLH}	—	V_{DD} –0.5	—	—	V	7	1
CTL input voltage "L"	V_{CTLL}	—	—	—	V_{SS} +0.5	V	7	1
INPUT CURRENT								
Current consumption on operation	I_{OPE}	V1 = V2 = V3*4 = 3.5 V	—	14	28	µA	5	2
Current consumption at power down	I_{PDN}	V1 = V2 = V3*4 = 1.5 V	—	—	0.1	µA	5	2
VC1 pin current	I_{VC1}	V1 = V2 = V3*4 = 3.5 V	–0.3	0	0.3	µA	9	3
VC2 pin current	I_{VC2}	V1 = V2 = V3*4 = 3.5 V	–0.3	0	0.3	µA	9	3
CTL pin current "H"	I_{CTLH}	V1 = V2 = V3*4 = 3.5 V, $V_{CTL1} = V_{DD}$	—	—	0.1	µA	8	3
CTL pin current "L"	I_{CTLL}	V1 = V2 = V3*4 = 3.5 V, $V_{CTL1} = V_{SS}$	–0.4	–0.2	—	µA	8	3
OUTPUT CURRENT								
COP pin leakage current	I_{COH}	V_{COP} = 24 V	—	—	0.1	µA	10	4
COP pin sink current	I_{COL}	$V_{COP} = V_{SS} + 0.5$ V	10	—	—	µA	10	4
DOP pin source current	I_{DOH}	$V_{DOP} = V_{DD} - 0.5$ V	10	—	—	µA	11	4
DOP pin sink current	I_{DOL}	$V_{DOP} = V_{SS} + 0.5$ V	10	—	—	µA	11	4

***1.** Voltage temperature coefficient 1 : Overcharge detection voltage

***2.** Voltage temperature coefficient 2 : Overcurrent detection voltage 1

***3.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

***4.** Because S-8253A Series are the protection ICs for 2-serial cell, there is no V3 for them.

2. Detection Delay Time

(1) S-8253AAA, S-8253AAB, S-8253AAC, S-8253AAD, S-8253AAE, S-8253AAF, S-8253AAG, S-8253BAA, S-8253BAC, S-8253BAD, S-8253BAE, S-8253BAH

Table 7

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = 25°C)								
Overcharge detection delay time	t_{CU}	—	0.92	1.15	1.38	s	3	1
Overdischarge detection delay time	t_{DL}	—	115	144	173	ms	3	1
Overcurrent detection delay time 1	t_{IOV1}	—	7.2	9	10.8	ms	4	1
Overcurrent detection delay time 2	t_{IOV2}	—	3.6	4.5	5.4	ms	4	1
Overcurrent detection delay time 3	t_{IOV3}	—	220	300	380	µs	4	1

(2) S-8253BAB, S-8253BAF, S-8253BAG, S-8253BAI

Table 8

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = 25°C)								
Overcharge detection delay time	t_{CU}	—	0.92	1.15	1.38	s	3	1
Overdischarge detection delay time	t_{DL}	—	115	144	173	ms	3	1
Overcurrent detection delay time 1	t_{IOV1}	—	3.6	4.5	5.4	ms	4	1
Overcurrent detection delay time 2	t_{IOV2}	—	0.89	1.1	1.4	ms	4	1
Overcurrent detection delay time 3	t_{IOV3}	—	220	300	380	µs	4	1

(3) S-8253AAH

Table 9

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DELAY TIME (Ta = 25°C)								
Overcharge detection delay time	t_{CU}	—	0.92	1.15	1.38	s	3	1
Overdischarge detection delay time	t_{DL}	—	115	144	173	ms	3	1
Overcurrent detection delay time 1	t_{IOV1}	—	14.5	18	22	ms	4	1
Overcurrent detection delay time 2	t_{IOV2}	—	3.6	4.5	5.4	ms	4	1
Overcurrent detection delay time 3	t_{IOV3}	—	220	300	380	µs	4	1

■ Test Circuits

1. Overcharge Detection Voltage 1, Overcharge Release Voltage 1, Overdischarge Detection Voltage 1, Overdischarge Release Voltage 1 (Test Condition 1, Test Circuit 1)

Confirm that V1 = V2 = 3.5 V (S-8253A Series), V1 = V2 = V3 = 3.5 V (S-8253B Series), V4 = 0 V, V5 = 0 V, and the COP and DOP pins are "L" (V_{DD} × 0.1 V or lower) (this status is referred to as the initial status).

1. 1 Overcharge Detection Voltage 1 (V_{CU1}), Overcharge Release Voltage 1 (V_{CL1})

Overcharge detection voltage 1 (V_{CU1}) is the voltage of V1 when the voltage of the COP pin is "H" (V_{DD} × 0.9 V or more) after the V1 voltage has been gradually increased starting at the initial status. Overcharge release voltage 1 (V_{CL1}) is the voltage of V1 when the voltage at the COP pin is low after the V1 voltage has been gradually decreased.

1. 2 Overdischarge Detection Voltage 1 (V_{DL1}), Overdischarge Release Voltage 1 (V_{DU1})

Overdischarge detection voltage 1 (V_{DL1}) is the voltage of V1 when the voltage of the DOP pin is high after the V1 voltage has been gradually decreased starting at the initial status. Overdischarge release voltage 1 (V_{DU1}) is the voltage of V1 when the voltage at the DOP pin is low after the V1 voltage has been gradually increased.

By changing Vn (n = 2: S-8253A Series, n = 2, 3: S-8253B Series) the overcharge detection voltage (V_{CUn}), overcharge release voltage (V_{CLn}), overdischarge detection voltage (V_{DLn}), and overdischarge release voltage (V_{DUn}) can be measured in the same way as when n = 1.

2. Overcurrent Detection Voltage 1, Overcurrent Detection Voltage 2, Overcurrent Detection Voltage 3 (Test Condition 2, Test Circuit 1)

Confirm that V1 = V2 = 3.5 V (S-8253A Series), V1 = V2 = V3 = 3.5 V (S-8253B Series), V4 = 0 V, V5 = 0 V, and the COP pin and DOP pin are low (this status is referred to as the initial status).

2. 1 Overcurrent Detection Voltage 1 (V_{IOV1})

Overcurrent detection voltage 1 (V_{IOV1}) is the voltage of V5 when the voltages of the COP pin and DOP pin are high after the V5 voltage has been gradually increased starting at the initial status.

2. 2 Overcurrent Detection Voltage 2 (V_{IOV2})

Overcurrent detection voltage 2 (V_{IOV2}) is the voltage of V5 when the voltages of the COP pin and DOP pin are high within the minimum and maximum values of overcurrent detection time 2 (t_{IOV2}) after the voltage of V5 was instantaneously increased (within 10 μs) starting at the initial status.

2. 3 Overcurrent Detection Voltage 3 (V_{IOV3})

Overcurrent detection voltage 3 (V_{IOV3}) is the voltage of V5 when the voltages of the COP pin and DOP pin are high within the minimum and maximum values of overcurrent detection time 3 (t_{IOV3}) after the voltage of V5 was instantaneously increased (within 10 μs) starting at the initial status.

3. Overcharge Detection Delay Time, Overdischarge Detection Delay Time (Test Condition 3, Test Circuit 1)

Confirm that V1 = V2 = 3.5 V (S-8253A Series), V1 = V2 = V3 = 3.5 V (S-8253B Series), V4 = 0 V, V5 = 0 V, and the COP pin and DOP pin are low (this status is referred to as the initial status).

3. 1 Overcharge Detection Delay Time (t_{CU})

The overcharge detection delay time (t_{CU}) is the time it takes for the voltage of the COP pin to change from low to high after the voltage of V1 is instantaneously changed from overcharge detection voltage 1 (V_{CU1}) − 0.2 V to overcharge detection voltage 1 (V_{CU1}) + 0.2 V (within 10 μs) starting at the initial status.

3. 2 Overdischarge Detection Delay Time (t_{DL})

The overdischarge detection delay time (t_{DL}) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of V1 is instantaneously changed from overdischarge detection voltage 1 (V_{DL1}) + 0.2 V to overdischarge detection voltage 1 (V_{DL1}) − 0.2 V (within 10 μs) starting at the initial status.

4. Overcurrent Detection Delay Time 1, Detection Delay Time 2, Detection Delay Time 3 (Test Condition 4, Test Circuit 1)

Confirm that V1 = V2 = 3.5 V (S-8253A Series), V1 = V2 = V3 = 3.5 V (S-8253B Series), V4 = 0 V, V5 = 0 V, and the COP pin and DOP pin are low (this status is referred to as the initial status).

4. 1 Overcurrent Detection Delay Time 1 (t_{IOV1})

Overcurrent detection delay time 1 (t_{IOV1}) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of V5 is instantaneously changed to 0.35 V (within 10 μs) starting at the initial status.

4. 2 Overcurrent Detection Delay Time 2 (t_{IOV2})

Overcurrent detection delay time 2 (t_{IOV2}) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of V5 is instantaneously changed to 0.7 V (within 10 μs) starting at the initial status.

4. 3 Overcurrent Detection Delay Time 3 (t_{IOV3})

Overcurrent detection delay time 3 (t_{IOV3}) is the time it takes for the voltage of the DOP pin to change from low to high after the voltage of V5 is instantaneously changed to 1.6 V (within 10 μs) starting at the initial status.

5. Consumption on Operation, Power Consumption at Power-down (Test Condition 5, Test Circuit 2)

5. 1 Power Consumption on Operation (I_{OPE})

The power consumption during operation (I_{OPE}) is the current of the VSS pin (I_{SS}) when V1 = V2 = 3.5 V (S-8253A Series), V1 = V2 = V3 = 3.5 V (S-8253B Series), S1 = ON, and S2 = OFF.

5. 2 Power Consumption at Power-down (I_{PDN})

The power consumption at power-down (I_{PDN}) is the current of the VSS pin (I_{SS}) when V1 = V2 = 1.5 V (S-8253A Series), V1 = V2 = V3 = 1.5 V (S-8253B Series), S1 = OFF, and S2 = ON.

6. Resistance between VMP and VDD, Resistance between VMP and VSS (Test Condition 6, Test Circuit 2)

Confirm that V1 = V2 = 3.5 V (S-8253A Series), V1 = V2 = V3 = 3.5 V (S-8253B Series), S1 = ON, and S2 = OFF (this status is referred to as the initial status).

6. 1 Resistance between VMP and VDD (R_{VMD})

The resistance between VMP and VDD (R_{VMD}) is determined based on the current of the VMP pin (I_{VMD}) after S1 and S2 are switched to OFF and ON, respectively, starting at the initial status.

S-8253A Series : $R_{VMD} = (V1 + V2) / I_{VMD}$
S-8253B Series : $R_{VMD} = (V1 + V2 + V3) / I_{VMD}$

6. 2 Resistance between VMP and VSS (R_{VMS})

The resistance between VMP and VSS (R_{VMS}) is determined based on the current of the VMP pin (I_{VMS}) after V1 = V2 = 1.8 V (S-8253A Series) or V1 = V2 = V3 = 1.8 V (S-8253B Series) are set starting at the initial status.

S-8253A Series : $R_{VMS} = (V1 + V2) / I_{VMS}$
S-8253B Series : $R_{VMS} = (V1 + V2 + V3) / I_{VMS}$

7. CTL Pin Input Voltage "H" (Test Condition 7, Test Circuit 1)

Confirm that V1 = V2 = 3.5 V (S-8253A Series), V1 = V2 = V3 = 3.5 V (S-8253B Series), V4 = 0 V, V5 = 0 V, and the COP pin and DOP pin are low (this status is referred to as the initial status).

7. 1 CTL Pin Input Voltage "H" (V_{CTLH})

The CTL pin input voltage "H" (V_{CTLH}) is the voltage of V4 when the voltages of the COP pin and DOP pin are high after the voltage of V4 has been gradually increased starting at the initial status.

8. CTL Pin Input Voltage "L" (Test condition 7, Test circuit 1)

Confirm that V1 = V2 = 3.5 V (S-8253A Series), V1 = V2 = V3 = 3.5 V (S-8253B Series), V4 = 0 V, V5 = 0.35 V, and the COP pin and DOP pin are high (this status is referred to as the initial status).

8. 1 CTL Pin Input Voltage "L" (V_{CTLL})

The CTL pin input voltage "L" (V_{CTLL}) is the voltage of V4 when the voltages of the COP pin and DOP pin are low after the voltage of V4 has been gradually increased starting at the initial status.

9. CTL Pin Current "H", CTL Pin Current "L" (Test Condition 8, Test Circuit 3)

9. 1 CTL Pin Current "H" (I_{CTLH}), CTL Pin Current "L" (I_{CTLL})

The CTL pin current "H" (I_{CTLH}) is the current that flows through the CTL pin when V1 = V2 = 3.5 V (S-8253A Series), V1 = V2 = V3 = 3.5 V (S-8253B Series), and S3 = ON, S4 = OFF. The CTL current "L" (I_{CTLL}) is the current that flows through the CTL pin when S3 = OFF and S4 = ON after that.

10. VC1 Pin Current, VC2 Pin Current (Test Condition 9, Test Circuit 3)

10. 1 VC1 Pin Current (I_{VC1}), VC2 Pin Current (I_{VC2})

The VC1 pin current (I_{VC1}) is the current that flows through the VC1 pin when V1 = V2 = 3.5 V (S-8253A Series), V1 = V2 = V3 = 3.5 V (S-8253B Series), and S3 = OFF, S4 = ON. Similarly, the VC2 pin current (I_{VC2}) is the current that flows through the VC2 pin under these conditions (S-8253B Series only).

11. COP Pin Leakage Current, COP Pin Sink Current (Test Condition 10, Test Circuit 4)

11. 1 COP Pin Leakage Current (I_{COH})

The COP pin leakage current (I_{COH}) is the current that flows through the COP pin when V1 = V2 = 12 V (S-8253A Series), V1 = V2 = V3 = 8 V (S-8253B Series), S6 = S7 = S8 = OFF, and S5 = ON.

11. 2 COP Pin Sink Current (I_{COL})

The COP pin sink current (I_{COL}) is the current that flows through the COP pin when V1 = V2 = 3.5 V (S-8253A Series), V1 = V2 = V3 = 3.5 V (S-8253B Series), V6 = 0.5 V, S5 = S7 = S8 = OFF, and S6 = ON.

12. DOP Pin Source Current, DOP Pin Sink Current (Test Condition 11, Test Circuit 4)

12. 1 DOP Pin Source Current (I_{DOH})

The DOP pin source current (I_{DOH}) is the current that flows through the DOP pin when V1 = V2 = 1.8 V (S-8253A Series), V1 = V2 = V3 = 1.8 V (S-8253B Series), V7 = 0.5 V, S5 = S6 = S8 = OFF, and S7 = ON.

12. 2 DOP Pin Sink Current (I_{DOL})

The DOP pin sink current (I_{DOL}) is the current that flows through the DOP pin when V1 = V2 = 3.5 V (S-8253A Series), V1 = V2 = V3 = 3.5 V (S-8253B Series), V8 = 0.5 V, S5 = S6 = S7 = OFF, and S8 = ON.

13. 0 V Battery Charge Starting Battery Charger Voltage (Product with 0 V Battery Charge Function), 0 V Battery Charge Inhibition Battery Voltage (Product with 0 V Battery Charge Inhibition Function) (Test Condition 12, Test Circuit 5)

13. 1 0 V Battery Charge Starting Battery Charger Voltage (V_{0CHA}) (Product with 0 V Battery Charge Function)

The COP pin voltage should be lower than V_{0CHA} max. − 1 V when V1 = V2 = 0 V (S-8253A Series), V1 = V2 = V3 = 0 V (S-8253B Series), and V9 = V_{VMP} = V_{0CHA} max.

13. 2 0 V Battery Charge Inhibition Battery Voltage (V_{0INH}) (Product with 0 V Battery Charge Inhibition Function)

The COP pin voltage should be higher than V_{VMP} − 1 V when V1 = V2 = V_{0INH} min. (S-8253A Series), V1 = V2 = V3 = V_{0INH} min. (S-8253B Series), and V9 = V_{VMP} = 24 V.

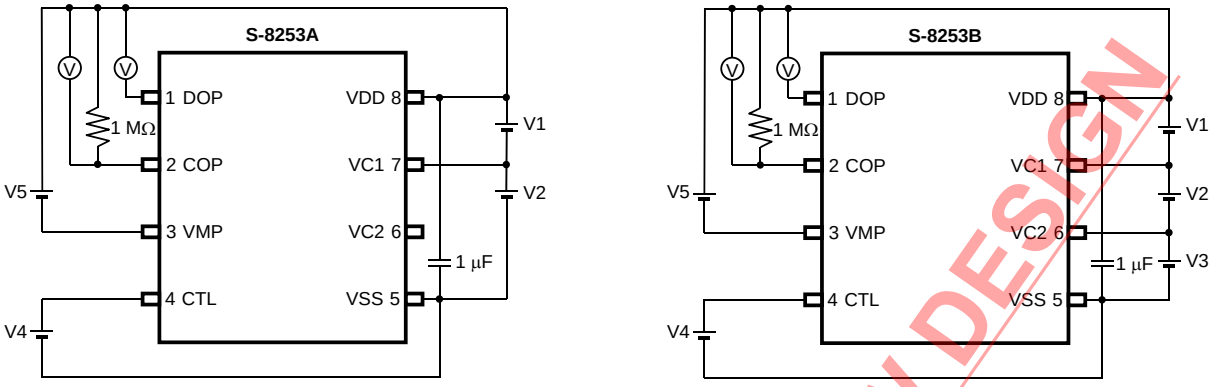


Figure 5 Test Circuit 1

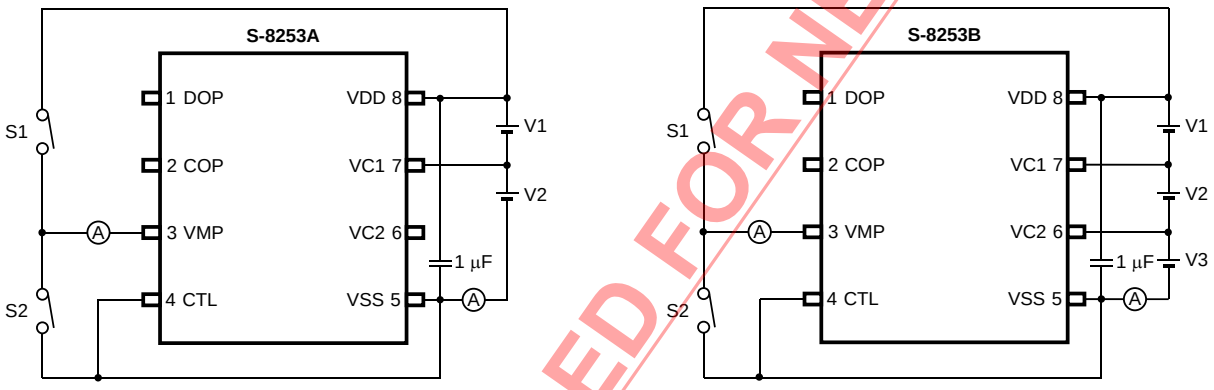


Figure 6 Test Circuit 2

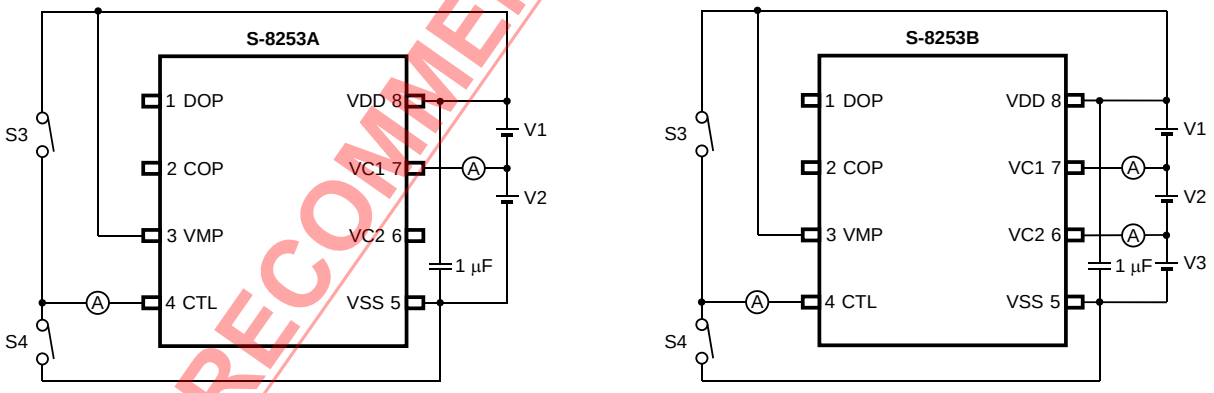


Figure 7 Test Circuit 3

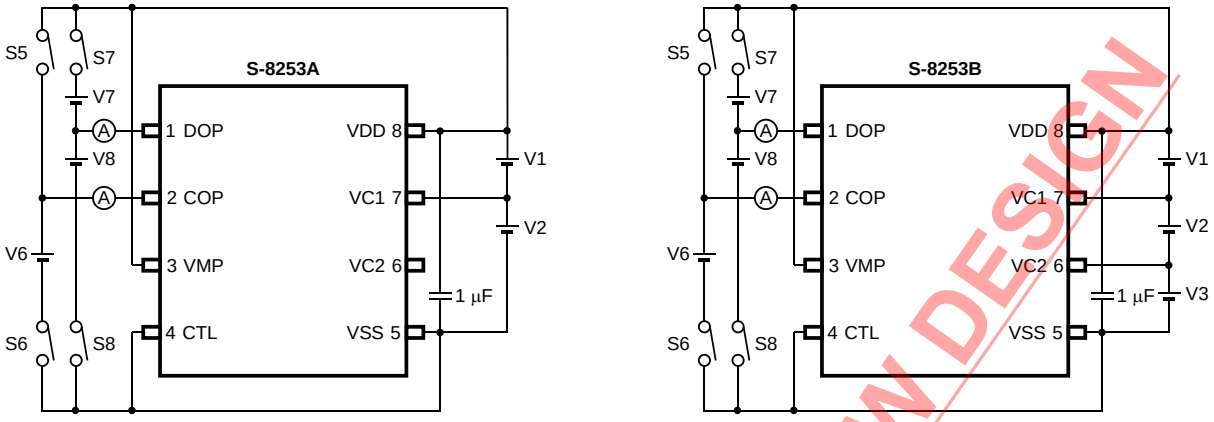


Figure 8 Test Circuit 4

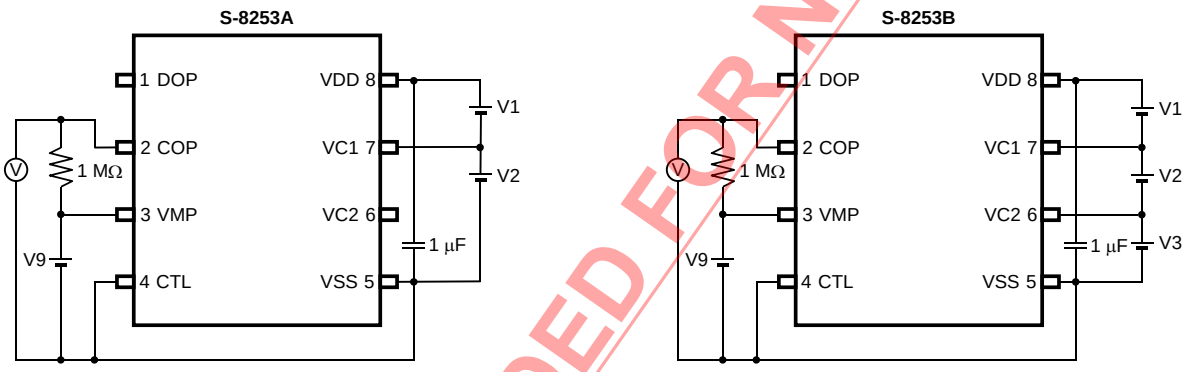


Figure 9 Test Circuit 5

■ Operation

Remark Refer to "■ **Battery Protection IC Connection Example**".

1. Normal Status

When all of the battery voltages are in the range from V_{DLn} to V_{CUn} and the discharge current is lower than the specified value (the VMP pin voltage is higher than $V_{DD} - V_{IOV1}$), the charging and discharging FETs are turned on. This condition is called the normal status, and in this condition charging and discharging can be carried out freely.

Caution When the battery is connected for the first time, discharging may not be enabled. In this case, short the VMP pin and VDD pin or connect the charger to restore the normal status.

2. Overcharge Status

When any one of the battery voltages becomes higher than V_{CUn} and the state continues for t_{CU} or longer, the COP pin becomes high impedance. Because the COP pin is pulled up to the EB+ pin voltage by an external resistor, the charging FET is turned off to stop charging. This is called the overcharge status. The overcharge status is released when one of the following two conditions holds.

(1) All battery voltages become V_{CLn} or lower.
(2) All of the battery voltages are V_{CUn} or lower, and the VMP pin voltage is $V_{DD} - V_{IOV1}$ or lower (since the discharge current flows through the body diode of the charging FET immediately after discharging is started when the charger is removed and a load is connected, the VMP pin voltage momentarily decreases by approximately 0.6 V from the VDD pin voltage. The IC detects this voltage and releases the overcharging status).

3. Overdischarge Status

When any one of the battery voltages becomes lower than V_{DLn} and the state continues for t_{DL} or longer, the DOP pin voltage becomes V_{DD} level, and the discharging FET is turned off to stop discharging. This is called the overdischarging status. After discharging is stopped due to the overdischarge status, the S-8253A/B Series enters the power-down status.

4. Power-down Status

When discharging has stopped due to the overdischarge status, the VMP pin is pulled down to the V_{SS} level by the R_{VMS} resistor. When the VMP pin voltage is lower than Typ. 0.8 V, the S-8253A/B Series enters the power-down status. In the power-down status, almost all the circuits of the S-8253A/B Series stop and the current consumption is I_{PDN} or lower. The conditions of each output pin are as follows.

(1) COP pin : High-Z
(2) DOP pin : V_{DD}

The power-down status is released when the following condition holds.

(1) The VMP pin voltage is Typ. 0.8 V or higher.

The overdischarging status is released when the following two conditions hold.

(1) All battery voltage is released at V_{DUn} or higher when the VMP pin voltage is Typ. 0.8 V or higher and the VMP pin voltage is lower than V_{DD}.
(2) All battery voltage is released at V_{DLn} or higher when the VMP pin voltage is Typ. 0.8 V or higher and the VMP pin voltage is V_{DD} or higher (when a charger is connected and VMP pin voltage is V_{DD} or higher, overdischarge hysteresis is released and electric discharge control FET is turned on at V_{DLn}).

5. Overcurrent Status

The S-8253A/B Series has three overcurrent detection levels (V_{IOV1}, V_{IOV2}, and V_{IOV3}) and three overcurrent detection delay times (t_{IOV1}, t_{IOV2}, and t_{IOV3}) corresponding to each overcurrent detection level. When the discharging current becomes higher than the specified value (the difference of the voltages of the VMP pin and VDD pin is greater than V_{IOV1}) and the state continues for t_{IOV1} or longer, the S-8253A/B Series enters the overcurrent status, in which the DOP pin voltage becomes V_{DD} level to turn off the discharging FET to stop discharging, the COP pin becomes high impedance and is pulled up to the EB+ pin voltage to turn off the charging FET to stop charging, and the VMP pin is pulled up to the V_{DD} voltage by the internal resistor (R_{VMD}). Operation of overcurrent detection levels 2, 3 (V_{IOV2}, V_{IOV3}) and overcurrent detection delay times 2, 3 (t_{IOV2}, t_{IOV3}) are the same as for V_{IOV1} and t_{IOV1}.

The overcurrent status is released when the following condition holds.

(1) The VMP pin voltage is $V_{DD} - V_{IOV1}$ or higher because a charger is connected or the load is released.

Caution The impedance that enables automatic restoration varies depending on the battery voltage and set value of overcurrent detection voltage 1.

6. 0 V Battery Charge Function

Regarding the charging of a self-discharged battery (0 V battery), the S-8253A/B Series has two functions from which one should be selected.

(1) 0 V battery charging is allowed (0 V battery charging is available.)
When the charger voltage is higher than V_{0CHA}, the 0 V battery can be charged.

(2) 0 V battery charging is prohibited (0 V battery charging is unavailable.)
When one of the battery voltages is lower than V_{0INH}, the 0 V battery cannot be charged.

Caution When the VDD pin voltage is lower than the minimum value of V_{DSOP}, the operation of the S-8253A/B Series is not guaranteed.

7. Delay Circuit

The following detection delay times are determined by dividing a clock of approximately 3.57 kHz by the counter.

(Example) Oscillator clock cycle (T_{CLK}) : 280 µs
Overcharge detection delay time (t_{CU}) : 1.15 s
Overdischarge detection delay time (t_{DL}) : 144 ms
Overcurrent detection delay time 1 (t_{IOV1}) : 9 ms
Overcurrent detection delay time 2 (t_{IOV2}) : 4.5 ms

Remark The overcurrent detection delay time 2 (t_{IOV2}) and overcurrent detection delay time 3 (t_{IOV3}) start when the overcurrent detection voltage 1 (V_{IOV1}) is detected. As soon as the overcurrent detection voltage 2 (V_{IOV2}) or overcurrent detection voltage 3 (V_{IOV3}) is detected over the detection delay time for overcurrent 2 (t_{IOV2}) or overcurrent 3 (t_{IOV3}) after the detection of overcurrent 1 (V_{IOV1}), the S-8253A/B turns the discharging control FET off within t_{IOV2} or t_{IOV3} of each detection.

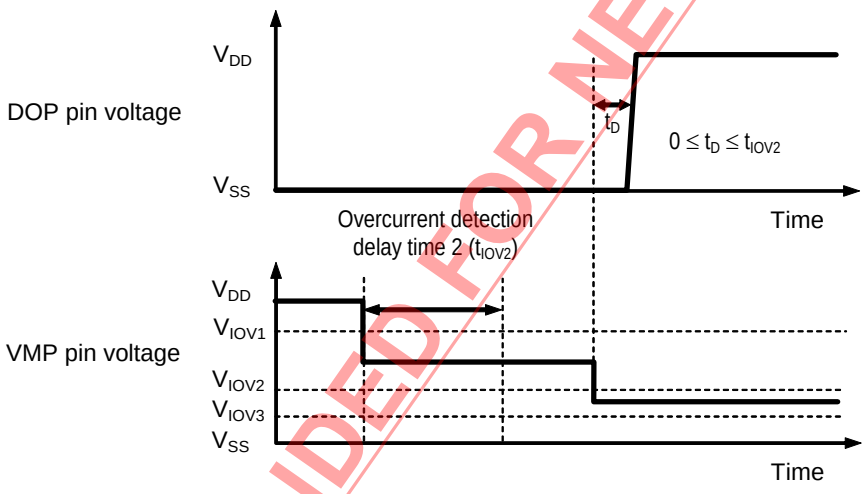


Figure 10

8. CTL Pin

The S-8253A/B Series has a control pin for charge / discharge control and shortening the test time. The levels, "L", "H", and "M", of the voltage input to the CTL pin determine the status of the S-8253A/B Series: normal operation, charge / discharge inhibition, or test time shortening. The CTL pin takes precedence over the battery protection circuit. During normal use, short the CTL pin and VSS pin.

Table 10 Conditions Set by CTL Pin

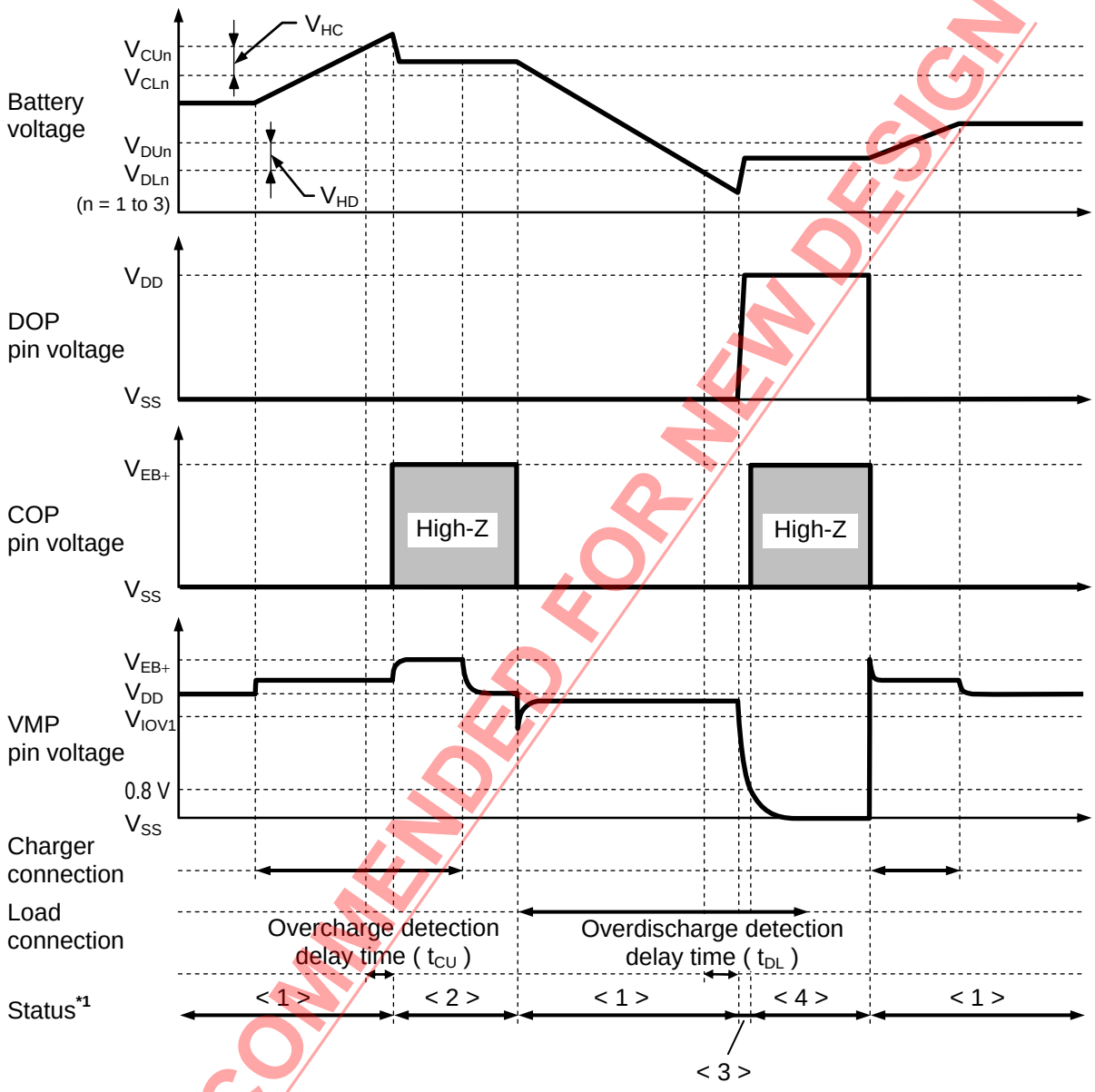
CTL Pin Potential	Status of IC	COP Pin	DOP Pin
Open	Charge / discharge inhibited status	High-Z	V_{DD}
High ($V_{CTL} \geq V_{CTLH}$)	Charge / discharge inhibited status	High-Z	V_{DD}
Middle ($V_{CTLL} < V_{CTL} < V_{CTLH}$)	Delay time-shortening status *1	(*2)	(*2)
Low ($V_{CTLL} \geq V_{CTL}$)	Normal status	(*2)	(*2)

***1.** In this status, delay times are shortened in 1 / 60 to 1 / 30 scale.
***2.** The pin status is controlled by the voltage detection circuit.

Caution 1. If the potential of the CTL pin is middle, overcurrent detection voltage 1 (V_{IOV1}) does not operate.
2. If you use the middle potential of the CTL pin, contact ABLIC Inc. marketing department.
3. Please note unexpected behavior might occur when electrical potential difference between the CTL pin ("L" level) and VSS is generated through the external filter (R_{VSS} and C_{VSS}) as a result of input voltage fluctuations.

■ Timing Chart

1. Overcharge Detection and Overdischarge Detection

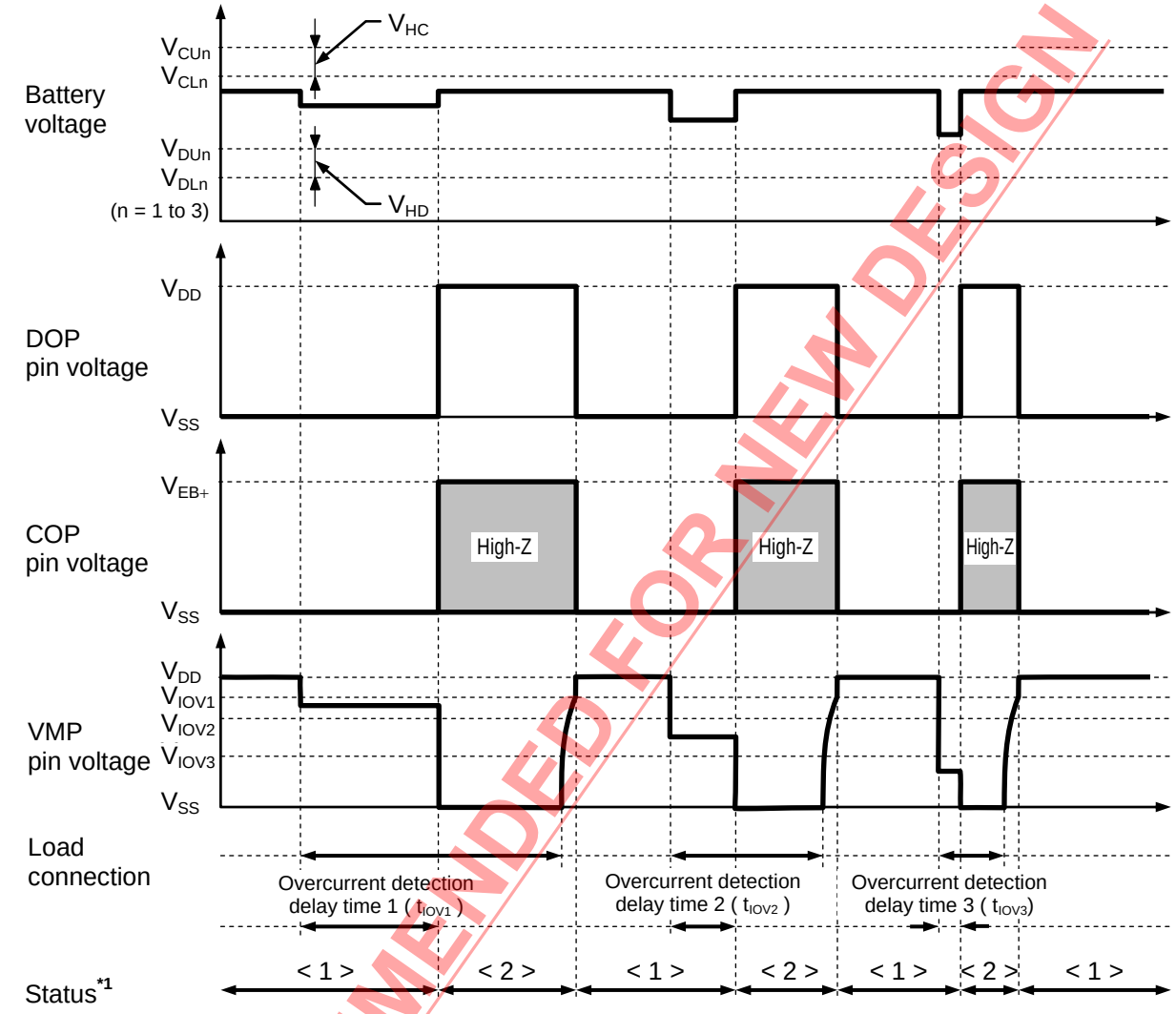


***1.** < 1 > : Normal status
< 2 > : Overcharge status
< 3 > : Overdischarge status
< 4 > : Power-down status

Remark The charger is assumed to charge with a constant current. V_{EB+} indicates the open voltage of the charger.

Figure 11

2. Overcurrent Detection



***1.** < 1 > : Normal status
< 2 > : Overcurrent status

Remark The charger is assumed to charge with a constant current. V_{EB+} indicates the open voltage of the charger.

Figure 12

■ Battery Protection IC Connection Example

1. S-8253A Series

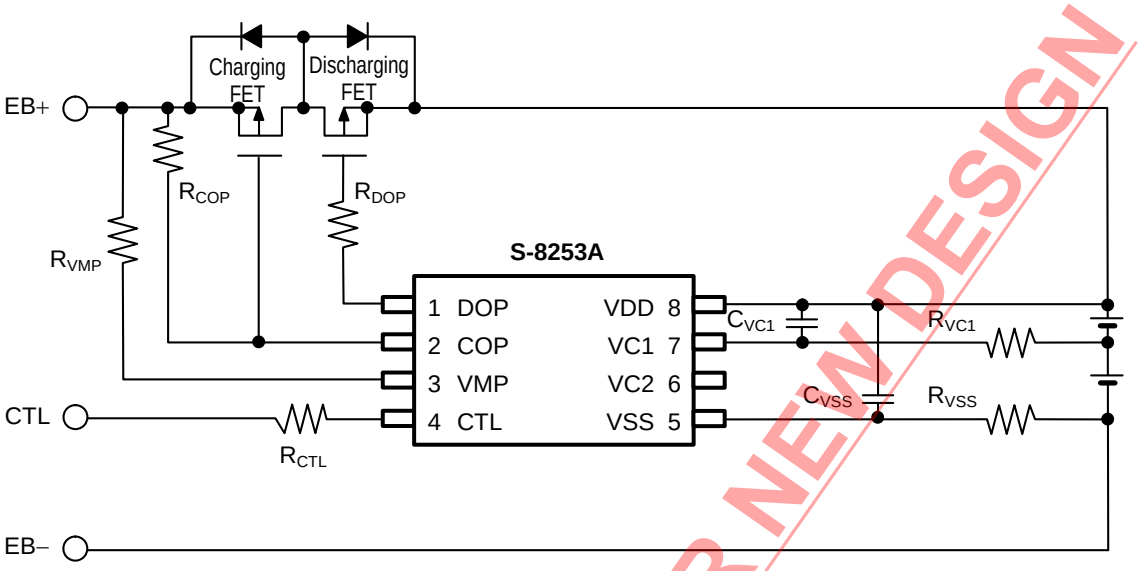


Figure 13

2. S-8253B Series

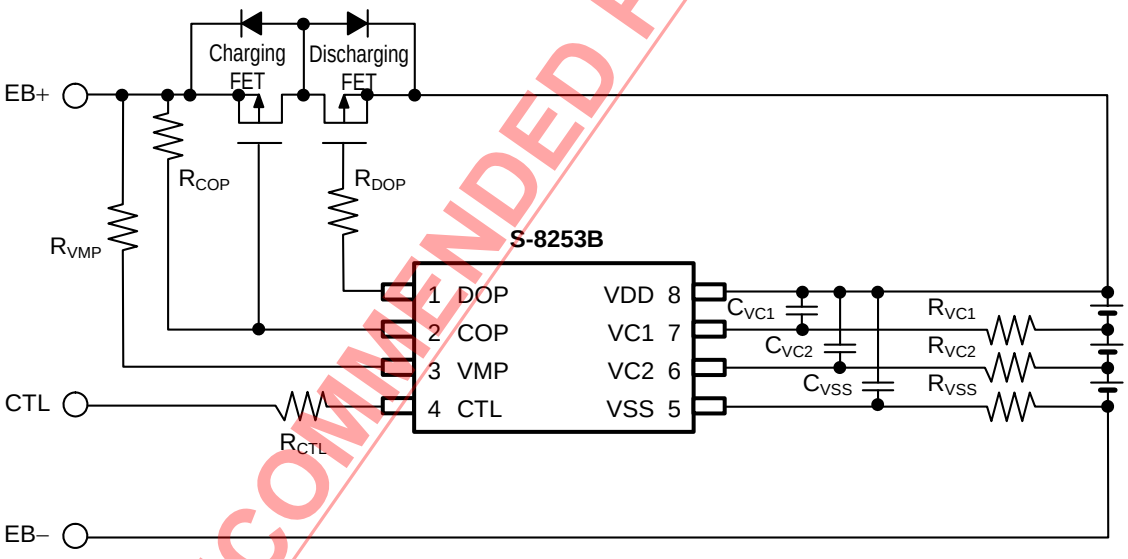


Figure 14

Table 11 Constants for External Components

No.	Symbol	Typ.	Range	Unit
1	R_{VC1}	1	0.51 to 1*1	kΩ
2	R_{VC2}	1	0.51 to 1*1	kΩ
3	R_{DOP}	5.1	2 to 10	kΩ
4	R_{COP}	1	0.1 to 1	MΩ
5	R_{VMP}	5.1	1 to 10	kΩ
6	R_{CTL}	1	1 to 100	kΩ
7	R_{VSS}	51	5.1 to 51*1	Ω
8	C_{VC1}	0.1	0.1 to 0.47*1	μF
9	C_{VC2}	0.1	0.1 to 0.47*1	μF
10	C_{VSS}	2.2	1 to 10*1	μF

***1.** Please set up a filter constant to be $R_{VSS} \times C_{VSS} \geq 51\ \mu F \bullet \Omega$ and to be $R_{VC1} \times C_{VC1} = R_{VC2} \times C_{VC2} = R_{VSS} \times C_{VSS}$.

Caution 1. The above constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform through evaluation using the actual application to set the constant.

■ Precautions

- In case of designing a circuit by using the CTL pin, as seen in **Figure 15**, note that discharging may stop during connecting a battery pack and the device.

Remark If you are cautious about this condition, please consider to use the S-8253C/D Series.

[Cause]

This is because the overcurrent detection voltage 3 (V_{IOV3}) is detected due to the rush current which flows into the device while a battery pack is in the delay time-shortening status.

[Mechanism]

As seen in **Figure 15**, before a battery pack is connected to the device, the battery pack may be in the charge / discharge inhibited status in which the CTL pin is internally pulled-up. From this status, if connecting the battery pack to the device, the CTL pin will be pulled-down in a time-constant C1 × (R1 + R_{PD}) by a pull-down resistor in the device. If the CTL's potential reaches V_{CTLL}<V_{CTL}<V_{CTLH}, the battery pack goes in the delay time-shortening status so that it releases charging and discharging, hence it starts charging a parasitic capacitor in the device. In this case, if the rush current, which makes the S-8253A/B Series to detect the overcurrent detection voltage 3 (V_{IOV3}), flows into the device, the overcurrent detection delay time 3 (t_{IOV3} = 300 µs typ.) will be shortened. So that the battery pack goes in the overcurrent status in several 10 µs. However, the battery pack goes in the normal status by connecting the device to the charger.

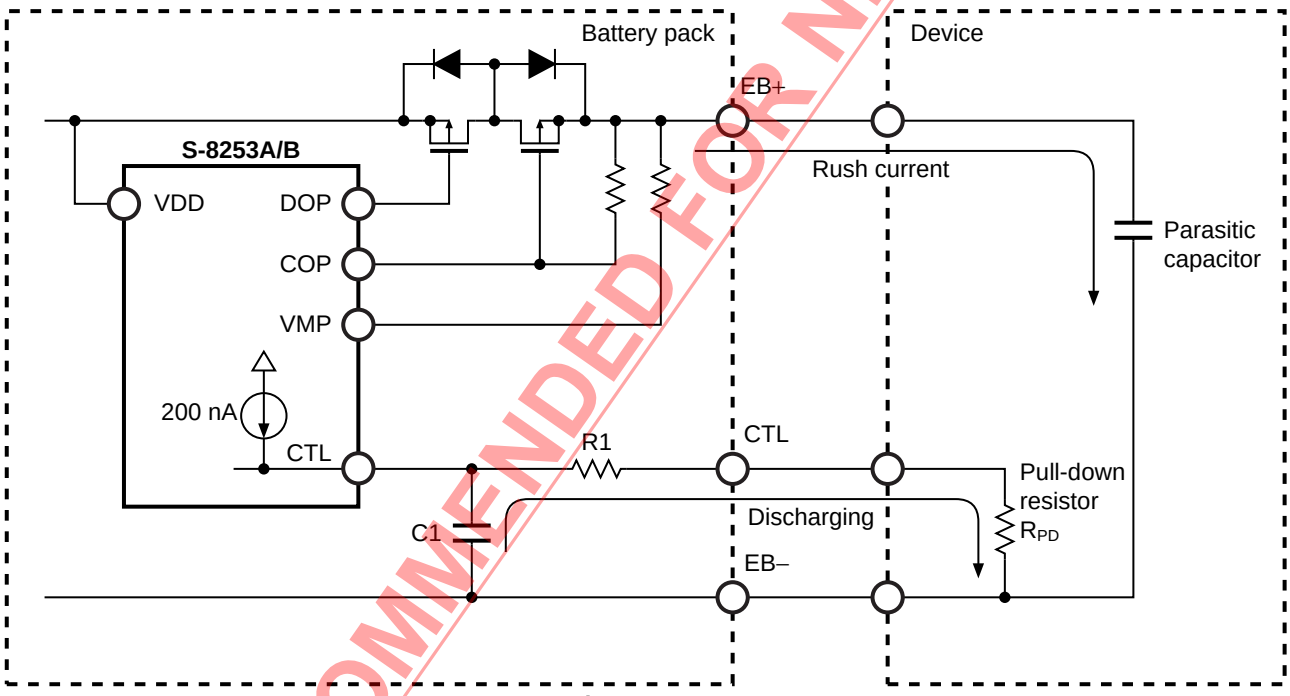


Figure 15

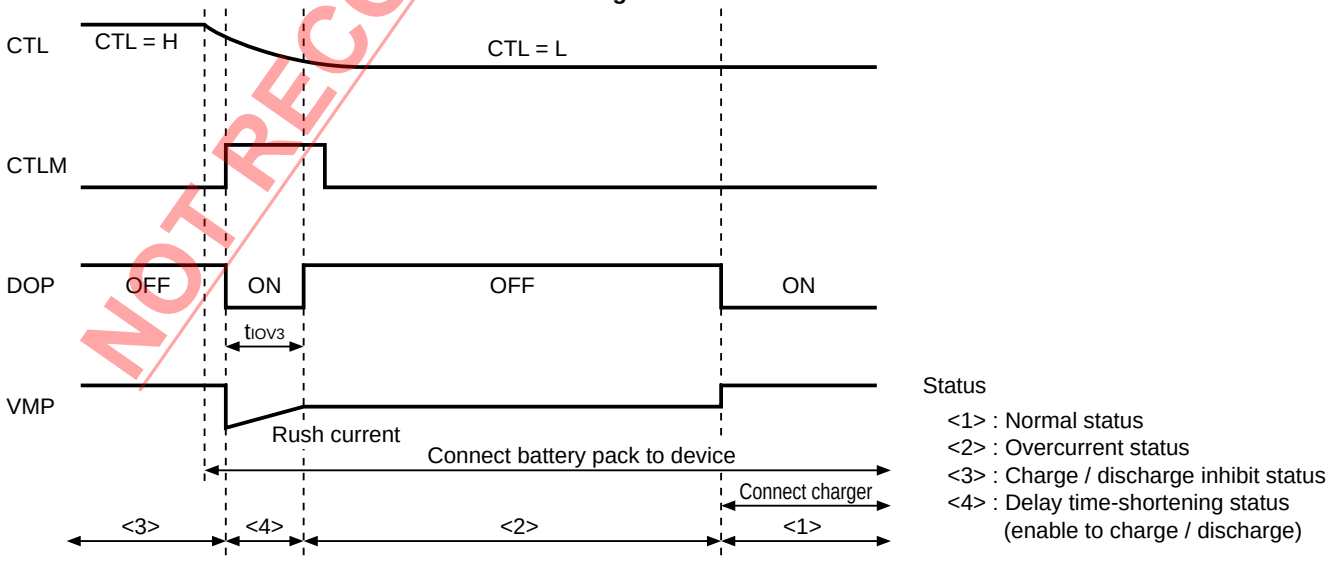


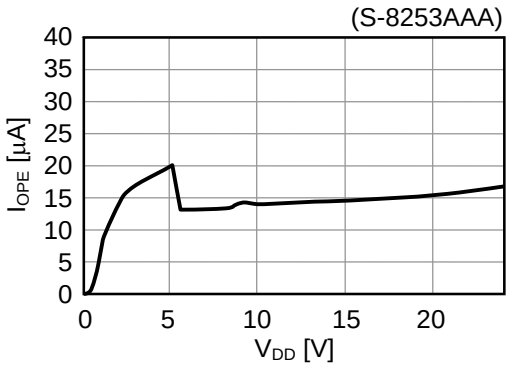
Figure 16

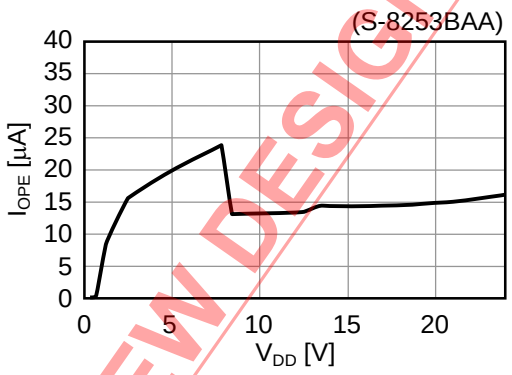
- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Batteries can be connected in any order, however, there may be cases when discharging cannot be performed when a battery is connected. In this case, short the VMP pin and VDD pin or connect the battery charger to return to the normal mode.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

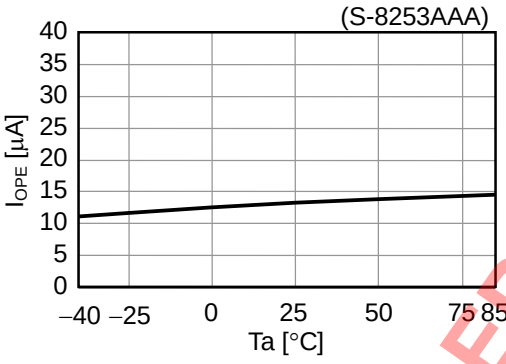
1. Current Consumption

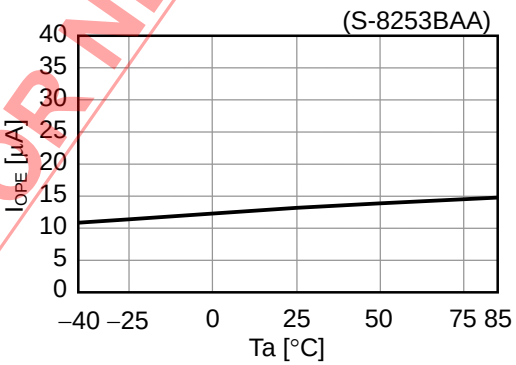
1. 1 I_{OPE} vs. V_{DD}



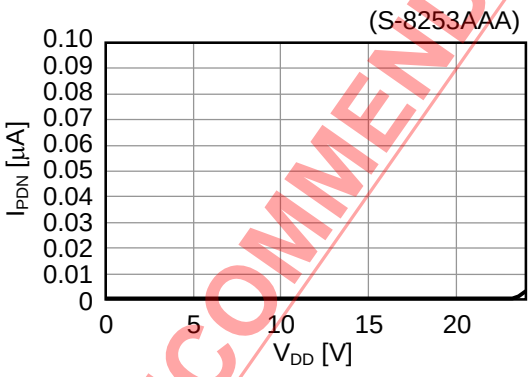


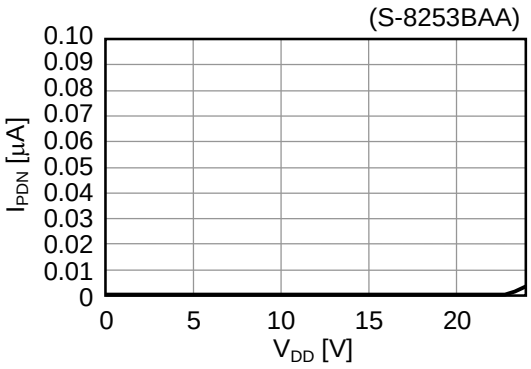
1. 2 I_{OPE} vs. Ta



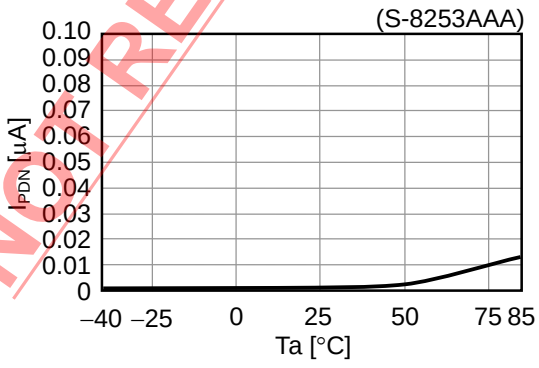


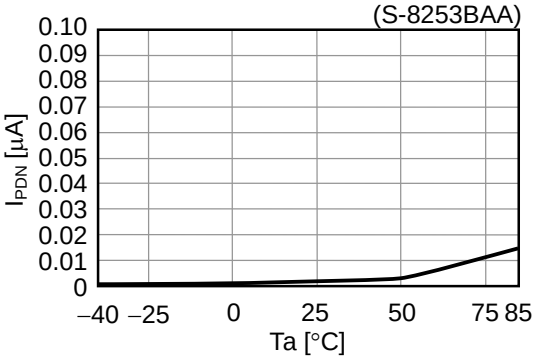
1. 3 I_{PDN} vs. V_{DD}





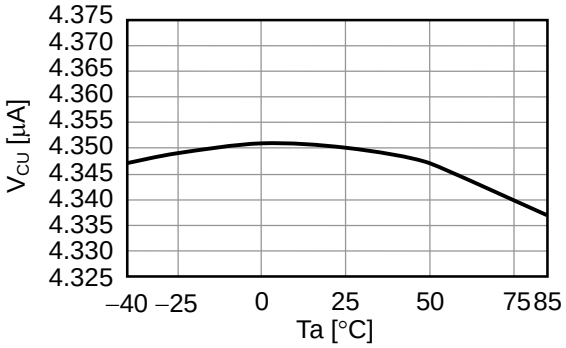
1. 4 I_{PDN} vs. Ta



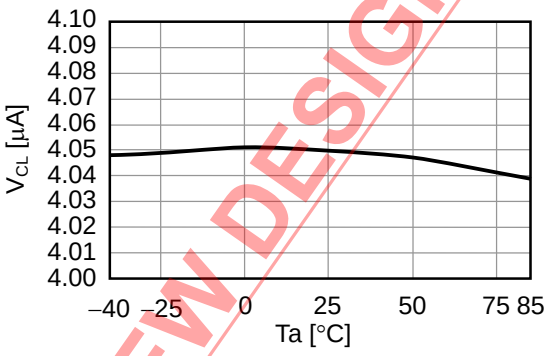


2. Overcharge Detection / Release Voltage, Overdischarge Detection / Release Voltage, Overcurrent Detection Voltage, and Delay Times (S-8253AAA, S-8253BAA)

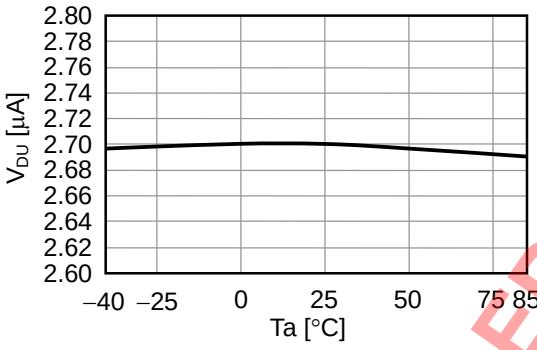
2. 1 V_{CU} vs. Ta



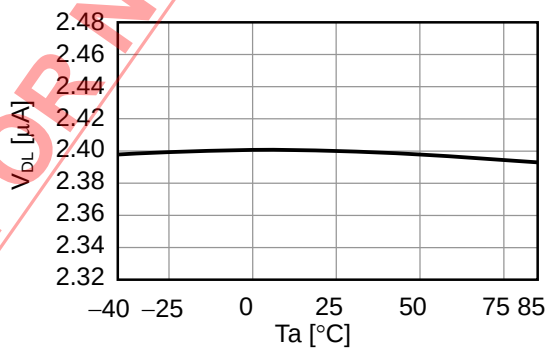
2. 2 V_{CL} vs. Ta



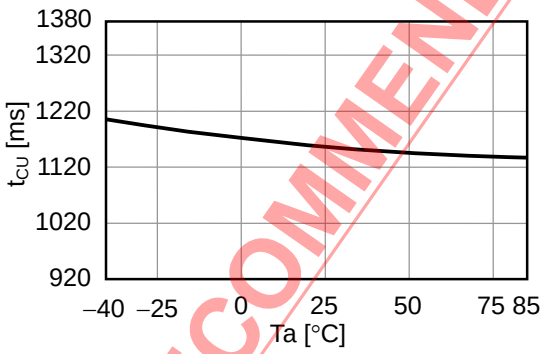
2. 3 V_{DU} vs. Ta



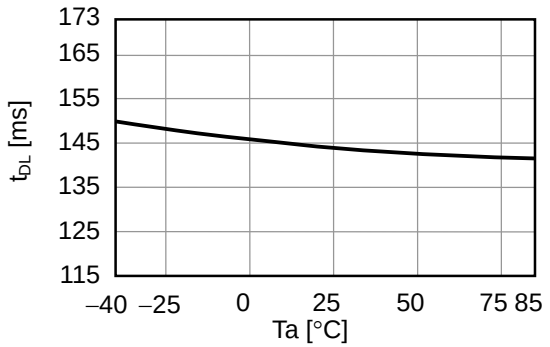
2. 4 V_{DL} vs. Ta



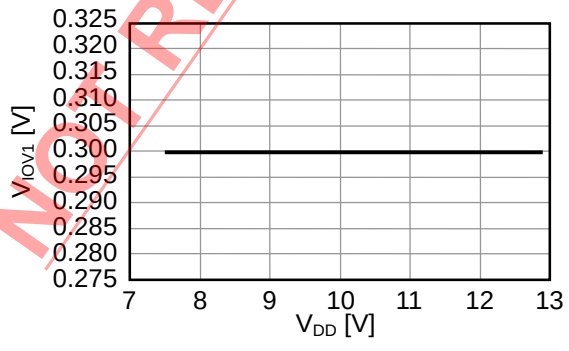
2. 5 t_{CU} vs. Ta



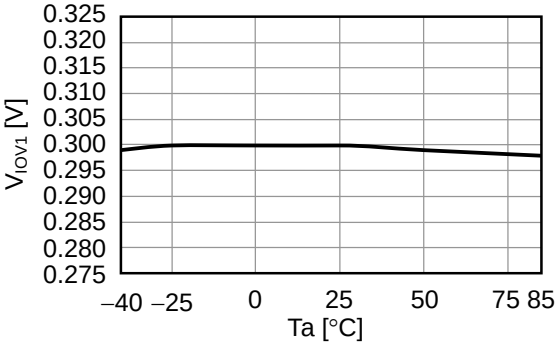
2. 6 t_{DL} vs. Ta



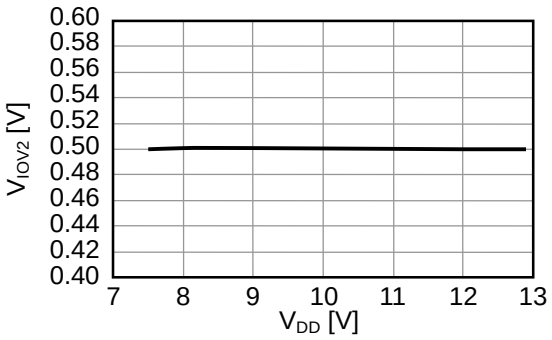
2. 7 V_{IOV1} vs. V_{DD}



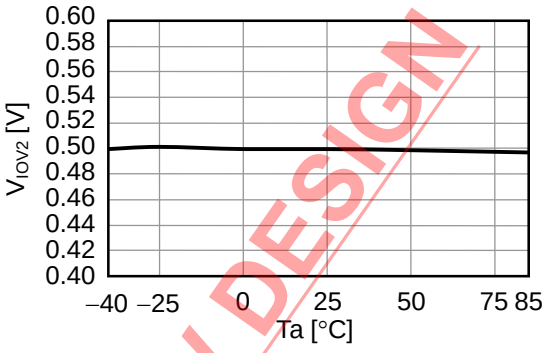
2. 8 V_{IOV1} vs. Ta



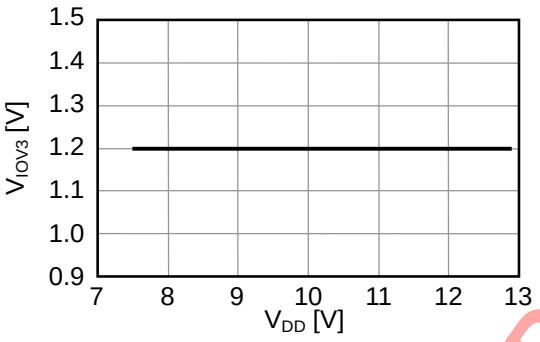
2. 9 V_{IOV2} vs. V_{DD}



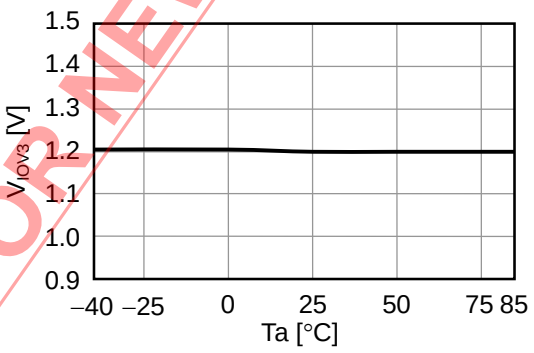
2. 10 V_{IOV2} vs. Ta



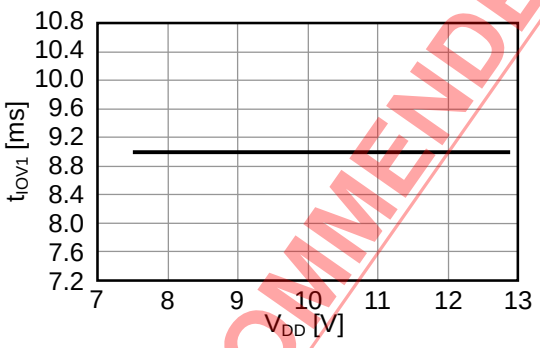
2. 11 V_{IOV3} vs. V_{DD}



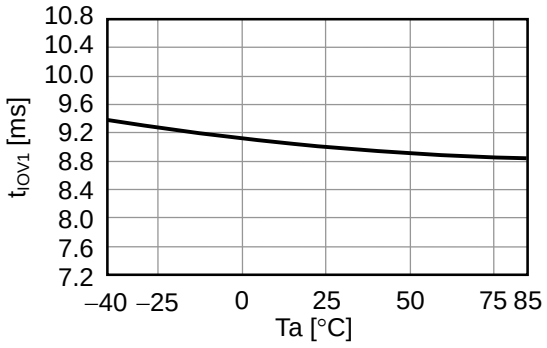
2. 12 V_{IOV3} vs. Ta



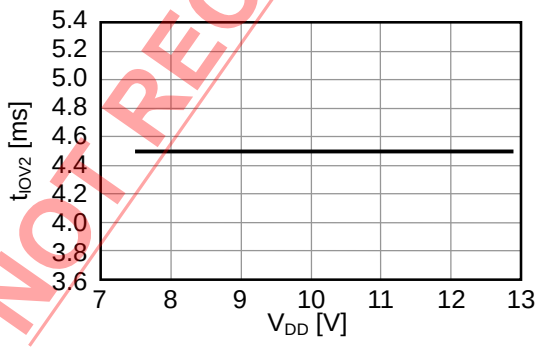
2. 13 t_{IOV1} vs. V_{DD}



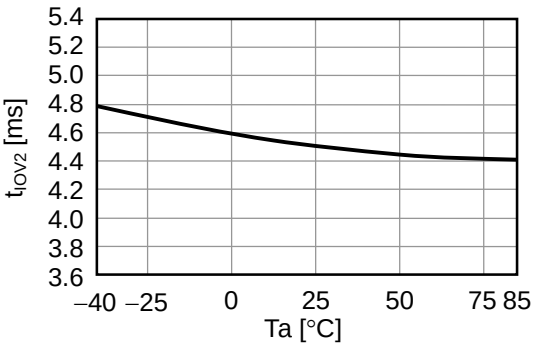
2. 14 t_{IOV1} vs. Ta



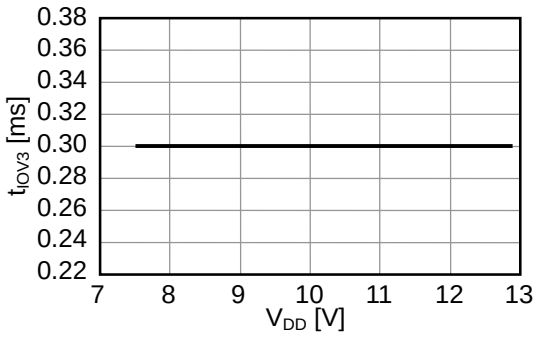
2. 15 t_{IOV2} vs. V_{DD}



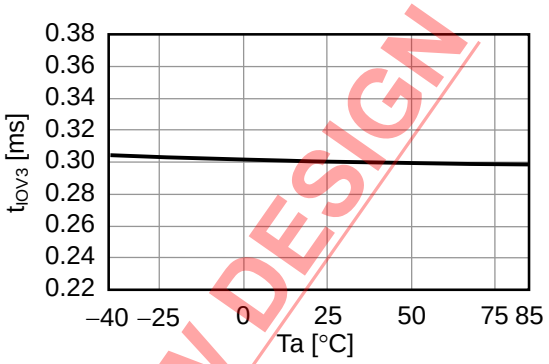
2. 16 t_{IOV2} vs. Ta



2. 17 t_{IOV3} vs. V_{DD}

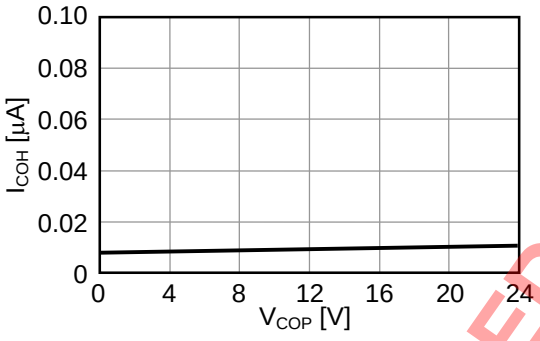


2. 18 t_{IOV3} vs. Ta

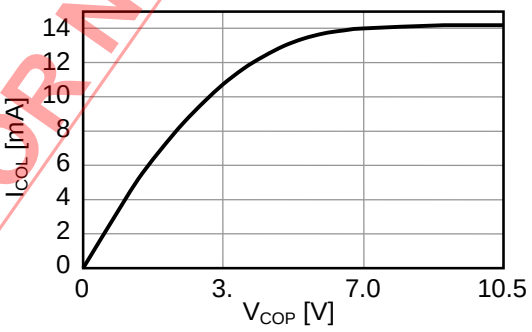


3. COP / DOP Pin (S-8253AAA, S-8253BAA)

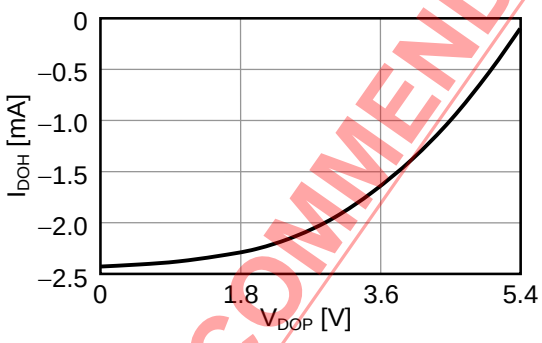
3. 1 I_{COH} vs. V_{COP}



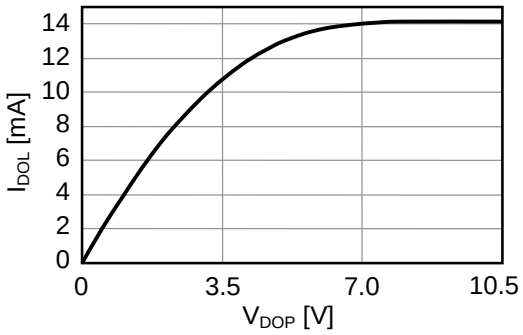
3. 2 I_{COL} vs. V_{COP}

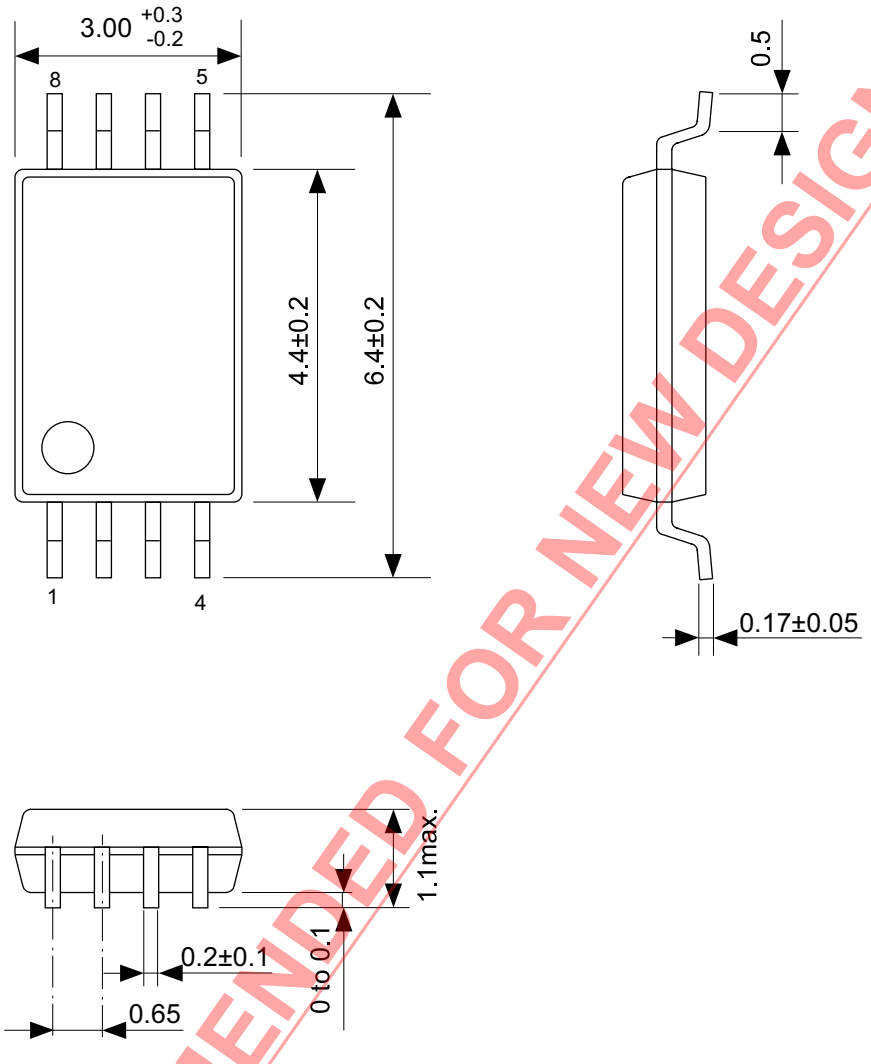


3. 3 I_{DOH} vs. V_{DOP}



3. 4 I_{DOL} vs. V_{DOP}





No. FT008-A-P-SD-1.2

TITLE	TSSOP8-E-PKG Dimensions
No.	FT008-A-P-SD-1.2
ANGLE	
UNIT	mm

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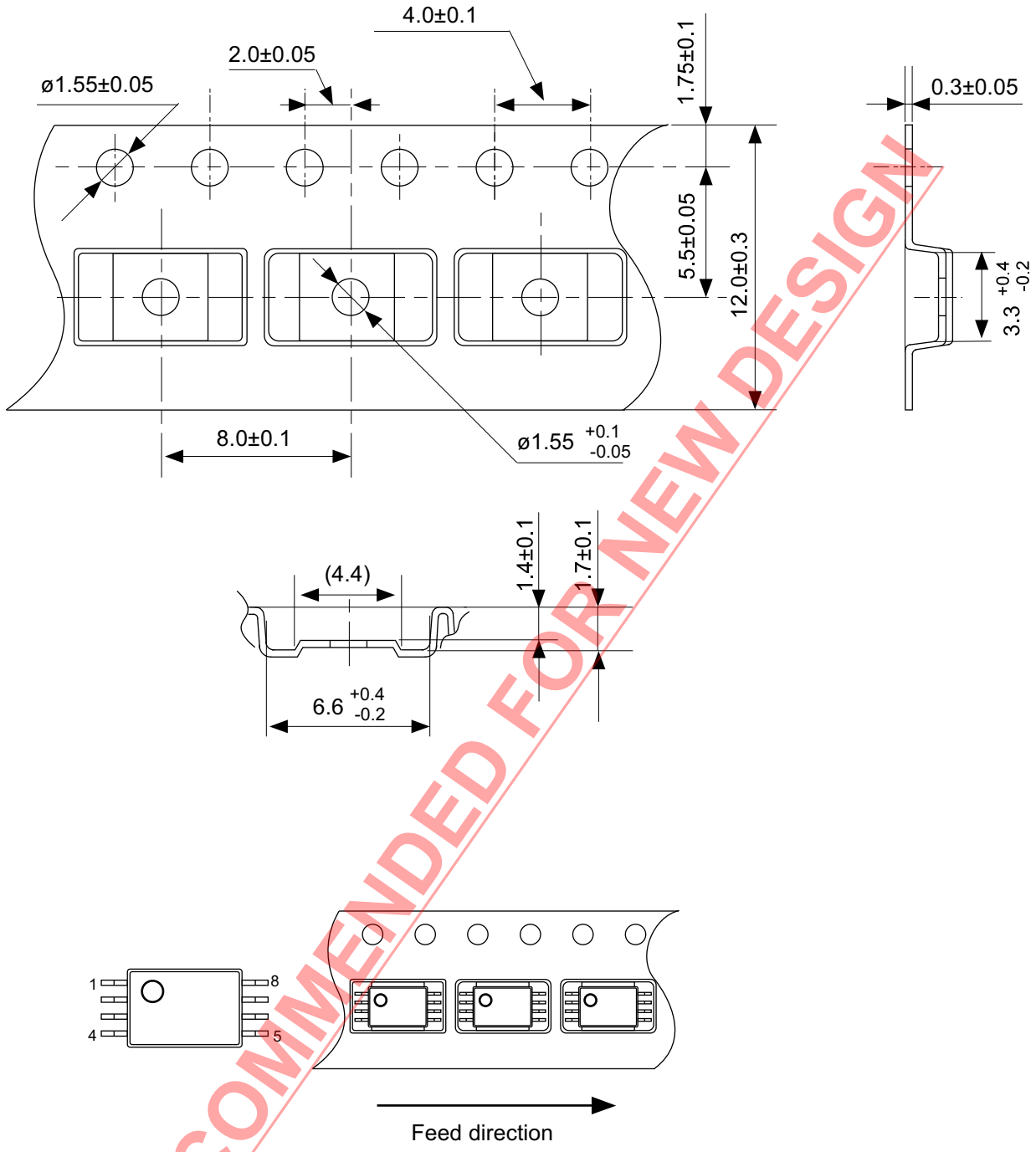

No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
ANGLE	
UNIT	mm

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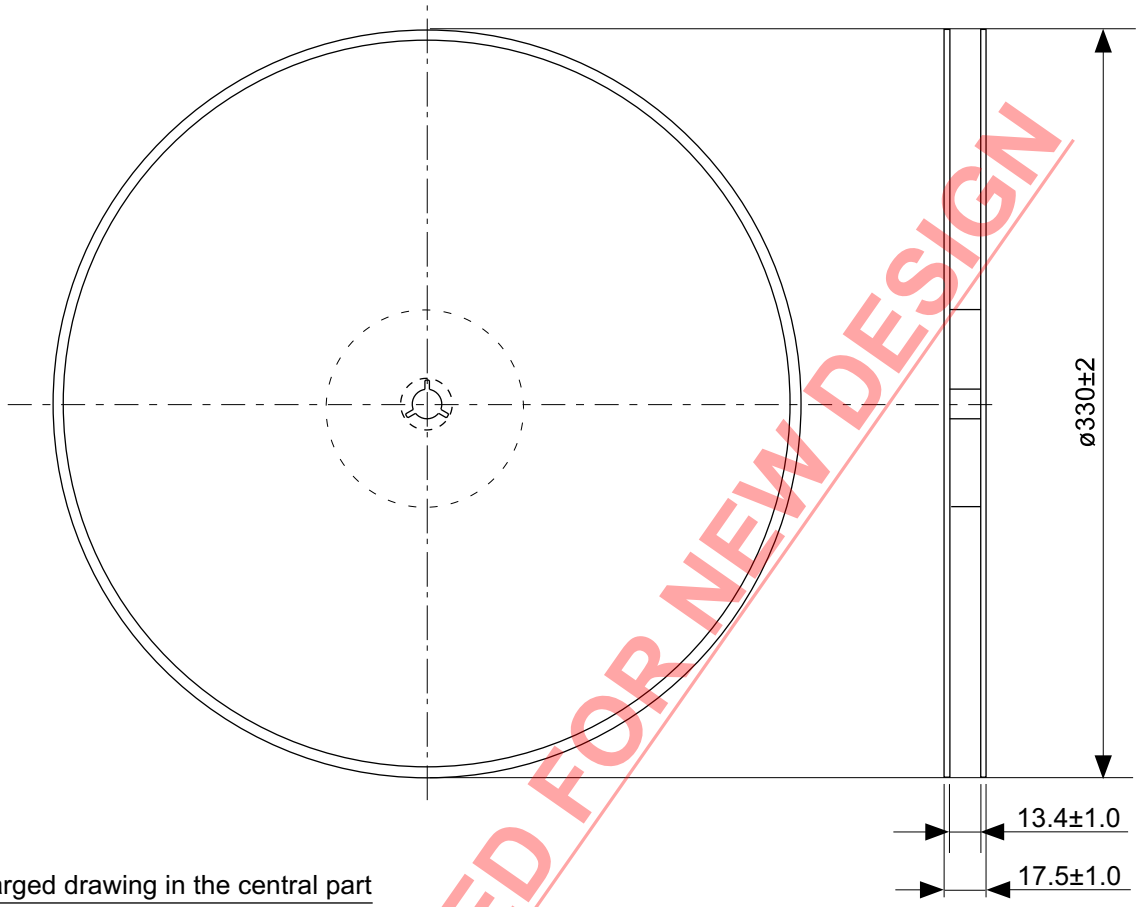
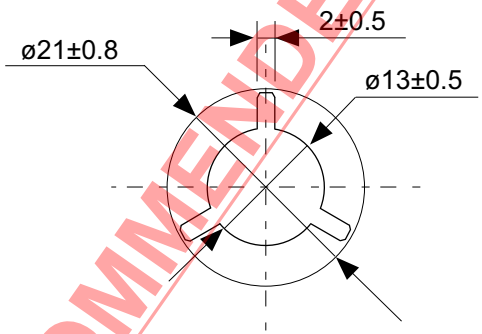
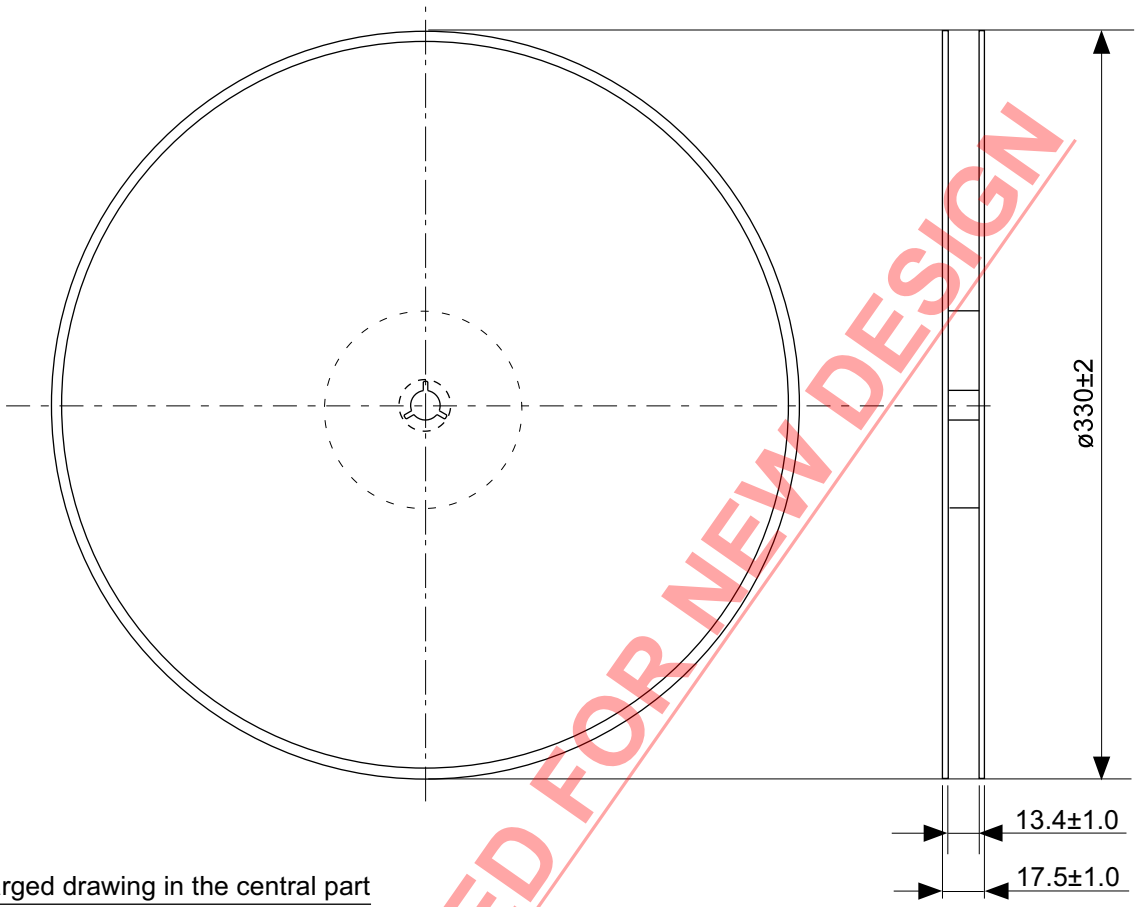


Enlarged drawing in the central part

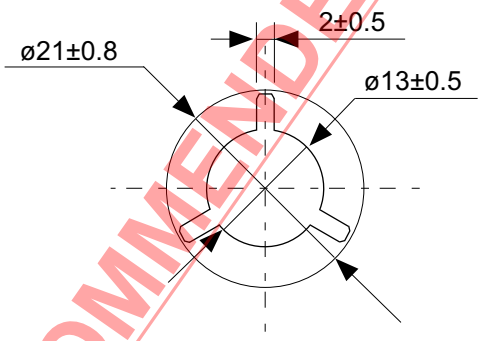


No. FT008-E-R-SD-1.0

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-SD-1.0		
ANGLE		QTY.	3,000
UNIT	mm		
	ABLIC Inc.		



Enlarged drawing in the central part



No. FT008-E-R-S1-1.0

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-S1-1.0		
ANGLE		QTY.	4,000
UNIT	mm		

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