

## HCSL Compatible Clock Generator for PCI Express

### ELECTRICAL SPECIFICATIONS

#### ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	$V_{DD}$	-0.5	4.6	V
Input Voltage Range	$V_I$	-0.5	$V_{DD}+0.5$	V
Output Voltage Range	$V_O$	-0.5	$V_{DD}+0.5$	V
Soldering Temperature			260	°C
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature*		-40	+85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. \*Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

#### AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Input Frequency	Fundamental Crystal		25		MHz
Input ( $F_{IN}$ ) Frequency			25		MHz
Input ( $F_{IN}$ ) Signal Amplitude	Internally AC coupled	0.9		$V_{DD}$	Vpp
Output Frequency		25		200	MHz
Output Enable Time	OE Function; $T_a=25^\circ\text{C}$ , Add one clock period to this measurement for a usable clock output.			10	ns
Output Disable Time	OE Function; $T_a=25^\circ\text{C}$			10	ns
Settling Time	At power-up ( $V_{DD} \geq 2.25\text{V}$ )			10	ms
VDD Sensitivity	Frequency vs. $V_{DD}$ , $\pm 10\%$	-2		2	ppm
Output Rise Time	10/90% $V_{OH}$		0.3	0.5	ns
Output Fall Time	90/10% $V_{OH}$		0.3	0.5	ns
Skew Between Outputs	Measured at 50% $V_{OH}$			250	ps
Duty Cycle	At $V_{DD}/2$	45	50	55	%
Period Jitter, peak-to-peak	- With capacitive decoupling between $V_{DD}$ and GND - At 100MHz - 20,000 samples measured		28		ps
Cycle-to-Cycle, RMS			9		ps
Cycle-to-Cycle, peak			25		ps
TIE, RMS			2		ps

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**DC SPECIFICATIONS**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic	$I_{DD}$	At 100MHz, No Load		25		mA
Operating Voltage	$V_{DD}$		2.25		3.63	V
Output Low Voltage	$V_{OL}$	HCSL termination, (RS = 150Ω, RT = 49.9Ω) 3.3V (RS = 100Ω, RT = 49.9Ω) 2.5V			0.05	V
Output High Voltage	$V_{OH}$		0.65	0.75	0.85	V
Output Current	$I_{OSD}$		13	15	17	mA

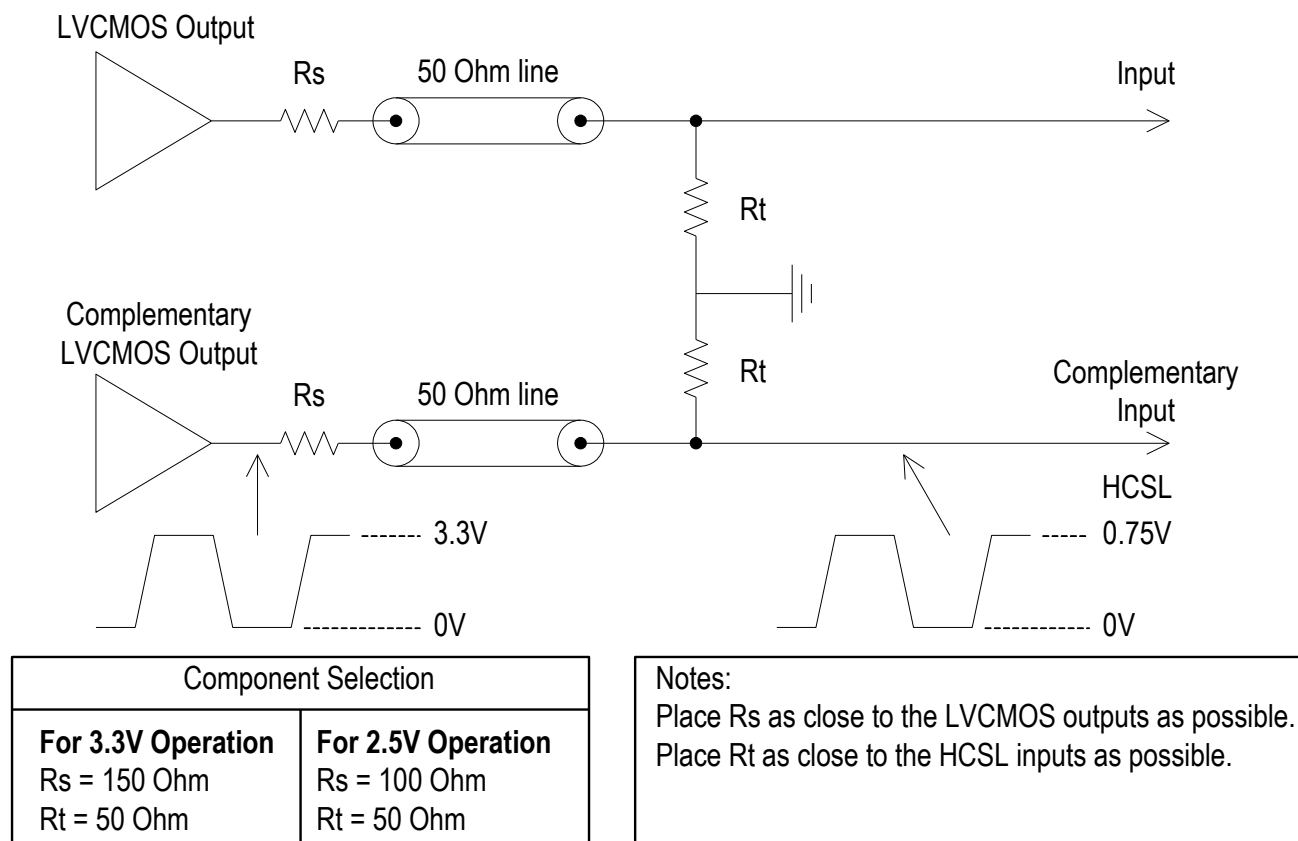
**CRYSTAL SPECIFICATIONS**

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Fundamental Crystal Resonator Frequency	$F_{XIN}$		25		MHz
Crystal Loading Rating	$C_L (xtal)$		18		pF
Maximum Sustainable Drive Level				500	μW
Operating Drive Level			100		μW
Crystal Shunt Capacitance	C0			6	pF
Effective Series Resistance, Fundamental	ESR			45	Ω

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### PCI EXPRESS/HCSL COMPATIBLE LAYOUT GUIDELINES

Figure 1 below describes how to terminate the complementary LVCMOS outputs of PL602-XX for use with HCSL inputs.



**Figure 1**

### PCB LAYOUT CONSIDERATIONS FOR PERFORMANCE OPTIMIZATION

The following guidelines are to assist you with a performance optimized PCB design:

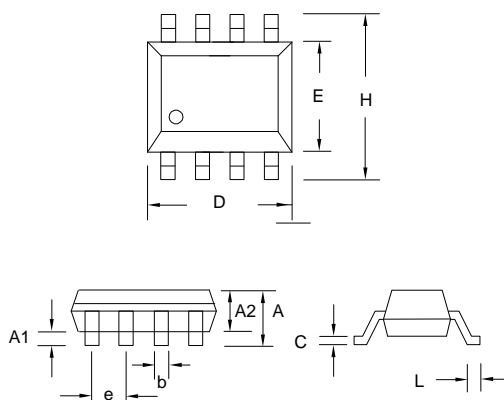
- Keep all the PCB traces to PL602-XX as short as possible, as well as keeping all other traces as far away from it as possible.
- Place the crystal as close as possible to both crystal pins of the device. This will reduce the cross-talk between the crystal and the other signals.
- Separate crystal pin traces from the other signals on the PCB, but allow ample distance between the two crystal pin traces.
- Place a  $0.01\mu\text{F}$ ~ $0.1\mu\text{F}$  decoupling capacitor between VDD and GND, on the component side of the PCB, close to the VDD pin. It is not recommended to place this component on the backside of the PCB.
- It is highly recommended to keep the VDD and GND traces as short as possible.
- When connecting long traces ( $> 1$  inch) to a CMOS output, it is important to design the traces as a transmission line or 'stripline', to avoid reflections or ringing. In this case, the CMOS output needs to be matched to the trace impedance. Usually 'striplines' are designed for  $50\Omega$  impedance and CMOS outputs usually have lower than  $50\Omega$  impedance so matching can be achieved by adding a resistor in series with the CMOS output pin to the 'stripline' trace.

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### PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

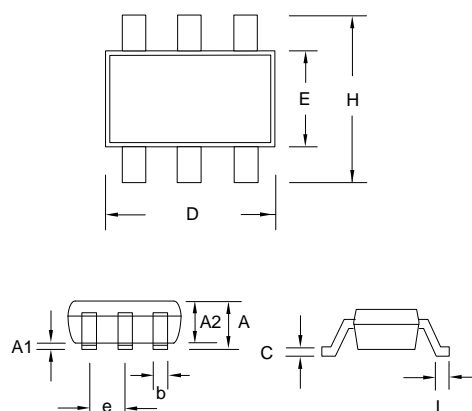
#### SOP-8L

Symbol	Dimension in MM	
	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
B	0.33	0.53
C	0.19	0.27
D	4.80	5.00
E	3.80	4.00
H	5.80	6.20
L	0.40	0.89
e	1.27 BSC	



#### SOT23-6L

Symbol	Dimension in MM	
	Min.	Max.
A	1.05	1.35
A1	0.05	0.15
A2	1.00	1.20
B	0.30	0.50
C	0.08	0.20
D	2.80	3.00
E	1.50	1.70
H	2.60	3.0
L	0.35	0.55
e	0.95 BSC	



## HCSL Compatible Clock Generator for PCI Express

### ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

**For part ordering, please contact our Sales Department:**

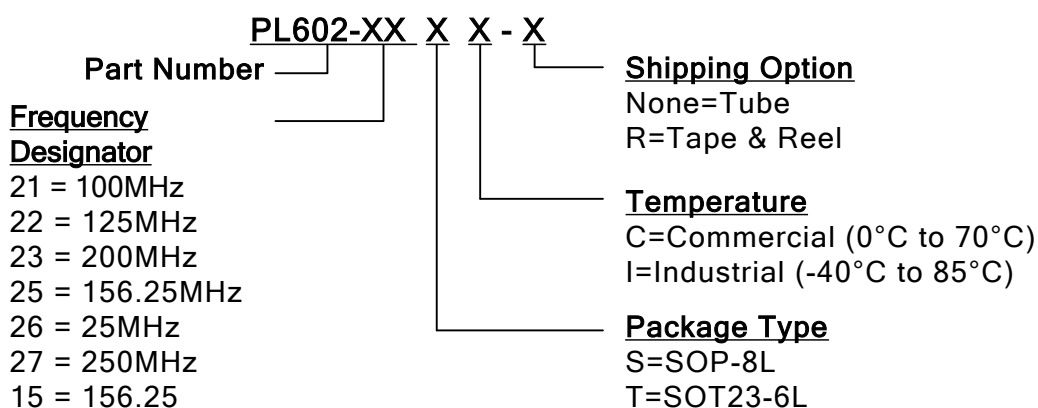
2180 Fortune Drive, San Jose, CA 95131, USA

Tel: (408) 944-0800 Fax: (408) 474-1000

#### PART NUMBER

The order number for this device is a combination of the following:

Part number, Package type and Operating temperature range



Part / Order Number	Marking	Package Option
PL602-2XSC	P602-2X	8-Pin SOP (Tube)
PL602-2XSC-R	SC LLLLL	8-Pin SOP (Tape and Reel)
PL602-1XTC-R	F1X LLL	6-Pin SOT-23 (Tape and Reel)
PL602-2XTC-R	F2X LLL	6-Pin SOT-23 (Tape and Reel)

Note: LLL / LLLLL designate Production Lot.

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