

High Speed Translator Buffer to LVDS

PIN DESCRIPTIONS

Name	Pin Number		Type	Description
	SOP-8L	QFN-16L		
GND	1,3,7	1,2,4,5, 9,13,14,15	P	Ground.
VDD	5,8	7,10,11,12	P	Power supply.
REF_IN	2	3	I	Reference input signal. The frequency of this signal will be reproduced at the output (after translation to LVDS level).
LVDS	4	6	O	LVDS True output.
LVDS_BAR	6	8	O	LVDS Complementary output.
OE	N/A	16	I	Output enable ('1' for enable). Internal pull-up (default is '1').

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	$V_{DD}+0.5$	V
Output Voltage, dc	V_O	-0.5	$V_{DD}+0.5$	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

2. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, No Load	I_{DD}	Fout = 200MHz, LVDS		25	30	mA
Operating Voltage	V_{DD}		2.25		3.63	V
Output Clock Duty Cycle		@ 1.25V (LVDS)	±5% of input			%
Short Circuit Current				±50		mA

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3. AC Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Frequency		0		1000	MHz
Input signal swing	REF_IN input	100			mV
Output Frequency		0		1000	MHz

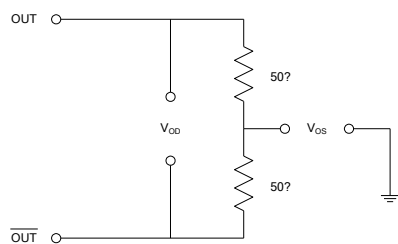
4. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	$R_L = 100\ \Omega$ (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	$V_{out} = V_{DD}$ or GND, $V_{DD} = 0V$		± 1	± 10	μA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

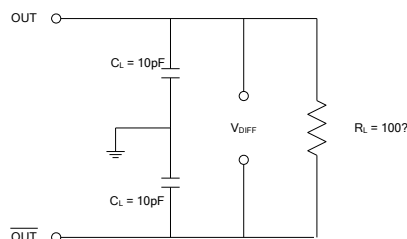
5. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	$R_L = 100\ \Omega$ $C_L = 10\ pF$ (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

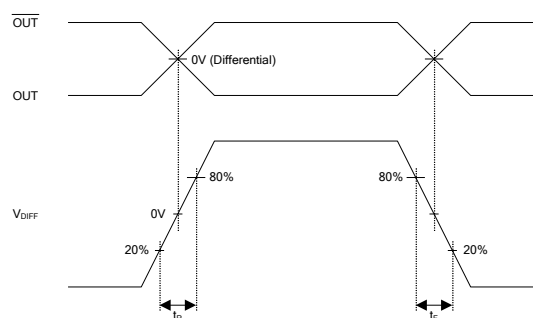
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transition Time Waveform

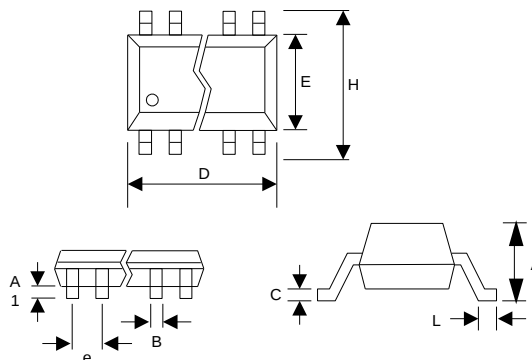


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PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

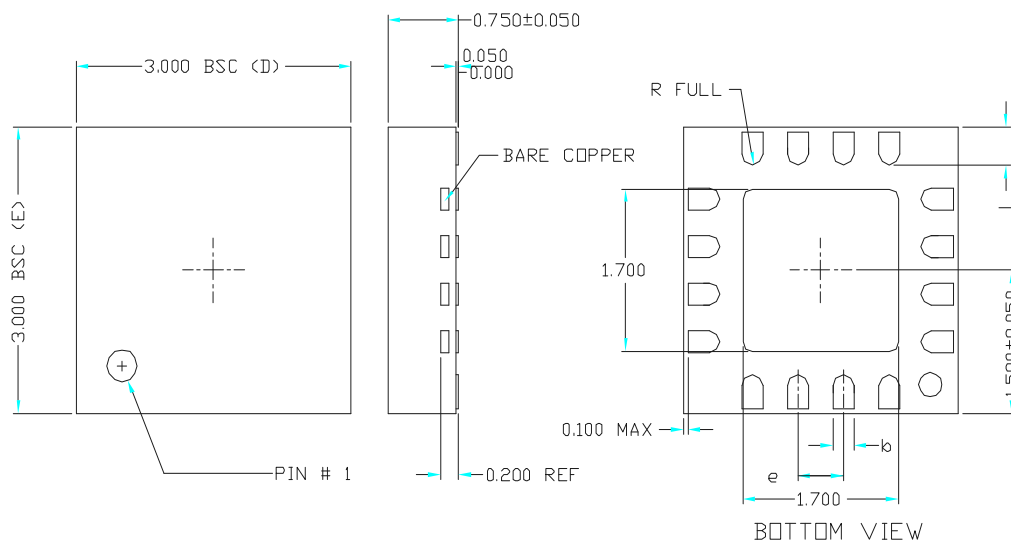
8 PIN SOP (dimensions in mm)

SOP-8L		
Symbol	Min.	Max.
A	1.47	1.73
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	4.95
E	3.80	4.00
H	5.80	6.20
L	0.38	1.27
e	1.27 BSC	



VARIATIONS:

SYMBOL	QFN-16L		
	MIN	NOM	MAX
e	0.50 BSC		
b	0.18	0.23	0.30
L	0.30	0.40	0.50
ND	4		
NE	4		



High Speed Translator Buffer to LVDS**ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)**

For part ordering, please contact our Sales Department:

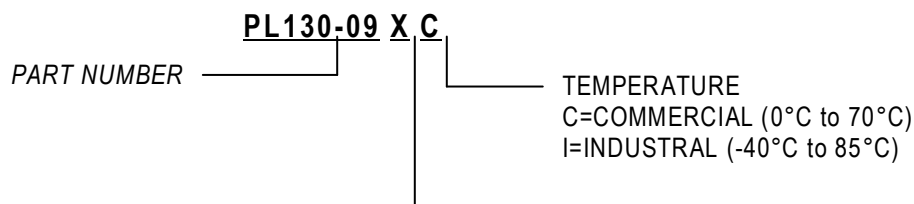
2180 Fortune Drive, San Jose, CA 95131, USA

Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER

The order number for this device is a combination of the following:

Device number, Package type and Operating temperature range



Part/Order Number	Marking	Package Option
PL130-09QC-R	P130 09	16-pin QFN-16L - (Tape and Reel)
PL130-09SC	P130-09	8-pin SOP-8L - (Tube)
PL130-09SC-R	P130-09	8-pin SOP-8L - (Tape and Reel)

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