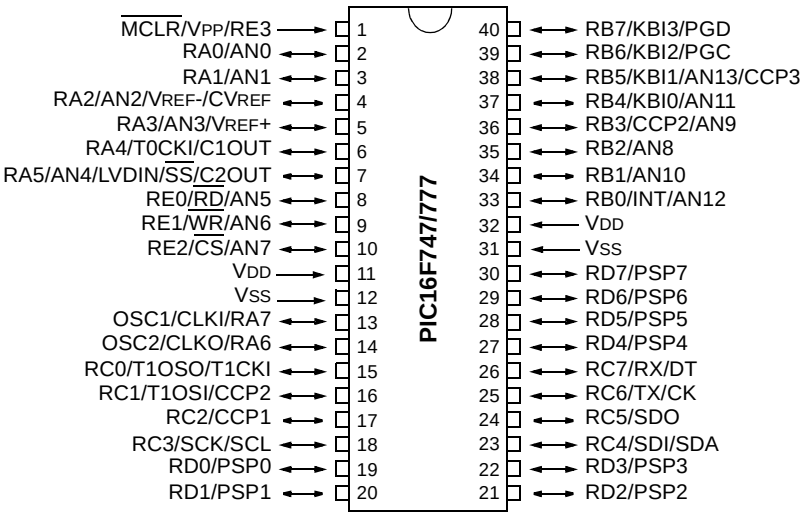
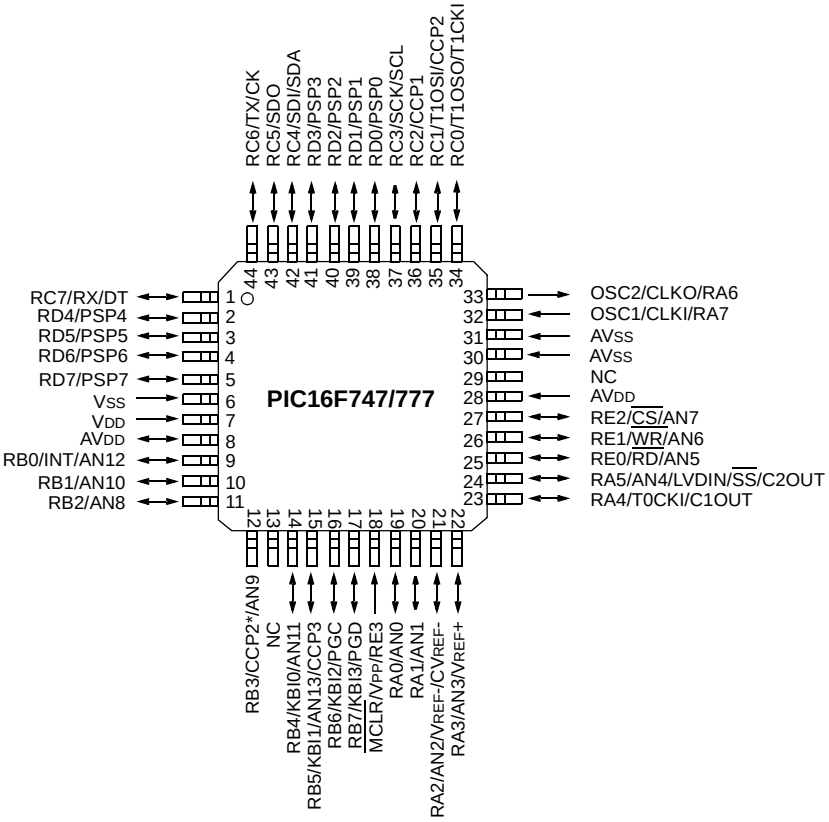
Pin Diagrams (Continued)

PDIP (40-pin)



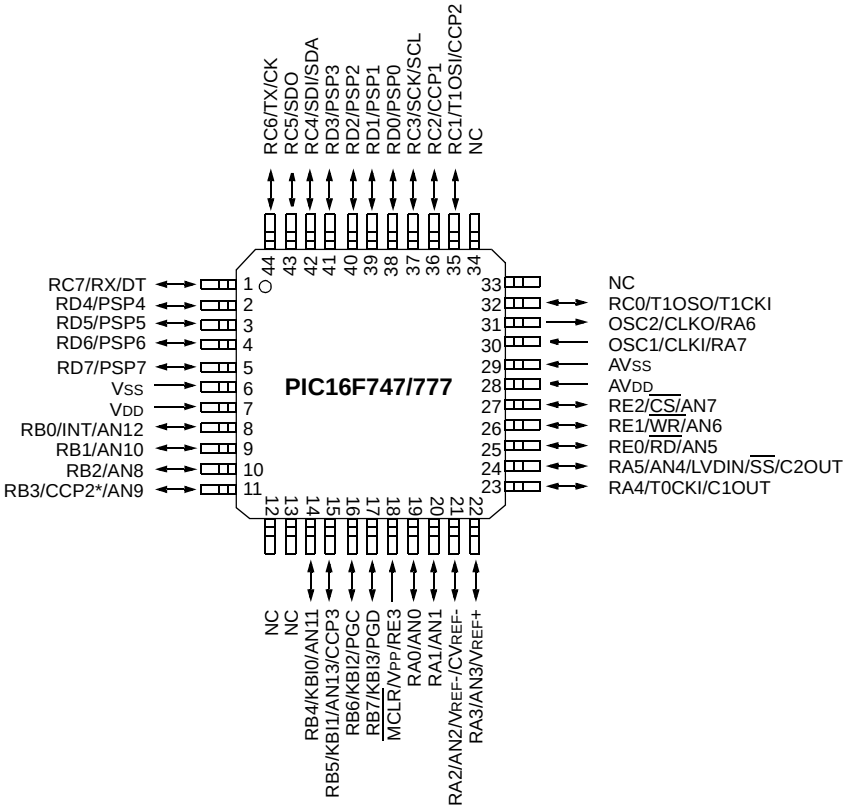
QFN (44-pin)



* Alternate pinout for CCP2 is enabled by a fuse.

Pin Diagrams (Continued)

TQFP (44-pin)



* Alternate pinout for CCP2 is enabled by a fuse.

2.0 PROGRAM MODE ENTRY

2.1 User Program Memory Map

The user memory space extends from 0x0000 to 0x1FFF (8K), or 0x0000 to 0x0FFF (4K). Table 2-1 shows the actual implementation of program memory in the PIC16F7X7 family. Configuration memory begins at 0x2000, and continues to 0x3FFF. The PC will increment from 0x0000 to 0x1FFF and wrap to 0x0000, 0x2000 to 0x3FFF and wrap around to 0x2000 (not to 0x0000).

Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to program memory is to reset the part and re-enter Program/Verify mode, as described in **Section 2.3 "Program/Verify Mode"**.

For PIC16F7X7 devices, configuration memory is selected when the PC points to any address in the range of 0x2000-0203F; however, only locations 0x2000 through 0x2008 are implemented. Addressing locations beyond 0x203F will access program memory (see Figure 2-1).

TABLE 2-1: IMPLEMENTATION OF PROGRAM MEMORY IN THE PIC16F7X7 FAMILY

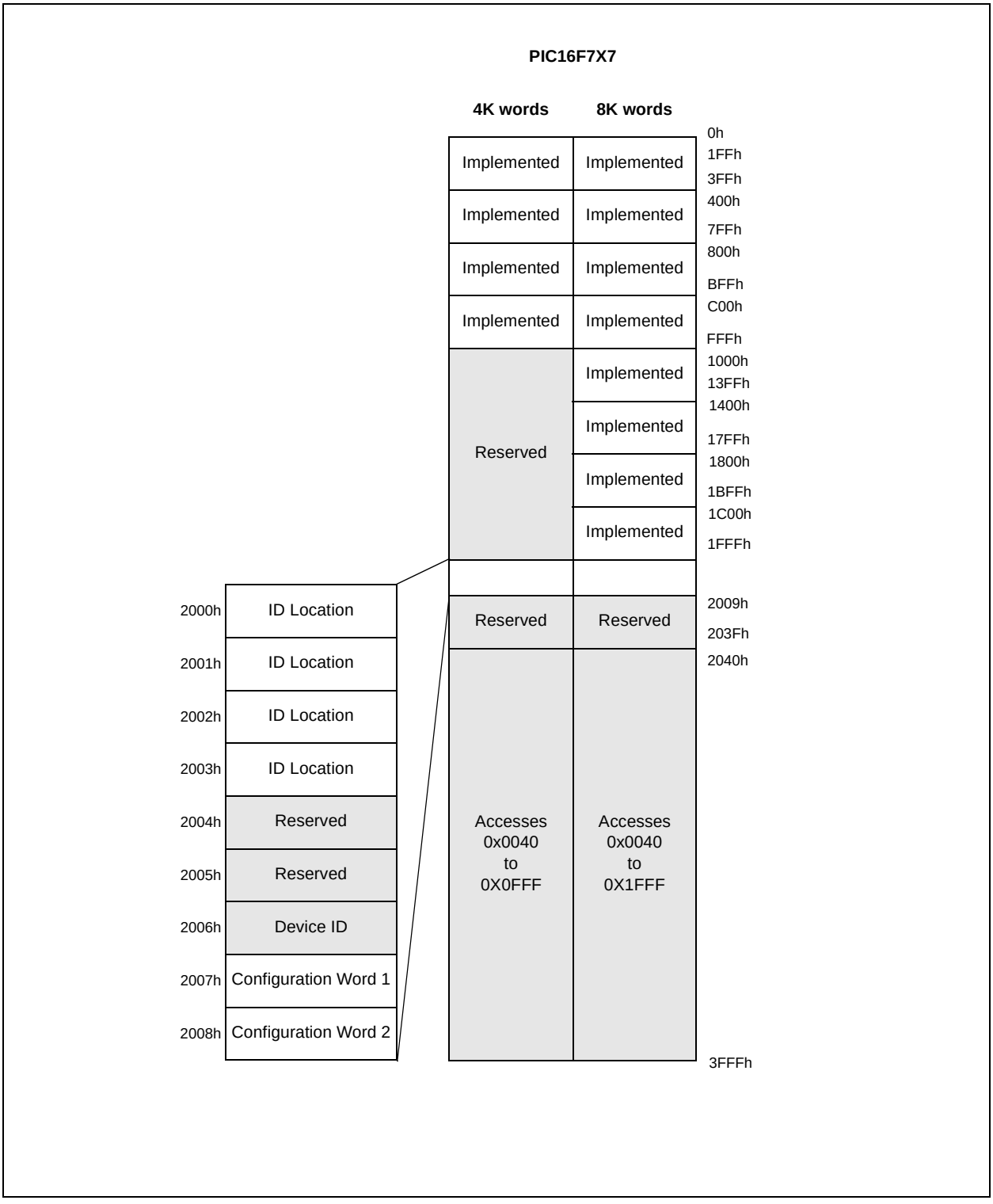
Device	Program Memory Size
PIC16F737/747	0x0000-0x0FFF (4K)
PIC16F767/777	0x0000-0x1FFF (8K)

2.2 ID Locations

A user may store identification information (ID) in four ID locations mapped to [0x2000:0x2003]. It is recommended that each ID location word is written as '11 1111 1000 bbbb', where 'bbbb' is ID information. The ID locations can be read after code protection is enabled.

To understand the program memory read mechanism after code protection is enabled, refer to **Section 4.0 "Code Protection"**. Table 4-1 shows specific calculations and behavior for each of the PIC16F7X7 devices.

FIGURE 2-1: PROGRAM MEMORY MAPPING FOR PIC16F7X7 DEVICES



2.3 Program/Verify Mode

The Program/Verify mode is entered by holding pins RB6 and RB7 low, while raising the $\overline{MCLR}$ pin from V_{IL} to V_{PP}. Once in this mode, the user program memory and the configuration memory can be accessed and programmed in serial fashion. (RB6 and RB7 are Schmitt Trigger inputs in this mode.)

Note:	The $\overline{MCLR}$ pin should be raised from below V_{IL} to above the minimum V_{IHH} (V_{PP}) within 100 µs of V_{DD} rise. This ensures that the device always enters Programming mode before any instructions that may be in program memory can be executed. Otherwise, unintended instruction execution could occur when the INTRC clock source is configured as the primary clock.

The sequence that enters the device into the Programming/Verify mode, places all other logic into the Reset state. All I/O pins are in the Reset state (high-impedance inputs).

A device Reset will clear the PC and point to address 0x0000. The Increment Address command will increment the PC. The Load Configuration command will set the PC to 0x2000. The available commands are shown in Table 2-2.

The normal sequence for programming two program memory words at a time is as follows:

1. Issue the Load Data command to load a word at the current (even) program memory address.
2. Issue an Increment Address command.
3. Load a word at the current (odd) program memory address using the 'Load Data' command.
4. Issue a Begin Programming command to begin programming.
5. Wait tprog (about 1 ms).
6. Issue an End Programming command.
7. Increment to the next address.
8. Repeat this sequence as required to write program and configuration memory.

The alternative sequence for programming one program memory word at a time is as follows:

1. Set a word for the current memory location using the Load Data command.
2. Issue a Begin Programming command to begin programming.
3. Wait tprog (about 1 ms).
4. Issue an End Programming command.
5. Increment to the next address.
6. Repeat this alternative sequence as required to write program and configuration memory.

The address and program counter is reset to 0x0000 by resetting the device (taking $\overline{MCLR}$ below V_{IL}) and re-entering Programming mode. Program and configuration memory may then be read or verified using the Read Data and Increment Address commands.

2.3.1 SERIAL PROGRAM/VERIFY OPERATION

RB6 is used as a clock input pin, and RB7 is used for entering command bits and data input/output. To enter a command, the clock pin (RB6) is pulsed six times. Each command bit is latched on the falling edge of the clock (RB6), with the Least Significant bit (LSb) of the command being input first. The data on pin RB7 needs a minimum setup (tset1) and hold time (thold1) with respect to the falling edge of the clock. The Read and Load commands are specified to have a minimum delay (tdly1) between the command and data. After this delay, the clock pin is cycled 16 times, with the first cycle being a Start bit (0) and the last cycle being a Stop bit (0). Data is transferred LSb first (see Figure 5-1).

During a read operation, the LSb will be output on pin RB7 on the rising edge of the second clock pulse and during a load operation, the LSb will be latched on the falling edge of the second clock pulse. A minimum delay (tdly2) is required between consecutive commands (see Figure 5-2).

To allow for decoding of commands and reversal of data pin configuration, a time separation of at least (tdly1) is required between a command and a data word, or another command (see Figure 5-3).

The available commands are listed below:

- Load Configuration
- Load Data for Memory
- Read Data from Memory
- Increment Address
- Begin Programming
- Bulk Erase Program Memory
- End Programming

TABLE 2-2: COMMAND MAPPING FOR PIC16F7X7

Command	Mapping (LSb … MSb)						Data (LSb first)
Load Configuration (Set PC = 2000h)	0	0	0	0	x	x	0, data (14), 0
Load Data for Memory	0	1	0	0	x	x	0, data (14), 0
Read Data from Memory	0	0	1	0	x	x	0, data (14), 0
Increment Address	0	1	1	0	x	x	
Begin Programming	0	0	0	1	x	x	
Bulk Erase Program Memory (Chip Erase)	1	0	0	1	x	x	
End Programming	0	1	1	1	x	x	

2.3.1.1 Load Configuration

After receiving the Load Configuration command, the PC will be set to 0x2000 and the data sent with the command is discarded. The four ID locations and the Configuration Word can then be programmed using the normal programming sequence, as described in **Section 2.3 "Program/Verify Mode"**. A description of the memory mapping schemes of the program memory for normal operation and Configuration mode operation is shown in Figure 2-1. After the configuration memory is entered, the only way to get back to the user program memory is to exit the Program/Verify Test mode by taking $\overline{MCLR}$ low.

2.3.1.2 Load Data for Memory

The device will load in a 14-bit "data word" (LSb first) when 16 cycles are applied, as described previously. A timing diagram for the Load Data command is shown in Figure 5-1.

2.3.1.3 Read Data from Memory

The device will transmit data bits out of the memory (program or configuration) currently addressed by the PC, starting with the second rising edge of the clock input. RB7 will go into Output mode on the second rising clock edge and will revert back to Input mode (high-impedance) after the 16th rising edge. Data is sent out LSb first. A timing diagram for this command is shown in Figure 5-2.

If the device is code-protected, user program memory will read all '0's. Configuration memory can still be read.

2.3.1.4 Increment Address

The PC is incremented by one. A timing diagram for this command is shown in Figure 5-3.

2.3.1.5 Begin Programming

A Load Data command must be issued before every Begin Programming command. Programming of memory (configuration or program) will begin after this command is received and decoded. Programming requires (tprog) time and is terminated using an End Programming command.

2.3.1.6 Chip Erase (Program Memory)

Erasure of configuration and program memory begins after this command is received and decoded. The erase sequence is self-timed and it is not necessary to issue an End Programming command, only to wait for the appropriate time interval (tera) for the entire erase sequence, before issuing another command.

This procedure will disable code protection (code-protect bit = 1); however, all data within the program memory will be erased when this command is executed and thus, the security of the data or code is not compromised.

Note:	All chip erase operations must take place with V_{DD} between 4.75V and 5.25V (i.e., V_{DDP}).

2.4 Programming Algorithm Requires Variable V_{DD}

The PIC16F7X7 devices use an intelligent algorithm. The algorithm calls for program verification at V_{DDAPP}.

The actual chip erase and programming must be done with V_{DD} in the V_{DDP} range (see Table 5-1).

V_{DDP} = V_{DD} range required during programming

V_{DDAPP} = V_{DD} in the target application

Programmers must verify the PIC16F7X7 devices at V_{DDAPP}. Since Microchip may introduce future versions of the PIC16F7X7 devices with a broader V_{DD} range, it is best that these levels are user selectable (defaults are acceptable).

Note:	Any programmer not meeting this requirement may only be classified as a "prototype" or "development" programmer, but not a "production quality" programmer.

FIGURE 2-2: PROGRAMMING METHOD FLOWCHART (SHEET 1 OF 3)

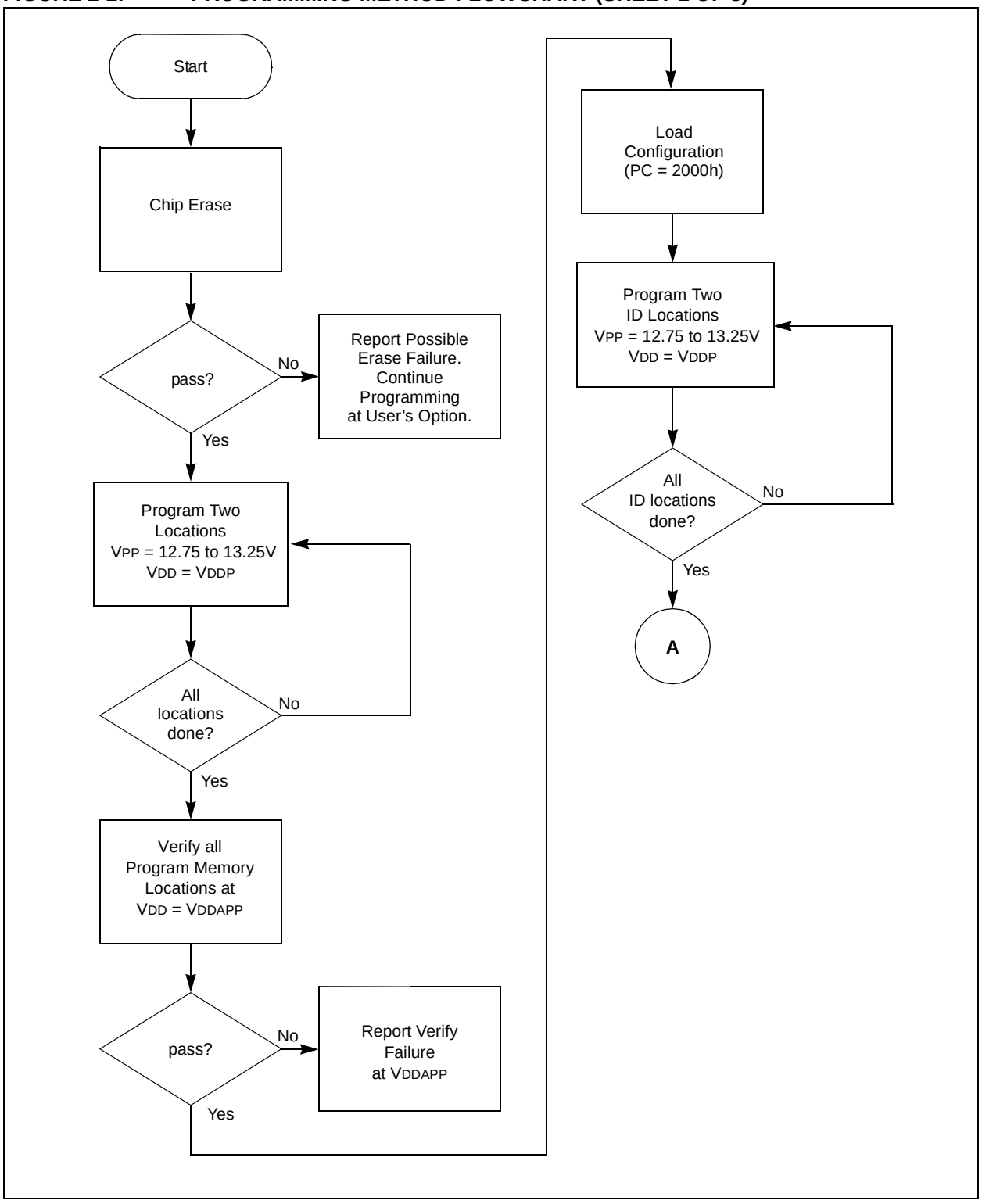


FIGURE 2-3: PROGRAMMING METHOD FLOWCHART (SHEET 2 OF 3)

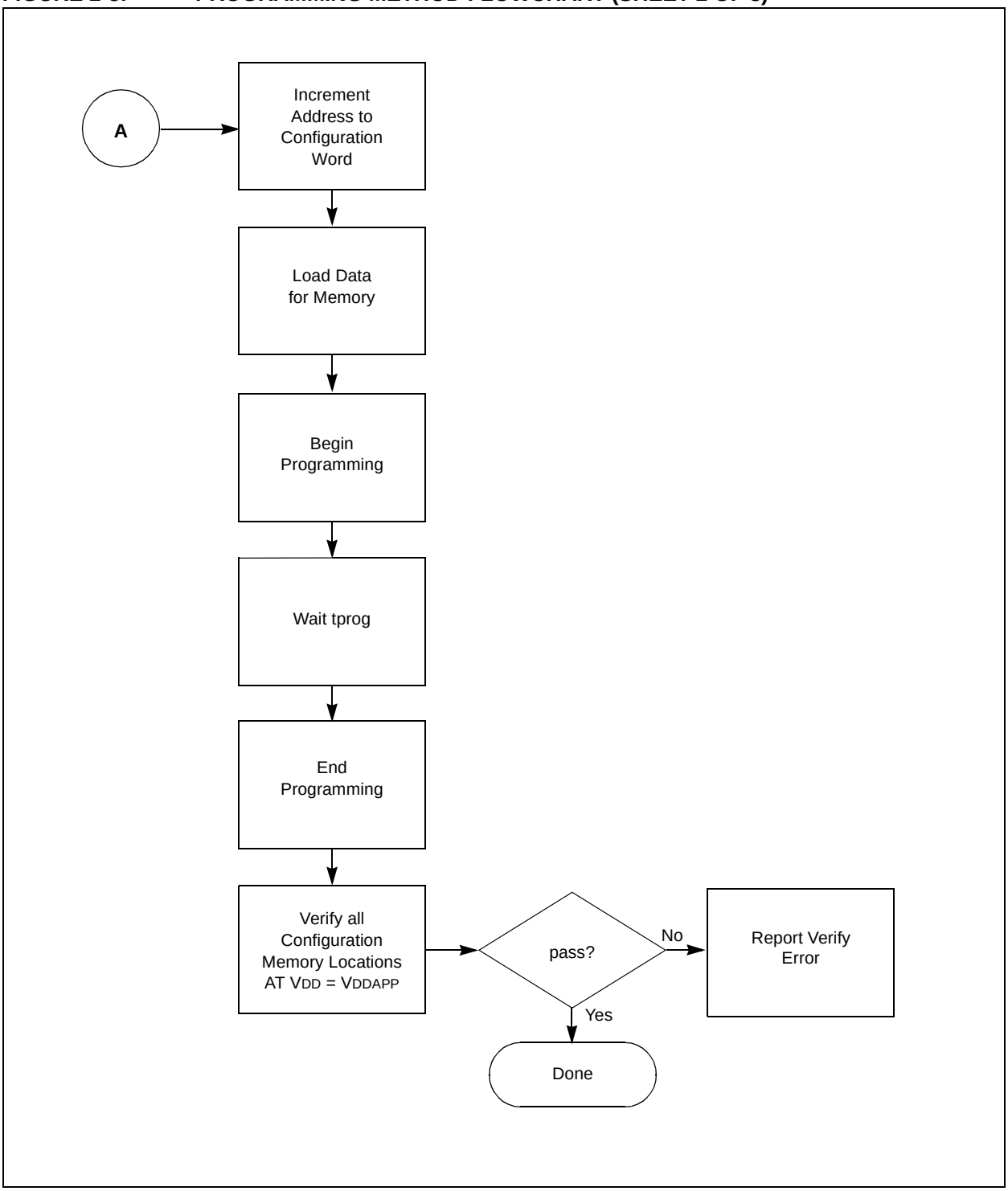
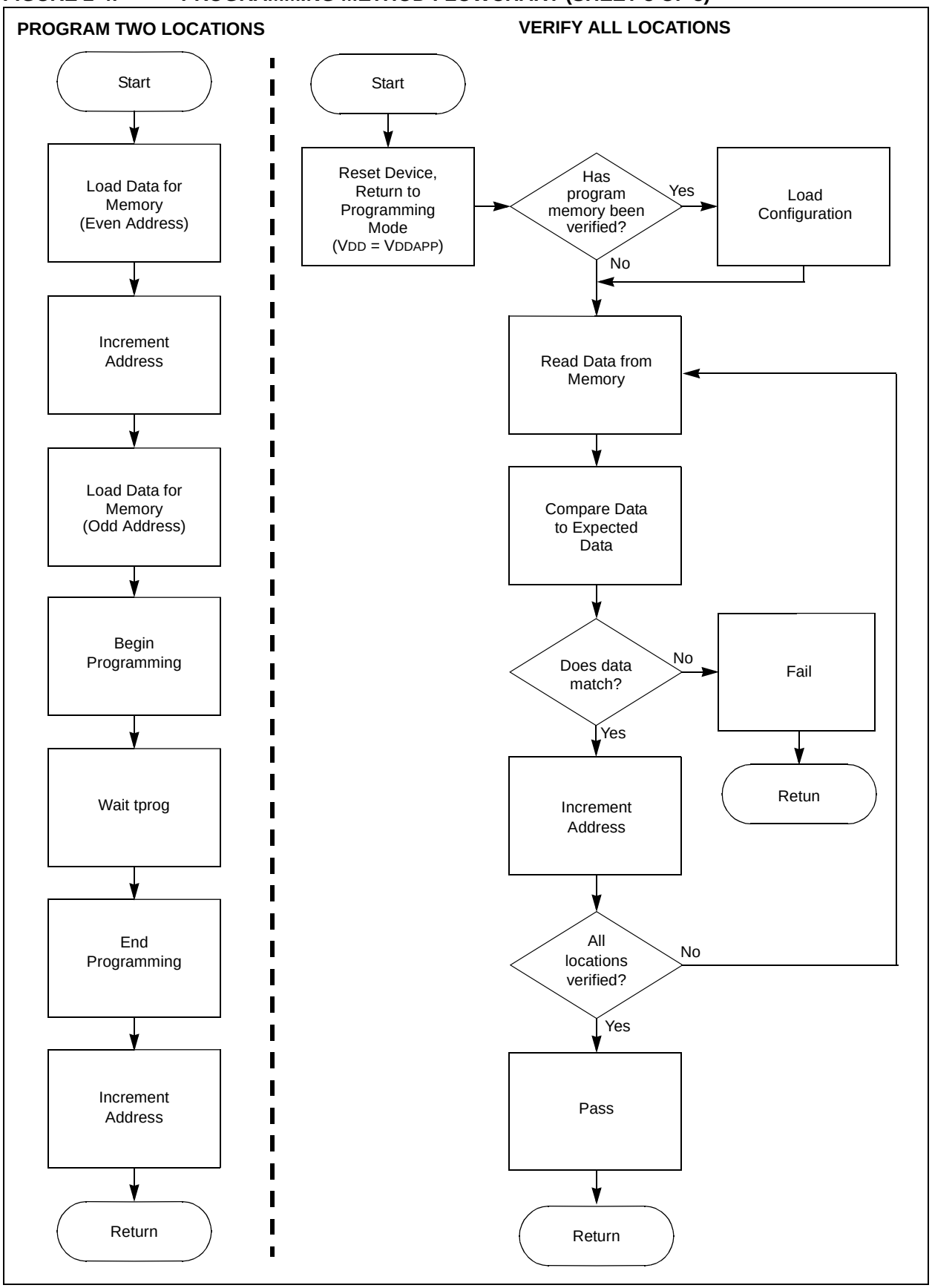


FIGURE 2-4: PROGRAMMING METHOD FLOWCHART (SHEET 3 OF 3)



3.0 CONFIGURATION WORD

The PIC16F7X7 devices have configuration bits in configuration words located at 0x2007 and 0x2008. These bits can be cleared (reads '0'), or left unchanged (reads '1'), to select various device configurations.

3.1 Device ID Word

The device ID word for the PIC16F7X7 devices is located at 2006h. The nine Most Significant bits are the device ID number, while the five Least Significant bits are the device revision number.

TABLE 3-1: DEVICE ID VALUE

Device	Device ID Word (0x2006)	
	Dev	Rev
PIC16F737	00 1011 101	n nnnn
PIC16F747	00 1011 111	n nnnn
PIC16F767	00 1110 101	n nnnn
PIC16F777	00 1101 111	n nnnn

REGISTER 3-1: CONFIGURATION WORD 1 (2007h) REGISTER FOR PIC16F7X7

CP	CCPMX	RESV	–	–	BORV1	BORV0	BOREN	MCLRE	F0SC2	$\overline{\text{PWRTEN}}$	WDTEN	F0SC1	F0SC0
bit 13													bit 0

bit 13 **CP:** Flash Program Memory Code Protection bits
1 = Code protection off
0 = 0000h to 1FFFh code-protected for 767, 777 and 0000h to 0FFFh for 737, 747 (all protected)

bit 12 **CCPMX**: CCP2 Multiplex bit
1 = CCP2 is on RC1
0 = CCP2 is on RB3

bit 11 **Reserved:** Set to '1' for Normal Operation

bit 10-9 **Unimplemented:** Read as '1'

bit 8-7 **BORV<1:0>:** Brown-out Reset Voltage bits
11 = V_{BOR} set to 2.0V
10 = V_{BOR} set to 2.7V
01 = V_{BOR} set to 4.2V
00 = V_{BOR} set to 4.5V

bit 6 **BOREN:** Brown-out Reset Enable bit
BOREN combines with BORSEN to control when BOR is enabled and how it is controlled
BOREN:BORSEN
11 = BOR enabled and always on
10 = BOR enabled during operation and disabled during Sleep by hardware
01 = BOR controlled by software bit SBOREN
00 = BOR disabled

bit 5 **MCLRE:** RE3/V_{PP}/$\overline{\text{MCLR}}$ Pin Function Select bit
1 = RE3/V_{PP}/$\overline{\text{MCLR}}$ pin function is $\overline{\text{MCLR}}$
0 = RE3/V_{PP}/$\overline{\text{MCLR}}$ pin function is digital input only, $\overline{\text{MCLR}}$ gated to '1'

bit 3 **$\overline{\text{PWRTEN}}$:** Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 2 **WDTEN:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 4, 1-0 **FOSC2:FOSC0:** Oscillator Selection bits
111 = EXTRC oscillator; CLKO function on OSC2/CLKO/RA6
110 = EXTRC oscillator; Port I/O function on OSC2/CLKO/RA6
101 = INTRC oscillator; CLKO function on OSC2/CLKO/RA6 and Port I/O function on OSC1/CLKI/RA7
100 = INTRC oscillator; Port I/O function on OSC1/CLKI/RA7 and OSC2/CLKO/RA6
011 = EXTCLK; Port I/O function on OSC2/CLKO/RA6
010 = HS oscillator
001 = XT oscillator
000 = LP oscillator

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 3-2: CONFIGURATION WORD 2 (2008h) REGISTER FOR PIC16F7X7

–	–	–	–	–	–	–	BORSEN	–	–	–	–	IESO	FCMEN
bit 13													bit 0

bit 13-7 **Unimplemented:** Read as '1'

bit 6 **BORSEN:** Brown-out Reset Software Enable bit
Refer to Configuration Word Register 1 (Register 3-1), bit 6 for the function of this bit

bit 5-2 **Unimplemented:** Read as '1'

bit 1 **IESO:** Internal External Switchover bit
1 = Internal External Switchover mode enabled
0 = Internal External Switchover mode disabled

bit 0 **FCMEN:** Fail-Safe Clock Monitor Enable bit
1 = Fail-Safe Clock Monitor enabled
0 = Fail-Safe Clock Monitor disabled

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

4.0 CODE PROTECTION

Once code protection is enabled, all program memory locations read all '0's; further programming of program memory is disabled. ID locations and the Configuration Word may still be read and programmed (1's to 0's only).

4.1 Disabling Code Protection

The following procedure should be performed before any other programming is attempted. This procedure also turns off code protection (code-protect bit = 1); however, ***all program memory will be erased when this procedure is executed and thus, the security of the code is not compromised.***

Procedure to disable code protection:

a) Issue the Chip Erase command.
b) Wait for the erase cycle time (tera) to pass. The program memory is erased, then the configuration memory is erased.

4.2 Embedding Configuration Word and ID Information in the HEX File

To allow portability of code, the programmer is required to read the Configuration Word and ID locations from the hex file, when loading the hex file. If Configuration Word information was not present in the hex file, then a simple warning message may be issued. Similarly, while saving a hex file, Configuration Word and ID information must be included. An option to not include this information may be provided.

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

4.3 Checksum Computation

The checksum is calculated by reading the contents of the PIC16F7X7 memory locations and adding up the opcodes, up to the maximum user addressable location. Any carry bits exceeding 16 bits are neglected. Finally, the Configuration Word (appropriately masked) is added to the checksum. Checksum computation for each member of the PIC16F7X7 is shown in Table 4-1.

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The Configuration Word, appropriately masked
- Masked ID locations (when applicable)

The Least Significant 16 bits of this sum are the checksum.

Table 4-1 describes how to calculate the checksum for each device. Note that the checksum calculation differs depending on the code protection setting. Since the program memory locations read out differently depending on the code protection setting, the table describes how to manipulate the actual program memory values to simulate the values that would be read from a protected device. When calculating a checksum of a non-protected device, the entire program memory can simply be read and summed. The Configuration Word and ID locations can always be read.

TABLE 4-1: CHECKSUM COMPUTATION FOR PIC16F7X7 DEVICES

Device	Code-protect	Checksum	Blank Value	0x25E6 at 0x0000 and max address
PIC16F737	OFF	SUM(0000:0FFF) + (CONFIG0 & 39FF) + (CONFIG1 & 0043)	2A42	F610
	ALL	(CONFIG0 & 39FF) + (CONFIG1 & 0043) + SUM(IDs)	4484	1052
PIC16F747	OFF	SUM(0000:0FFF) + (CONFIG0 & 39FF) + (CONFIG1 & 0043)	2A42	F610
	ALL	(CONFIG0 & 39FF) + (CONFIG1 & 0043) + SUM(IDs)	4484	1052
PIC16F767	OFF	SUM(0000:1FFF) + (CONFIG0 & 39FF) + (CONFIG1 & 0043)	1A42	E610
	ALL	(CONFIG0 & 39FF) + (CONFIG1 & 0043) + SUM(IDs)	3484	0052
PIC16F777	OFF	SUM(0000:1FFF) + (CONFIG0 & 39FF) + (CONFIG1 & 0043)	1A42	E610
	ALL	(CONFIG0 & 39FF) + (CONFIG1 & 0043) + SUM(IDs)	3484	0052

Legend:
CFWD = Configuration Word
SUM[a:b] = [Sum of locations a to b inclusive]
SUM_ID = ID locations masked by 0x0F, then concatenated into a 16-bit value with ID0 as the Most Significant nibble.
For example, ID0 = 0x01, ID2 = 0x02, ID3 = 0x03, ID4 = 0x04, then SUM_ID = 0x1234
Checksum = [Sum of all the individual expressions] **MODULO** [0xFFFF]
\+ = Addition
& = Bitwise AND

5.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

5.1 AC/DC Characteristics

TABLE 5-1: TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

Standard Operating Conditions (unless otherwise stated) Operating Temperature: +10°C ≤ TA ≤ +40°C Operating Voltage: 4.5V ≤ VDD ≤ 5.5V						
Characteristics	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions/Comments**
General						
VDD level for read and verification	VDD	2.0	—	5.5	V	
VDD level for programming and erasing	VDDP	4.75	—	5.25	V	
High voltage on $\overline{MCLR}$ for chip erase and program write operations	VPP	12.75	—	13.25	V	**(Notes 1, 2)**
$\overline{MCLR}$ rise time (VSS to VPP) for Test mode entry	tVHHR	—	—	1.0	µs	
(RB6, RB7) input high level	VIH1	0.8 VDD	—	—	V	Schmitt Trigger input
(RB6, RB7) input low level	VIL1	—	—	0.2 VDD	V	Schmitt Trigger input
Serial Program/Verify						
Data in setup time before clock↓	tset1	100	—	—	ns	
Data in hold time after clock↓	thld1	100	—	—	ns	
Data input not driven to next clock input (delay required between command/data or command/command)	tdly1	1.0	—	—	µs	
Delay between clock↓ to clock↑ of next command or data	tdly2	1.0	—	—	µs	
Clock↑ to data out valid (during read data)	tdly3	200	—	—	ns	
Erase cycle time	tera	30	—	—	ms	**(Note 3)**
Programming cycle time	tprog	1	—	1	ms	

Note 1: VPP should be current limited to about 100 mA.

2: VPP must remain above VDDP + 4.0V to remain in Programming mode, while not actually erasing or programming.

3: The chip erase is self-timed.

FIGURE 5-1: LOAD DATA COMMAND MODE (PROGRAM/VERIFY)

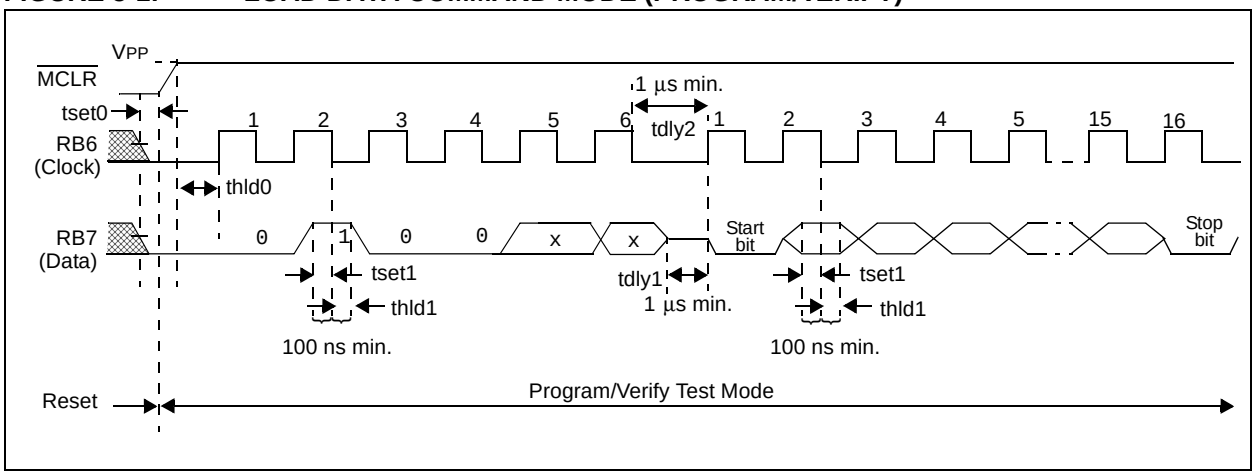


FIGURE 5-2: READ DATA COMMAND MODE (PROGRAM/VERIFY)

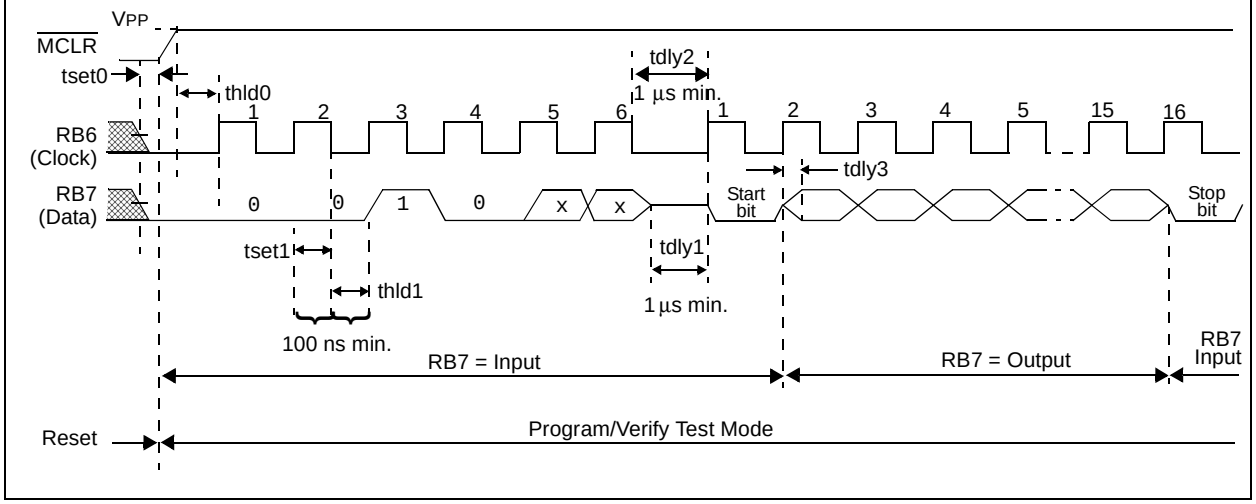
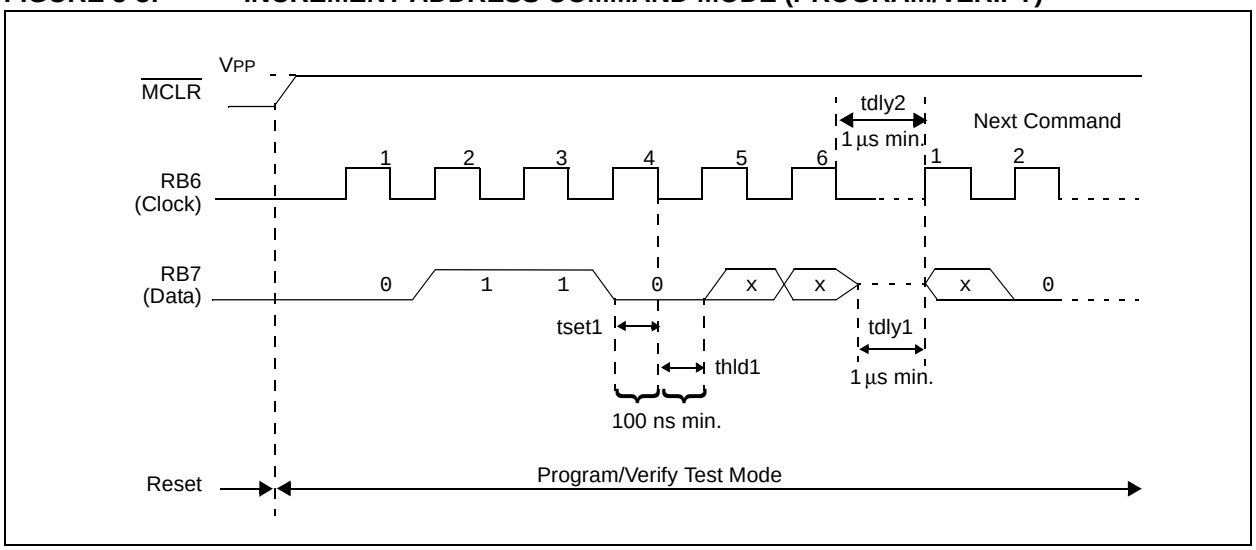


FIGURE 5-3: INCREMENT ADDRESS COMMAND MODE (PROGRAM/VERIFY)



Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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ISO/TS 16949:2002

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Korea - Seoul
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Singapore
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France - Massy
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10/20/04