Peripheral Features: (Continued)

- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) Module:
  - Supports LIN 2.1 and J2602
  - Auto-Baud Detect
  - Auto Wake-up on BREAK character
- mTouch™ Sensing Oscillator Module:
  - Up to 12 input channels
- Data Signal Modulator Module:
  - Selectable modulator and carrier sources
- SR Latch:
  - Multiple Set/Reset input options
  - Emulates 555 Timer applications
- On-board Voltage Regulator:
  - Output voltage of 5.0V with tolerances of ±2% over temperature range
  - Maximum continuous input voltage of 30V
  - Internal thermal overload protection
  - Internal short circuit current limit
  - External components limited to filter capacitor only and load capacitor
  - Automatic thermal shutdown
- Internal Bus Transceiver compliant with LIN Bus Specifications 1.3, 2.0 and 2.1, and compliant to SAE J2602:
  - Support Baud Rates up to 20 Kbaud
  - 43V load dump protected
  - Very low EMI meets stringent OEM requirements
  - Wide supply voltage, 7.0V-30.0V continuous
  - Internal bus pull-up resistor and diode
  - Protected against ground shorts
  - Protected against loss of ground
  - High current drive
  - Automatic thermal shutdown
- Extended Temperature Range: -40 to +125°C

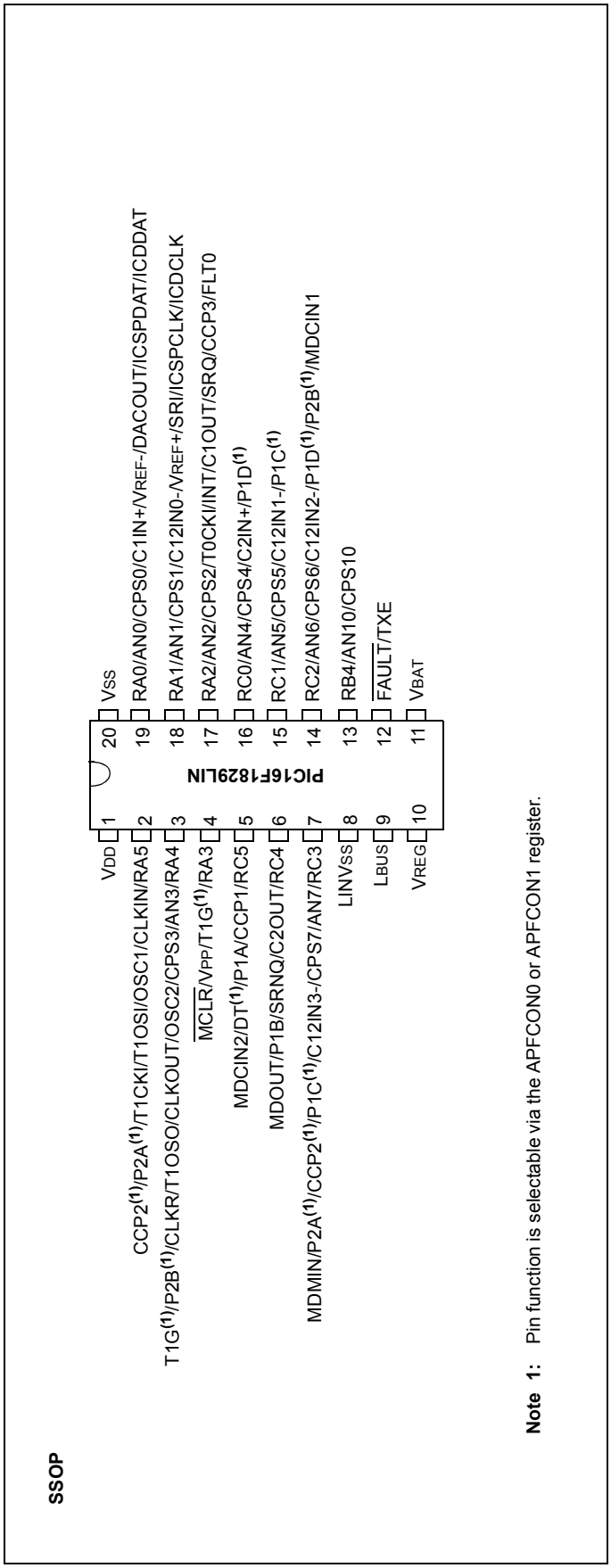
PIC16F1829LIN Device Overview

Device	Program Memory	Data Memory		I/Os(1)	10-bit ADC (ch)	Cap Sense (ch)	Comparators	Timers (8/16-bit)	EUSART(2)	ECCP (Full-Bridge)	ECCP (Half-Bridge)	CCP	SR Latch	Other Features
	Words	SRAM (bytes)	Data EEPROM (bytes)											
PIC16F1829LIN	8K	1024	256	13	9	12	2	4/1	1	1	1	1(3)	Yes	LIN/J2602 Transceiver, Voltage Regulator

Note 1: One pin is input-only.
2: EUSART dedicated to LIN communications.
3: One CCP only available internally.

FIGURE 1: 20-PIN DIAGRAM FOR PIC16F1829LIN

SSOP



Note 1: Pin function is selectable via the APFCON0 or APFCON1 register.

TABLE 1-1: PIC16F1829LIN PIN SUMMARY

I/O	20-Pin SSOP	A/D	Reference	Cap Sense	Comparator	SR Latch	Timers	CCP	EUSART	Interrupt	Modulator	Pull-up	Basic
RA0	19	AN0	VREF- DACOUT	CPS0	C1IN+	—	—	—	—	IOC	—	Y	ICSPDAT/ ICDDAT
RA1	18	AN1	VREF+	CPS1	C12IN0-	SRI	—	—	—	IOC	—	Y	ICSPCLK/ ICDCLK
RA2	17	AN2	—	CPS2	C1OUT	SRQ	T0CKI	CCP3 FLT0	—	INT/ IOC	—	Y	—
RA3	4	—	—	—	—	—	T1G(1)	—	—	IOC	—	Y(4)	$\overline{\text{MCLR}}$ VPP
RA4	3	AN3	—	CPS3	—	—	T1G(1) T1OSO	P2B(1)	—	IOC	—	Y	OSC2 CLKOUT CLKR
RA5	2	—	—	—	—	—	T1CKI T1OSI	CCP2(1) P2A(1)	—	IOC	—	Y	OSC1 CLKIN
RB4	13	AN10	—	CPS10	—	—	—	—	—	IOC	—	Y	—
RB5	(2)	—	—	—	—	—	—	—	RX(1)	—	—	Y	—
RB6	(2)	—	—	—	—	—	—	—	—	—	—	Y	$\overline{\text{CS}}$/LWAKE
RB7	(2)	—	—	—	—	—	—	—	TX(1)	—	—	Y	—
RC0	16	AN4	—	CPS4	C2IN+	—	—	P1D(1)	—	—	—	Y	—
RC1	15	AN5	—	CPS5	C12IN1-	—	—	P1C(1)	—	—	—	Y	—
RC2	14	AN6	—	CPS6	C12IN2-	—	—	P1D(1) P2B(1)	—	—	MDCIN1	Y	—
RC3	7	AN7	—	CPS7	C12IN3-	—	—	P1C(1) CCP2(1) P2A(1)	—	—	MDMIN	Y	—
RC4	6	—	—	—	C2OUT	SRNQ	—	P1B	—	—	MDOUT	Y	—
RC5	5	—	—	—	—	—	—	CCP1 P1A	—	—	MDCIN2	Y	—
RC6	—	—	—	—	—	—	—	—	—	—	—	—	No connection
RC7	(2)	—	—	—	—	—	—	—	—	—	—	Y	POWERGOOD input from Voltage Regulator
$\overline{\text{FAULT}}$ /TXE	12	—	—	—	—	—	—	—	—	—	—	—	—
VBAT	11	—	—	—	—	—	—	—	—	—	—	—	—
VREG	10	—	—	—	—	—	—	—	—	—	—	—	—
LBUS	9	—	—	—	—	—	—	—	—	—	—	—	—
VDD	1	—	—	—	—	—	—	—	—	—	—	—	VDD
Vss	20	—	—	—	—	—	—	—	—	—	—	—	Vss
Vss	8	—	—	—	—	—	—	—	—	—	—	—	LIN Vss

Note 1: Pin function is selectable via the APFCON0 or APFCON1 register.
2: Internal connection. No associated external pin.

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NOTES:

1.0 DEVICE OVERVIEW

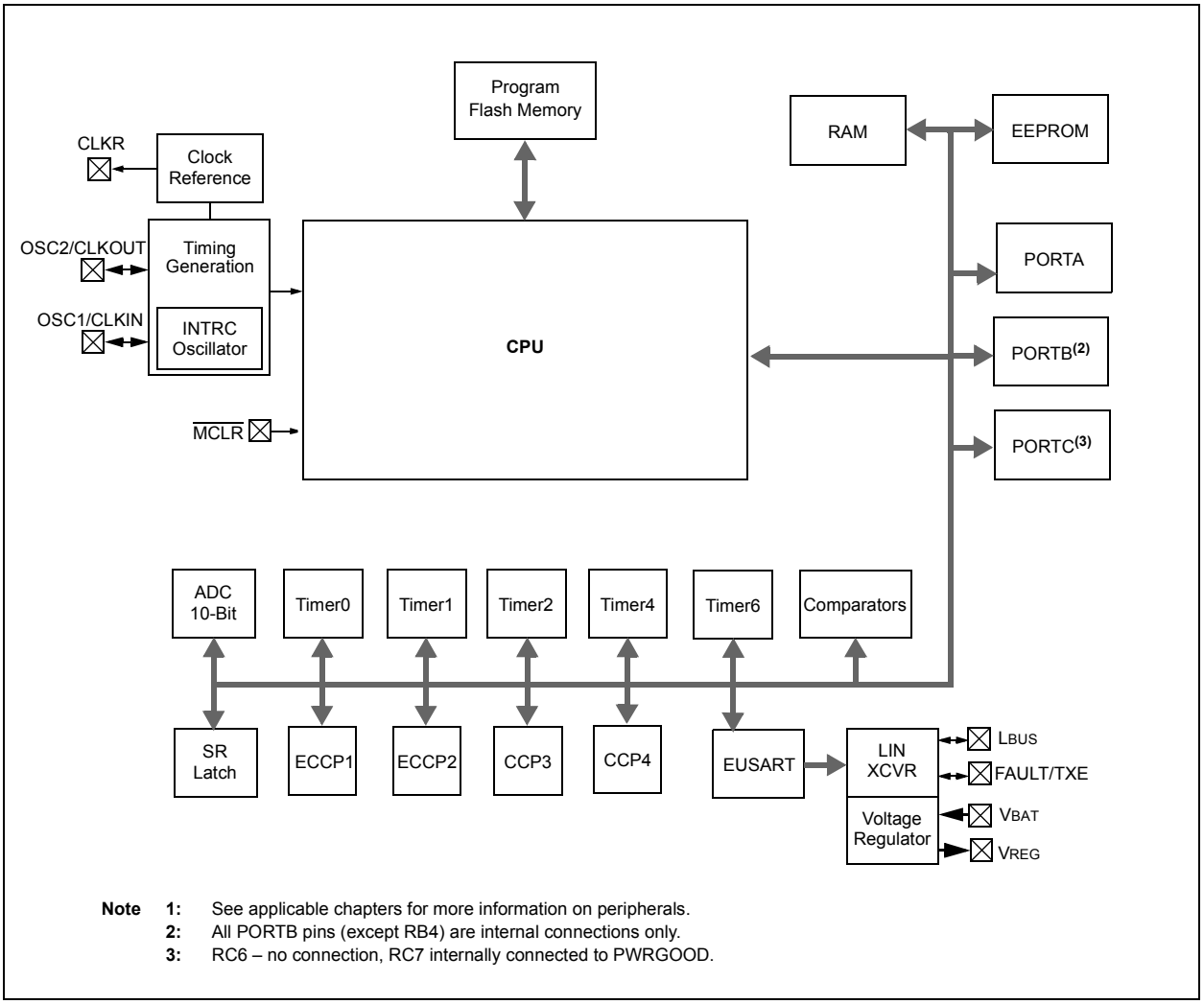
The PIC16F1829LIN is described within this data sheet. It is available in 20-pin SSOP package. Figure 1-1 shows a block diagram of the PIC16F1829LIN device. Tables 1-1 and 1-2 show the pinout description.

Refer to Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16F1829LIN
ADC		•
Capacitive Sensing (CPS) Module		•
Data EEPROM		•
Digital-to-Analog Converter (DAC)		•
Digital Signal Modulator (DSM)		•
EUSART		•
Fixed Voltage Reference (FVR)		•
SR Latch		•
Capture/Compare/PWM Modules		
	ECCP1	•
	ECCP2	•
	CCP3	•
Comparators		
	C1	•
	C2	•
Timers		
	Timer0	•
	Timer1	•
	Timer2	•
	Timer4	•
	Timer6	•

FIGURE 1-1: PIC16F1829LIN BLOCK DIAGRAM(1)



Note 1: See applicable chapters for more information on peripherals.
2: All PORTB pins (except RB4) are internal connections only.
3: RC6 – no connection, RC7 internally connected to PWRGOOD.

TABLE 1-2: PIC16F1829LIN PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/CPS0/C1IN+/VREF-/ DACOUT/ICSPDAT/ICDDAT	RA0	TTL	CMOS	General purpose I/O.
	AN0	AN	—	A/D Channel 0 input.
	CPS0	AN	—	Capacitive sensing input 0.
	C1IN+	AN	—	Comparator C1 positive input.
	VREF-	AN	—	A/D and DAC Negative Voltage Reference input.
	DACOUT	—	AN	Digital-to-Analog Converter output.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
	ICDDAT	ST	CMOS	In-Circuit Data I/O.
RA1/AN1/CPS1/C12IN0-/VREF+/ SRI/ICSPCLK/ICDCLK	RA1	TTL	CMOS	General purpose I/O.
	AN1	AN	—	A/D Channel 1 input.
	CPS1	AN	—	Capacitive sensing input 1.
	C12IN0-	AN	—	Comparator C1 or C2 negative input.
	VREF+	AN	—	A/D and DAC Positive Voltage Reference input.
	SRI	ST	—	SR latch input.
	ICSPCLK	ST	—	Serial Programming Clock.
	ICDCLK	ST	—	In-Circuit Debug Clock.
RA2/AN2/CPS2/T0CKI/INT/ C1OUT/SRQ/CCP3/FLT0	RA2	ST	CMOS	General purpose I/O.
	AN2	AN	—	A/D Channel 2 input.
	CPS2	AN	—	Capacitive sensing input 2.
	T0CKI	ST	—	Timer0 clock input.
	INT	ST	—	External interrupt.
	C1OUT	—	CMOS	Comparator C1 output.
	SRQ	—	CMOS	SR latch non-inverting output.
	CCP3	ST	CMOS	Capture/Compare/PWM 3.
	FLT0	ST	—	ECCP Auto-Shutdown Fault input.
RA3/T1G(1)/VPP/$\overline{MCLR}$	RA3	TTL	—	General purpose input.
	T1G	ST	—	Timer1 gate input.
	VPP	HV	—	Programming voltage.
	$\overline{MCLR}$	ST	—	Master Clear with internal pull-up.
RA4/AN3/CPS3/OSC2/ CLKOUT/T1OSO/CLKR P2B(1)/T1G(1,2)	RA4	TTL	CMOS	General purpose I/O.
	AN3	AN	—	A/D Channel 3 input.
	CPS3	AN	—	Capacitive sensing input 3.
	OSC2	—	CMOS	Comparator C2 output.
	CLKOUT	—	CMOS	FOSC/4 output.
	T1OSO	XTAL	XTAL	Timer1 oscillator connection.
	CLKR	—	CMOS	Clock Reference output.
	P2B	—	CMOS	PWM output.
	T1G	ST	—	Timer1 gate input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C™ = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin functions can be moved using the APFCON0 or APFCON1 register.
2: Default function location.
3: Internal Connection. No associated external pin.

TABLE 1-2: PIC16F1829LIN PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA5/CLKIN/OSC1/T1OSI/ T1CKI/P2A(1)/CCP2(1)	RA5	TTL	CMOS	General purpose I/O.
	CLKIN	CMOS	—	External clock input (EC mode).
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	T1OSI	XTAL	XTAL	Timer1 oscillator connection.
	T1CKI	ST	—	Timer1 clock input.
	P2A	—	CMOS	PWM output.
	CCP2	ST	CMOS	Capture/Compare/PWM 2.
RB4/AN10/CPS10	RB4	TTL	CMOS	General purpose I/O.
	AN10	AN	—	A/D Channel 10 input.
	CPS10	AN	—	Capacitive sensing input 10.
RB5(3)/RX(1,2)/	RB5	TTL	CMOS	General purpose I/O.
	RX	ST	—	USART asynchronous input.
RB6(3)/$\overline{CS}$/LWAKE	RB6	TTL	CMOS	General purpose I/O.
	$\overline{CS}$/ LWAKE	TTL	OD	LIN Transceiver Chip Select and Wake-up.
RB7(3)/TX(1,2)	RB7	TTL	CMOS	General purpose I/O.
	TX	—	CMOS	USART asynchronous transmit.
RC0/AN4/CPS4/C2IN+/P1D(1)	RC0	TTL	CMOS	General purpose I/O.
	AN4	AN	—	A/D Channel 4 input.
	CPS4	AN	—	Capacitive sensing input 4.
	C2IN+	AN	—	Comparator C2 positive input.
	P1D	—	CMOS	PWM output.
RC1/AN5/CPS5/C12IN1-/P1C(1)	RC1	TTL	CMOS	General purpose I/O.
	AN5	AN	—	A/D Channel 5 input.
	CPS5	AN	—	Capacitive sensing input 5.
	C12IN1-	AN	—	Comparator C1 or C2 negative input.
	P1C	—	CMOS	PWM output.
RC2/AN6/CPS6/C12IN2-/ P1D(1,2)/P2B(1,2)/MDCIN1	RC2	TTL	CMOS	General purpose I/O.
	AN6	AN	—	A/D Channel 6 input.
	CPS6	AN	—	Capacitive sensing input 6.
	C12IN2-	AN	—	Comparator C1 or C2 negative input.
	P1D	—	CMOS	PWM output.
	P2B	—	CMOS	PWM output.
	MDCIN1	ST	—	Modulator Carrier Input 1.
RC3/AN7/CPS7/C12IN3-/ P2A(1,2)/CCP2(1,2)/P1C(1,2)/ MDMIN	RC3	TTL	CMOS	General purpose I/O.
	AN7	AN	—	A/D Channel 7 input.
	CPS7	AN	—	Capacitive sensing input 7.
	C12IN3-	AN	—	Comparator C1 or C2 negative input.
	P2A	—	CMOS	PWM output.
	CCP2	AN	—	Capacitive sensing input 2.
	P1C	—	CMOS	PWM output.
	MDMIN	ST	—	Modulator source input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C™ = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin functions can be moved using the APFCON0 or APFCON1 register.
2: Default function location.
3: Internal Connection. No associated external pin.

TABLE 1-2: PIC16F1829LIN PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC4/C2OUT/SRNQ/P1B/ MDOUT	RC4	TTL	CMOS	General purpose I/O.
	C2OUT	—	CMOS	Comparator C2 output.
	SRNQ	—	CMOS	SR latch inverting output.
	P1B	—	CMOS	PWM output.
	MDOUT	—	CMOS	Modulator output.
RC5/P1A/CCP1// MDCIN2	RC5	TTL	CMOS	General purpose I/O.
	P1A	—	CMOS	PWM output.
	CCP1	ST	CMOS	Capture/Compare/PWM 1.
	MDCIN2	ST	—	Modulator Carrier Input 2.
RC6	RC6	—	—	No connection.
RC7/POWERGOOD	RC7	TTL	—	POWERGOOD input from voltage regulator.
$\overline{\text{FAULT}}$/TXE	—	TTL	OD	LIN Fault Indicator and Transmitter Enable.
VBAT	Battery Supply	Power	—	Battery voltage input to the LIN Transceiver and the voltage regulator.
VREG	Regulator Output	—	Power	Regulated 5.0V output.
LBUS	Network Bus	HV	HV	LIN/J2602 bus network connection.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.
LIN VSS	VSS	Power	—	Ground reference for voltage regulator and LIN bus.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C™ = Schmitt Trigger input with I^2C levels
HV = High Voltage XTAL = Crystal

Note 1: Pin functions can be moved using the APFCON0 or APFCON1 register.
2: Default function location.
3: Internal Connection. No associated external pin.

NOTES:

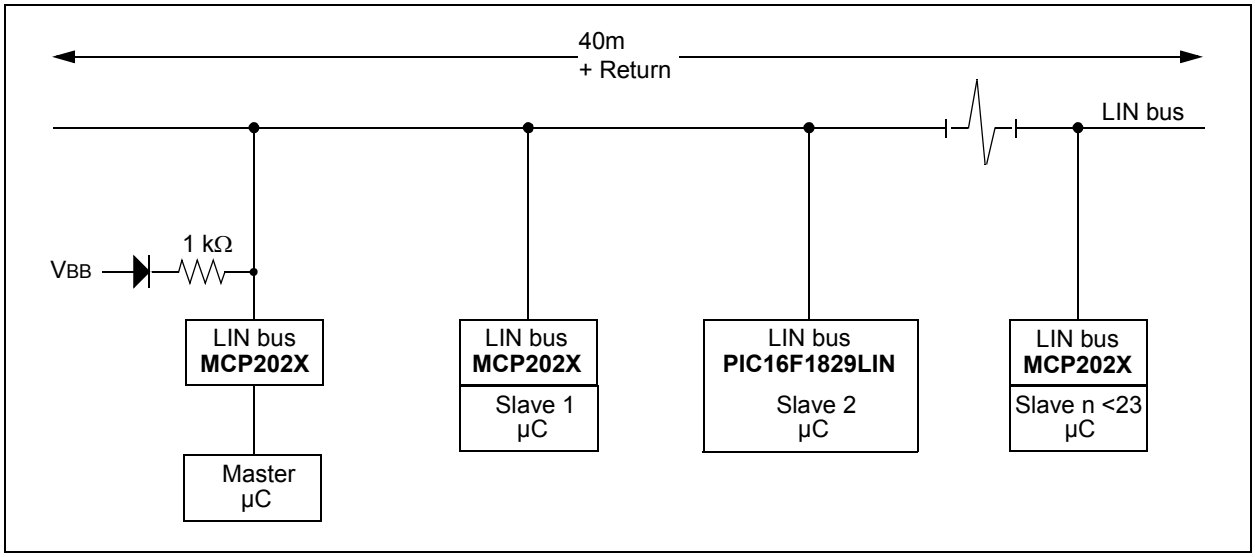
2.0 USING THE PIC16F1829LIN IN LIN BUS APPLICATIONS

Note:	Failure to follow the recommended setup and initialization may result in improper or unknown LIN operation.

2.1 Hardware

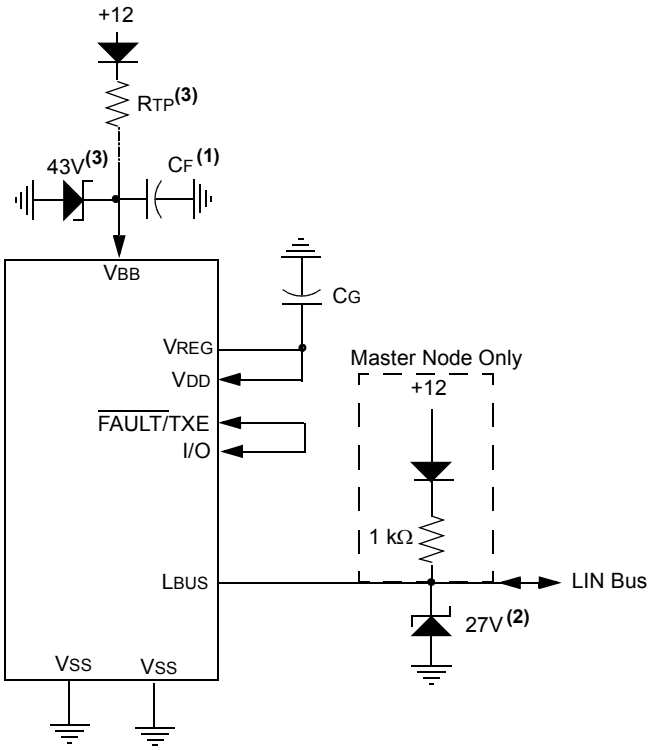
The PIC16F1829LIN internal connections are optimized to reduce the number of components in a typical LIN/J2602 node in a LIN bus system. Some features and modules of the stand-alone PIC16F1829 are no longer available or their functionality has changed.

FIGURE 2-1: TYPICAL LIN NETWORK CONFIGURATION



For this reason, the following figure (Figure 2-2) is a recommended block diagram. Note that the microcontroller is powered by the internal voltage regulator and an external connection must be made between V_{REG} and V_{BB} along with a load capacitor. $\overline{FAULT}$/TXE can be monitored or controlled by any I/O pin.

FIGURE 2-2: TYPICAL PIC16F1829LIN APPLICATION



Note 1: CF is the filter capacitor for the external voltage supply.

2: Transient suppressor diode. VCLAMP L = 27V.

3: These components are required for additional load dump protection above 43V.

2.2 Software

Please refer to the sections of this data sheet to determine what facilities have changed and what register values need to be properly initialized. Failure to follow these guidelines may result in improper operation.

2.2.1 TYPICAL INITIALIZATION CODE

```
InitialiseIOports
        banksel ANSELH
        MOVLW   0x04            ;disable AN8:9,11
        ANDWF   ANSELH,f
        banksel TRISB
        MOVLW   0xC0            ;PORTB7:6 must be inputs
        IORWF   TRISB,f
        MOVLW   0xCF            ;PORTB5:4 must be outputs
        ANDWF   TRISB,f
        MOVLW   0x80
        IORWF   TRISC,f         ;PORTC7 is an input
        banksel LATB
        BSF     LINCS           ;Chip Select Transceiver
        RETURN

SetupLINUSART
        banksel RCSTA
        MOVLW   B'10010000'     ;UART enabled,8-bit,continuous receive
        MOVWF   RCSTA
        MOVLW   B'00000100'     ;8-bit, asynchronous, high-baudrate
        MOVWF   TXSTA
        MOVLW   B'00001000'     ;16-bit Baud Rate Generator
        MOVWF   BAUDCON
        CLRF    SPBRGH
        MOVLW   0x31            ;setup initially for 20KBaud @ 4.0MHz, BRGH=1, BRG16=1
        MOVWF   SPBRG
        banksel LATB
        BSF     LINCS           ;to enable transceiver
        RETURN
```

2.2.2 SAMPLE TRANSMIT SOFTWARE

This routine is called when PIR1<TXIF> = 1:

```
PutDATAbyte
        banksel TXREG
        MOVF    INDF0,w                 ; copy data byte into w-register
        MOVWF   TXREG
        INCF    FSR0, f                 ; point to next location
        DECFSZ  MESSAGE_COUNTER, f      ; decrement Message Counter by one
        RETURN
```

2.2.3 SAMPLE RECEIVE SOFTWARE

The following routines are called when PIR1<RCIF> = 1:

```
GetBREAK
        banksel RCSTA
        BTFSS   RCSTA,FERR      ; was BREAK character longer than 8 bits?
        GOTO    BadBREAKchar    ; no, not a valid BREAK, too short
        MOVF    RCREG,w         ; dump break character, reset RCIF and FERR
        BTFSS   STATUS,Z
        GOTO    BadBREAKchar    ; no, not a valid BREAK, not zero
        DECF    MESSAGE_COUNTER
        banksel PORTB
        BTFSS   LINRX
        GOTO    $-2
        banksel BAUDCTL
        BSF     BAUDCTL,ABDEN   ; enable AutoBaud
        RETURN
BadBREAKchar
        MOVF    RCREG,w         ; dump break character, reset RCIF and FERR
        RETURN

GetSYNC
        banksel BAUDCTL
        BTFSC   BAUDCTL,ABDOVF; did baud rate generator overflow?
        GOTO    BadSYNCchar; yes, bad sync character
        BTFSC   RCSTA,FERR; was there a Framing Error?
        GOTO    BadSYNCchar; yes, bad sync character
        DECF    SPBRG
        MOVF    RCREG,w         ; dump sync character, reset RCIF
        DECF    MESSAGE_COUNTER
        RETURN
BadSYNCchar
        BCF     BAUDCTL,ABDOVF; clear the overflow condition
        MOVLW   .12             ; reset the state machine
        MOVWF   MESSAGE_COUNTER
        RETURN

GetDATAbyte
        banksel RCREG
        MOVF    RCREG,w         ; get character, reset RCIF and FERR
        MOVWF   RXTX_REG        ; copy data into w-register
        MOVWF   INDF0           ; copy data into data area
        INCF    FSR0, f         ; point to next location
        DECF    MESSAGE_COUNTER, f ; decrement number of bytes to receive by one
        RETURN
```


2.3 Routing CCP4 to a Pin

Normally, CCP4 uses RC6 as an output pin. This pin is not available on the PIC16F1829LIN. This output function can be re-routed to RC4, through the Data Signal Modulator (DSM), as shown below.

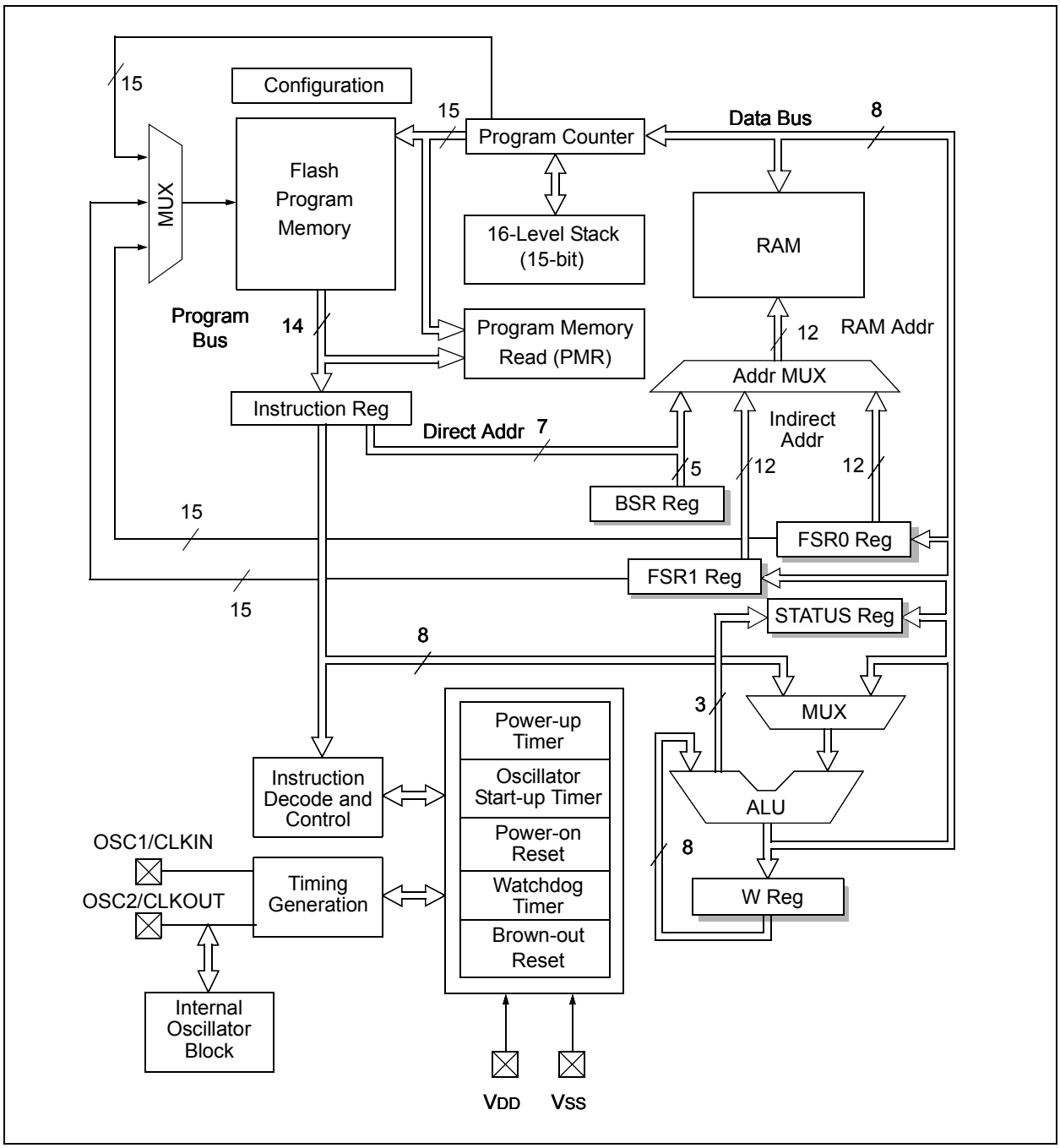
```
; Setup CCP4
    banksel PR2
    movlw   0xFF        ; set PWM for highest resolution
    movwf   PR2
    banksel CCP4CON
    movlw   b'00001100'; set for PWM mode
    movwf   CCP4CON
    movlw   0x80        ; preload the duty cycle with a value
    movwf   CCPR4L
    banksel CCPTMRS
    movlw   0x00        ; set Timer2 as clock source
    movwf   CCPTMRS
    banksel PIR1
    bcf     PIR1,TMR2IF; clear timer overflow flag
    movlw   b'00000101'; clock prescaler = 4
    movwf   T2CON
    bsf     T2CON,TMR2ON; turn on Timer 2
; Setup DSM to route CCP4 to RC4
    banksel MDCON
    movlw   b'11000000'; enable DSM, enable output pin
    movwf   MDCON
    movlw   0x00        ; modulation controlled by MCBIT
    movwf   MDSRC
    movlw   0x87        ; select CCP4 as carrier frequency and disable RC6
    movwf   MDCARL
    movwf   MDCARH      ; modulation source does not matter because high and low carriers are the
                        ; same.
```

NOTES:

3.0 ENHANCED MID-RANGE CPU

See *"PIC16(L)F1825/1829 Data Sheet"* (DS41440) for description of the enhanced mid-range 8-bit CPU core.

FIGURE 3-1: CORE BLOCK DIAGRAM



NOTES:

4.0 MEMORY ORGANIZATION

See *"PIC16(L)F1825/1829 Data Sheet"* (DS41440) for descriptions of Program memory, Data RAM and Data EEPROM.

TABLE 4-1: PIC16F1829LIN MEMORY MAP, BANKS 0-7

	BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7
000h	INDF0	080h	INDF0	100h	INDF0	180h	INDF0	200h	INDF0	280h	INDF0	300h	INDF0	380h	INDF0
001h	INDF1	081h	INDF1	101h	INDF1	181h	INDF1	201h	INDF1	281h	INDF1	301h	INDF1	381h	INDF1
002h	PCL	082h	PCL	102h	PCL	182h	PCL	202h	PCL	282h	PCL	302h	PCL	382h	PCL
003h	STATUS	083h	STATUS	103h	STATUS	183h	STATUS	203h	STATUS	283h	STATUS	303h	STATUS	383h	STATUS
004h	FSR0L	084h	FSR0L	104h	FSR0L	184h	FSR0L	204h	FSR0L	284h	FSR0L	304h	FSR0L	384h	FSR0L
005h	FSR0H	085h	FSR0H	105h	FSR0H	185h	FSR0H	205h	FSR0H	285h	FSR0H	305h	FSR0H	385h	FSR0H
006h	FSR1L	086h	FSR1L	106h	FSR1L	186h	FSR1L	206h	FSR1L	286h	FSR1L	306h	FSR1L	386h	FSR1L
007h	FSR1H	087h	FSR1H	107h	FSR1H	187h	FSR1H	207h	FSR1H	287h	FSR1H	307h	FSR1H	387h	FSR1H
008h	BSR	088h	BSR	108h	BSR	188h	BSR	208h	BSR	288h	BSR	308h	BSR	388h	BSR
009h	WREG	089h	WREG	109h	WREG	189h	WREG	209h	WREG	289h	WREG	309h	WREG	389h	WREG
00Ah	PCLATH	08Ah	PCLATH	10Ah	PCLATH	18Ah	PCLATH	20Ah	PCLATH	28Ah	PCLATH	30Ah	PCLATH	38Ah	PCLATH
00Bh	INTCON	08Bh	INTCON	10Bh	INTCON	18Bh	INTCON	20Bh	INTCON	28Bh	INTCON	30Bh	INTCON	38Bh	INTCON
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	WPUA	28Ch	—	30Ch	—	38Ch	INLVLA
00Dh	**PORTB**	08Dh	**TRISB**	10Dh	LATB	18Dh	ANSELB	20Dh	WPUB	28Dh	—	30Dh	—	38Dh	INLVLB
00Eh	**PORTC**	08Eh	**TRISC**	10Eh	LATC	18Eh	ANSELC	20Eh	WPUC	28Eh	—	30Eh	—	38Eh	INLVLC
00Fh	—	08Fh	—	10Fh	—	18Fh	—	20Fh	—	28Fh	—	30Fh	—	38Fh	—
010h	—	090h	—	110h	—	190h	—	210h	—	290h	—	310h	—	390h	—
011h	**PIR1**	091h	**PIE1**	111h	CM1CON0	191h	EEADRL	211h	**SSP1BUF**	291h	CCPR1L	311h	CCPR3L	391h	IOCAP
012h	**PIR2**	092h	**PIE2**	112h	CM1CON1	192h	EEADRH	212h	**SSP1ADD**	292h	CCPR1H	312h	CCPR3H	392h	IOCAN
013h	—	093h	—	113h	CM2CON0	193h	EEDATL	213h	**SSP1MSK**	293h	CCP1CON	313h	CCP3CON	393h	IOCAF
014h	—	094h	—	114h	CM2CON1	194h	EEDATH	214h	**SSP1STAT**	294h	PWM1CON	314h	—	394h	**IOCBP**
015h	TMR0	095h	OPTION_REG	115h	CMOUT	195h	EECON1	215h	**SSP1CON**	295h	CCP1AS	315h	—	395h	**IOCBN**
016h	TMR1L	096h	PCON	116h	BORCON	196h	EECON2	216h	**SSP1CON2**	296h	PSTR1CON	316h	—	396h	**IOCBF**
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h	—	217h	**SSP1CON3**	297h	—	317h	—	397h	—
018h	T1CON	098h	OSCTUNE	118h	DACCON0	198h	—	218h	—	298h	CCPR2L	318h	**CCPR4L**	398h	—
019h	T1GCON	099h	OSCCON	119h	DACCON1	199h	RCREG	219h	**SSP2BUF**	299h	CCPR2H	319h	**CCPR4H**	399h	—
01Ah	TMR2	09Ah	OSCSTAT	11Ah	SRCON0	19Ah	TXREG	21Ah	**SSP2ADD**	29Ah	CCP2CON	31Ah	**CCP4CON**	39Ah	CLKRCON
01Bh	PR2	09Bh	ADRESL	11Bh	SRCON1	19Bh	SPBRGL	21Bh	**SSP2MSK**	29Bh	PWM2CON	31Bh	—	39Bh	—
01Ch	T2CON	09Ch	ADRESH	11Ch	—	19Ch	SPBRGH	21Ch	**SSP2STAT**	29Ch	CCP2AS	31Ch	—	39Ch	MDCON
01Dh	—	09Dh	ADCON0	11Dh	**APFCON0**	19Dh	**RCSTA**	21Dh	**SSP2CON**	29Dh	PSTR2CON	31Dh	—	39Dh	MDSRC
01Eh	CPSCON0	09Eh	ADCON1	11Eh	**APFCON1**	19Eh	**TXSTA**	21Eh	**SSP2CON2**	29Eh	CCPTMRS	31Eh	—	39Eh	MDCARL
01Fh	CPSCON1	09Fh	—	11Fh	—	19Fh	**BAUDCON**	21Fh	**SSP2CON3**	29Fh	—	31Fh	—	39Fh	MDCARH
020h	General Purpose Register 96 Bytes	0A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h	General Purpose Register 80 Bytes	220h	General Purpose Register 80 Bytes	2A0h	General Purpose Register 80 Bytes	320h	General Purpose Register 80 Bytes	3A0h	General Purpose Register 80 Bytes
06Fh		0EFh		16Fh		1EFh		26Fh		2EFh		36Fh		3EFh	
070h		0F0h	Accesses 70h – 7Fh	170h	Accesses 70h – 7Fh	1F0h	Accesses 70h – 7Fh	270h	Accesses 70h – 7Fh	2F0h	Accesses 70h – 7Fh	370h	Accesses 70h – 7Fh	3F0h	Accesses 70h – 7Fh
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		37Fh		3FFh	

Legend: = Unimplemented data memory locations, read as '0'

Note 1: Registers in bold have functional differences. Please refer to the appropriate chapters for details.

TABLE 4-2: PIC16F1829LIN MEMORY MAP, BANKS 8-15

BANK 8		BANK 9		BANK 10		BANK 11		BANK 12		BANK 13		BANK 14		BANK 15	
400h	INDF0	480h	INDF0	500h	INDF0	580h	INDF0	600h	INDF0	680h	INDF0	700h	INDF0	780h	INDF0
401h	INDF1	481h	INDF1	501h	INDF1	581h	INDF1	601h	INDF1	681h	INDF1	701h	INDF1	781h	INDF1
402h	PCL	482h	PCL	502h	PCL	582h	PCL	602h	PCL	682h	PCL	702h	PCL	782h	PCL
403h	STATUS	483h	STATUS	503h	STATUS	583h	STATUS	603h	STATUS	683h	STATUS	703h	STATUS	783h	STATUS
404h	FSR0L	484h	FSR0L	504h	FSR0L	584h	FSR0L	604h	FSR0L	684h	FSR0L	704h	FSR0L	784h	FSR0L
405h	FSR0H	485h	FSR0H	505h	FSR0H	585h	FSR0H	605h	FSR0H	685h	FSR0H	705h	FSR0H	785h	FSR0H
406h	FSR1L	486h	FSR1L	506h	FSR1L	586h	FSR1L	606h	FSR1L	686h	FSR1L	706h	FSR1L	786h	FSR1L
407h	FSR1H	487h	FSR1H	507h	FSR1H	587h	FSR1H	607h	FSR1H	687h	FSR1H	707h	FSR1H	787h	FSR1H
408h	BSR	488h	BSR	508h	BSR	588h	BSR	608h	BSR	688h	BSR	708h	BSR	788h	BSR
409h	WREG	489h	WREG	509h	WREG	589h	WREG	609h	WREG	689h	WREG	709h	WREG	789h	WREG
40Ah	PCLATH	48Ah	PCLATH	50Ah	PCLATH	58Ah	PCLATH	60Ah	PCLATH	68Ah	PCLATH	70Ah	PCLATH	78Ah	PCLATH
40Bh	INTCON	48Bh	INTCON	50Bh	INTCON	58Bh	INTCON	60Bh	INTCON	68Bh	INTCON	70Bh	INTCON	78Bh	INTCON
40Ch	—	48Ch	—	50Ch	—	58Ch	—	60Ch	—	68Ch	—	70Ch	—	78Ch	—
40Dh	—	48Dh	—	50Dh	—	58Dh	—	60Dh	—	68Dh	—	70Dh	—	78Dh	—
40Eh	—	48Eh	—	50Eh	—	58Eh	—	60Eh	—	68Eh	—	70Eh	—	78Eh	—
40Fh	—	48Fh	—	50Fh	—	58Fh	—	60Fh	—	68Fh	—	70Fh	—	78Fh	—
410h	—	490h	—	510h	—	590h	—	610h	—	690h	—	710h	—	790h	—
411h	—	491h	—	511h	—	591h	—	611h	—	691h	—	711h	—	791h	—
412h	—	492h	—	512h	—	592h	—	612h	—	692h	—	712h	—	792h	—
413h	—	493h	—	513h	—	593h	—	613h	—	693h	—	713h	—	793h	—
414h	—	494h	—	514h	—	594h	—	614h	—	694h	—	714h	—	794h	—
415h	TMR4	495h	—	515h	—	595h	—	615h	—	695h	—	715h	—	795h	—
416h	PR4	496h	—	516h	—	596h	—	616h	—	696h	—	716h	—	796h	—
417h	T4CON	497h	—	517h	—	597h	—	617h	—	697h	—	717h	—	797h	—
418h	—	498h	—	518h	—	598h	—	618h	—	698h	—	718h	—	798h	—
419h	—	499h	—	519h	—	599h	—	619h	—	699h	—	719h	—	799h	—
41Ah	—	49Ah	—	51Ah	—	59Ah	—	61Ah	—	69Ah	—	71Ah	—	79Ah	—
41Bh	—	49Bh	—	51Bh	—	59Bh	—	61Bh	—	69Bh	—	71Bh	—	79Bh	—
41Ch	TMR6	49Ch	—	51Ch	—	59Ch	—	61Ch	—	69Ch	—	71Ch	—	79Ch	—
41Dh	PR6	49Dh	—	51Dh	—	59Dh	—	61Dh	—	69Dh	—	71Dh	—	79Dh	—
41Eh	T6CON	49Eh	—	51Eh	—	59Eh	—	61Eh	—	69Eh	—	71Eh	—	79Eh	—
41Fh	—	49Fh	—	51Fh	—	59Fh	—	61Fh	—	69Fh	—	71Fh	—	79Fh	—
420h	General Purpose Register 80 Bytes	4A0h	General Purpose Register 80 Bytes	520h	General Purpose Register 80 Bytes	5A0h	General Purpose Register 80 Bytes	620h	General Purpose Register 48 Bytes	6A0h	Unimplemented Read as '0'	720h	Unimplemented Read as '0'	7A0h	Unimplemented Read as '0'
46Fh		4EFh		56Fh		5EFh		64Fh		6EFh		76Fh		7EFh	
								650h	Unimplemented Read as '0'						
								66Fh							
470h	Accesses 70h – 7Fh	4F0h	Accesses 70h – 7Fh	570h	Accesses 70h – 7Fh	5F0h	Accesses 70h – 7Fh	670h	Accesses 70h – 7Fh	6F0h	Accesses 70h – 7Fh	770h	Accesses 70h – 7Fh	7F0h	Accesses 70h – 7Fh
47Fh		4FFh		57Fh		5FFh		67Fh		6FFh		77Fh		7FFh	

Legend: = Unimplemented data memory locations, read as '0'

Note 1: Registers in bold have functional differences. Please refer to the appropriate chapters for details.

TABLE 4-3: PIC16F1829LIN MEMORY MAP, BANKS 16-23

	BANK 16		BANK 17		BANK 18		BANK 19		BANK 20		BANK 21		BANK 22		BANK 23	
800h	INDF0	880h	INDF0	900h	INDF0	980h	INDF0	A00h	INDF0	A80h	INDF0	B00h	INDF0	B80h	INDF0
801h	INDF1	881h	INDF1	901h	INDF1	981h	INDF1	A01h	INDF1	A81h	INDF1	B01h	INDF1	B81h	INDF1
802h	PCL	882h	PCL	902h	PCL	982h	PCL	A02h	PCL	A82h	PCL	B02h	PCL	B82h	PCL
803h	STATUS	883h	STATUS	903h	STATUS	983h	STATUS	A03h	STATUS	A83h	STATUS	B03h	STATUS	B83h	STATUS
804h	FSR0L	884h	FSR0L	904h	FSR0L	984h	FSR0L	A04h	FSR0L	A84h	FSR0L	B04h	FSR0L	B84h	FSR0L
805h	FSR0H	885h	FSR0H	905h	FSR0H	985h	FSR0H	A05h	FSR0H	A85h	FSR0H	B05h	FSR0H	B85h	FSR0H
806h	FSR1L	886h	FSR1L	906h	FSR1L	986h	FSR1L	A06h	FSR1L	A86h	FSR1L	B06h	FSR1L	B86h	FSR1L
807h	FSR1H	887h	FSR1H	907h	FSR1H	987h	FSR1H	A07h	FSR1H	A87h	FSR1H	B07h	FSR1H	B87h	FSR1H
808h	BSR	888h	BSR	908h	BSR	988h	BSR	A08h	BSR	A88h	BSR	B08h	BSR	B88h	BSR
809h	WREG	889h	WREG	909h	WREG	989h	WREG	A09h	WREG	A89h	WREG	B09h	WREG	B89h	WREG
80Ah	PCLATH	88Ah	PCLATH	90Ah	PCLATH	98Ah	PCLATH	A0Ah	PCLATH	A8Ah	PCLATH	B0Ah	PCLATH	B8Ah	PCLATH
80Bh	INTCON	88Bh	INTCON	90Bh	INTCON	98Bh	INTCON	A0Bh	INTCON	A8Bh	INTCON	B0Bh	INTCON	B8Bh	INTCON
80Ch	—	88Ch	—	90Ch	—	98Ch	—	A0Ch	—	A8Ch	—	B0Ch	—	B8Ch	—
80Dh	—	88Dh	—	90Dh	—	98Dh	—	A0Dh	—	A8Dh	—	B0Dh	—	B8Dh	—
80Eh	—	88Eh	—	90Eh	—	98Eh	—	A0Eh	—	A8Eh	—	B0Eh	—	B8Eh	—
80Fh	—	88Fh	—	90Fh	—	98Fh	—	A0Fh	—	A8Fh	—	B0Fh	—	B8Fh	—
810h	—	890h	—	910h	—	990h	—	A10h	—	A90h	—	B10h	—	B90h	—
811h	—	891h	—	911h	—	991h	—	A11h	—	A91h	—	B11h	—	B91h	—
812h	—	892h	—	912h	—	992h	—	A12h	—	A92h	—	B12h	—	B92h	—
813h	—	893h	—	913h	—	993h	—	A13h	—	A93h	—	B13h	—	B93h	—
814h	—	894h	—	914h	—	994h	—	A14h	—	A94h	—	B14h	—	B94h	—
815h	—	895h	—	915h	—	995h	—	A15h	—	A95h	—	B15h	—	B95h	—
816h	—	896h	—	916h	—	996h	—	A16h	—	A96h	—	B16h	—	B96h	—
817h	—	897h	—	917h	—	997h	—	A17h	—	A97h	—	B17h	—	B97h	—
818h	—	898h	—	918h	—	998h	—	A18h	—	A98h	—	B18h	—	B98h	—
819h	—	899h	—	919h	—	999h	—	A19h	—	A99h	—	B19h	—	B99h	—
81Ah	—	89Ah	—	91Ah	—	99Ah	—	A1Ah	—	A9Ah	—	B1Ah	—	B9Ah	—
81Bh	—	89Bh	—	91Bh	—	99Bh	—	A1Bh	—	A9Bh	—	B1Bh	—	B9Bh	—
81Ch	—	89Ch	—	91Ch	—	99Ch	—	A1Ch	—	A9Ch	—	B1Ch	—	B9Ch	—
81Dh	—	89Dh	—	91Dh	—	99Dh	—	A1Dh	—	A9Dh	—	B1Dh	—	B9Dh	—
81Eh	—	89Eh	—	91Eh	—	99Eh	—	A1Eh	—	A9Eh	—	B1Eh	—	B9Eh	—
81Fh	—	89Fh	—	91Fh	—	99Fh	—	A1Fh	—	A9Fh	—	B1Fh	—	B9Fh	—
820h 86Fh	Unimplemented Read as '0'	8A0h 8EFh	Unimplemented Read as '0'	920h 96Fh	Unimplemented Read as '0'	9A0h 9EFh	Unimplemented Read as '0'	A20h A6Fh	Unimplemented Read as '0'	AA0h AEFh	Unimplemented Read as '0'	B20h B6Fh	Unimplemented Read as '0'	BA0h BEFh	Unimplemented Read as '0'
870h 87Fh	Accesses 70h – 7Fh	8F0h 8FFh	Accesses 70h – 7Fh	970h 97Fh	Accesses 70h – 7Fh	9F0h 9FFh	Accesses 70h – 7Fh	A70h A7Fh	Accesses 70h – 7Fh	AF0h AFFh	Accesses 70h – 7Fh	B70h B7Fh	Accesses 70h – 7Fh	BF0h BFFh	Accesses 70h – 7Fh

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: Registers in bold have functional differences. Please refer to the appropriate chapters for details.

TABLE 4-4: PIC16F1829LIN MEMORY MAP, BANKS 24-31

	BANK 24		BANK 25		BANK 26		BANK 27		BANK 28		BANK 29		BANK 30		BANK 31	
C00h	INDF0	C80h	INDF0	D00h	INDF0	D80h	INDF0	E00h	INDF0	E80h	INDF0	F00h	INDF0	F80h	INDF0
C01h	INDF1	C81h	INDF1	D01h	INDF1	D81h	INDF1	E01h	INDF1	E81h	INDF1	F01h	INDF1	F81h	INDF1
C02h	PCL	C82h	PCL	D02h	PCL	D82h	PCL	E02h	PCL	E82h	PCL	F02h	PCL	F82h	PCL
C03h	STATUS	C83h	STATUS	D03h	STATUS	D83h	STATUS	E03h	STATUS	E83h	STATUS	F03h	STATUS	F83h	STATUS
C04h	FSR0L	C84h	FSR0L	D04h	FSR0L	D84h	FSR0L	E04h	FSR0L	E84h	FSR0L	F04h	FSR0L	F84h	FSR0L
C05h	FSR0H	C85h	FSR0H	D05h	FSR0H	D85h	FSR0H	E05h	FSR0H	E85h	FSR0H	F05h	FSR0H	F85h	FSR0H
C06h	FSR1L	C86h	FSR1L	D06h	FSR1L	D86h	FSR1L	E06h	FSR1L	E86h	FSR1L	F06h	FSR1L	F86h	FSR1L
C07h	FSR1H	C87h	FSR1H	D07h	FSR1H	D87h	FSR1H	E07h	FSR1H	E87h	FSR1H	F07h	FSR1H	F87h	FSR1H
C08h	BSR	C88h	BSR	D08h	BSR	D88h	BSR	E08h	BSR	E88h	BSR	F08h	BSR	F88h	BSR
C09h	WREG	C89h	WREG	D09h	WREG	D89h	WREG	E09h	WREG	E89h	WREG	F09h	WREG	F89h	WREG
C0Ah	PCLATH	C8Ah	PCLATH	D0Ah	PCLATH	D8Ah	PCLATH	E0Ah	PCLATH	E8Ah	PCLATH	F0Ah	PCLATH	F8Ah	PCLATH
C0Bh	INTCON	C8Bh	INTCON	D0Bh	INTCON	D8Bh	INTCON	E0Bh	INTCON	E8Bh	INTCON	F0Bh	INTCON	F8Bh	INTCON
C0Ch	—	C8Ch	—	D0Ch	—	D8Ch	—	E0Ch	—	E8Ch	—	F0Ch	—	F8Ch	See Table 4-5 for register mapping details
C0Dh	—	C8Dh	—	D0Dh	—	D8Dh	—	E0Dh	—	E8Dh	—	F0Dh	—	F8Dh	
C0Eh	—	C8Eh	—	D0Eh	—	D8Eh	—	E0Eh	—	E8Eh	—	F0Eh	—	F8Eh	
C0Fh	—	C8Fh	—	D0Fh	—	D8Fh	—	E0Fh	—	E8Fh	—	F0Fh	—	F8Fh	
C10h	—	C90h	—	D10h	—	D90h	—	E10h	—	E90h	—	F10h	—	F90h	
C11h	—	C91h	—	D11h	—	D91h	—	E11h	—	E91h	—	F11h	—	F91h	
C12h	—	C92h	—	D12h	—	D92h	—	E12h	—	E92h	—	F12h	—	F92h	
C13h	—	C93h	—	D13h	—	D93h	—	E13h	—	E93h	—	F13h	—	F93h	
C14h	—	C94h	—	D14h	—	D94h	—	E14h	—	E94h	—	F14h	—	F94h	
C15h	—	C95h	—	D15h	—	D95h	—	E15h	—	E95h	—	F15h	—	F95h	
C16h	—	C96h	—	D16h	—	D96h	—	E16h	—	E96h	—	F16h	—	F96h	
C17h	—	C97h	—	D17h	—	D97h	—	E17h	—	E97h	—	F17h	—	F97h	
C18h	—	C98h	—	D18h	—	D98h	—	E18h	—	E98h	—	F18h	—	F98h	
C19h	—	C99h	—	D19h	—	D99h	—	E19h	—	E99h	—	F19h	—	F99h	
C1Ah	—	C9Ah	—	D1Ah	—	D9Ah	—	E1Ah	—	E9Ah	—	F1Ah	—	F9Ah	
C1Bh	—	C9Bh	—	D1Bh	—	D9Bh	—	E1Bh	—	E9Bh	—	F1Bh	—	F9Bh	
C1Ch	—	C9Ch	—	D1Ch	—	D9Ch	—	E1Ch	—	E9Ch	—	F1Ch	—	F9Ch	
C1Dh	—	C9Dh	—	D1Dh	—	D9Dh	—	E1Dh	—	E9Dh	—	F1Dh	—	F9Dh	
C1Eh	—	C9Eh	—	D1Eh	—	D9Eh	—	E1Eh	—	E9Eh	—	F1Eh	—	F9Eh	
C1Fh	—	C9Fh	—	D1Fh	—	D9Fh	—	E1Fh	—	E9Fh	—	F1Fh	—	F9Fh	
C20h C6Fh	Unimplemented Read as '0'	CA0h CEFh	Unimplemented Read as '0'	D20h D6Fh	Unimplemented Read as '0'	DA0h DEFh	Unimplemented Read as '0'	E20h E6Fh	Unimplemented Read as '0'	EA0h EEFh	Unimplemented Read as '0'	F20h F6Fh	Unimplemented Read as '0'	FA0h FEFh	
C70h CFFh	Accesses 70h – 7Fh	CF0h CFFh	Accesses 70h – 7Fh	D70h D7Fh	Accesses 70h – 7Fh	DF0h DFFh	Accesses 70h – 7Fh	E70h E7Fh	Accesses 70h – 7Fh	EF0h EFFh	Accesses 70h – 7Fh	F70h F7Fh	Accesses 70h – 7Fh	FF0h FFFh	Accesses 70h – 7Fh

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 4-5: PIC16F1829LIN MEMORY MAP, BANK 31

Bank 31	
F8Ch	Unimplemented Read as '0'
FE3h	
FE4h	STATUS_SHAD
FE5h	WREG_SHAD
FE6h	BSR_SHAD
FE7h	PCLATH_SHAD
FE8h	FSR0L_SHAD
FE9h	FSR0H_SHAD
FEAh	FSR1L_SHAD
FEBh	FSR1H_SHAD
FECh	—
FEDh	STKPTR
FEEh	TOSL
FEFh	TOSH

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 4-6: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 0											
000h(1)	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
001h(1)	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
002h(1)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
003h(1)	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
004h(1)	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
005h(1)	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
006h(1)	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
007h(1)	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
008h(1)	BSR	—	—	—	BSR<4:0>					---0 0000	---0 0000
009h(1)	WREG	Working Register								0000 0000	uuuu uuuu
00Ah(1)	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
00Bh(1)	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000
00Ch	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--xx xxxx
00Dh(2)	**PORTB**	**LINTX**	**LINCS**	**LINRX**	**RB4**	**—**	**—**	**—**	**—**	**xxxx ----**	**xxxx ----**
00Eh(2)	**PORTC**	**PWRGD**	**—**	**RC5**	**RC4**	**RC3**	**RC2**	**RC1**	**RC0**	**xxxx xxxx**	**xxxx xxxx**
00Fh	—	Unimplemented								—	—
010h	—	Unimplemented								—	—
011h	PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
012h	PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	—	—	CCP2IF	0000 0--0	0000 0--0
013h	PIR3	—	—	CCP4IF	CCP3IF	TMR6IF	—	TMR4IF	—	--00 0-0-	--00 0-0-
014h	PIR4	—	—	—	—	—	—	BCL2IF	SSP2IF	---- --00	---- --00
015h	TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
016h	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
017h	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
018h	T1CON	TMR1CS1	TMR1CS0	T1CKPS<1:0>		T1OSCEN	$\overline{T1SYNC}$	—	TMR1ON	0000 00-0	uuuu uu-u
019h	T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	$\overline{T1GGO}$/DONE	T1GVAL	T1GSS<1:0>		0000 0x00	uuuu uxuu
01Ah	TMR2	Timer2 Module Register								0000 0000	0000 0000
01Bh	PR2	Timer2 Period Register								1111 1111	1111 1111
01Ch	T2CON	—	T2OUTPS<3:0>				TMR2ON	T2CKPS<1:0>		-000 0000	-000 0000
01Dh	—	Unimplemented								—	—
01Eh	CPSCON0	CPSON	CPSRM	—	—	CPSRNG<1:0>		CPSOUT	T0XCS	00-- 0000	00-- 0000
01Fh	CPSCON1	—	—	—	—	CPSCH<3:0>				---- 0000	---- 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: Registers in bold have functional differences. Please refer to the appropriate chapters in the data sheet for details.

TABLE 4-6: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 1											
080h(1)	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
081h(1)	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
082h(1)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
083h(1)	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
084h(1)	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
085h(1)	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
086h(1)	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
087h(1)	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
088h(1)	BSR	—	—	—	BSR<4:0>					---0 0000	---0 0000
089h(1)	WREG	Working Register								0000 0000	uuuu uuuu
08Ah(1)	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
08Bh(1)	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000
08Ch	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
08Dh(2)	**TRISB**	**TRISB7**	**TRISB6**	**TRISB5**	**TRISB4**	**—**	**—**	**—**	**—**	**1111 ----**	**1111 ----**
08Eh(2)	**TRISC**	**TRISC7**	**TRISC6**	**TRISC5**	**TRISC4**	**TRISC3**	**TRISC2**	**TRISC1**	**TRISC0**	**1111 1111**	**1111 1111**
08Fh	—	Unimplemented								—	—
090h	—	Unimplemented								—	—
091h(2)	**PIE1**	**TMR1GIE**	**ADIE**	**RCIE**	**TXIE**	**SSP1IE**	**CCP1IE**	**TMR2IE**	**TMR1IE**	**0000 0000**	**0000 0000**
092h	PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	—	—	CCP2IE	0000 0--0	0000 0--0
093h	PIE3	—	—	CCP4IE	CCP3IE	TMR6IE	—	TMR4IE	—	--00 0-0-	--00 0-0-
094h(2)	**PIE4**	**—**	**—**	**—**	**—**	**—**	**—**	**BCL2IE**	**SSP2IE**	**---- --00**	**---- --00**
095h	OPTION_REG	$\overline{WPUEN}$	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			1111 1111	1111 1111
096h	PCON	STKOVF	STKUNF	—	—	$\overline{RMCLR}$	$\overline{RI}$	$\overline{POR}$	$\overline{BOR}$	00-- 11qq	qq-- qquu
097h	WDTCON	—	—	WDTPS<4:0>					SWDTEN	--01 0110	--01 0110
098h	OSCTUNE	—	—	TUN<5:0>						--00 0000	--00 0000
099h	OSCCON	SPLLEN	IRCF<3:0>				—	SCS<1:0>		0011 1-00	0011 1-00
09Ah	OSCSTAT	T1OSCR	PLLR	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS	10q0 0q00	qqqq qq0q
09Bh	ADRESL	A/D Result Register Low								xxxx xxxx	uuuu uuuu
09Ch	ADRESH	A/D Result Register High								xxxx xxxx	uuuu uuuu
09Dh	ADCON0	—	CHS<4:0>					GO/$\overline{DONE}$	ADON	-000 0000	-000 0000
09Eh	ADCON1	ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>		0000 -000	0000 -000
09Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: Registers in bold have functional differences. Please refer to the appropriate chapters in the data sheet for details.

TABLE 4-6: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 2											
100h(1)	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
101h(1)	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
102h(1)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
103h(1)	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
104h(1)	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
105h(1)	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
106h(1)	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
107h(1)	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
108h(1)	BSR	—	—	—	BSR<4:0>					---0 0000	---0 0000
109h(1)	WREG	Working Register								0000 0000	uuuu uuuu
10Ah(1)	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
10Bh(1)	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000
10Ch	LATA	—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0	--xx -xxx	--uu -uuu
10Dh(2)	**LATB**	**LATB7**	**LATB6**	**LATB5**	**LATB4**	**—**	**—**	**—**	**—**	**xxxx ----**	**xxxx ----**
10Eh(2)	**LATC**	**PWRGD**	**—**	**LATC5**	**LATC4**	**LATC3**	**LATC2**	**LATC1**	**LATC0**	**xxxx xxxx**	**uuuu uuuu**
10Fh	—	Unimplemented								—	—
110h	—	Unimplemented								—	—
111h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	—	C1SP	C1HYS	C1SYNC	0000 -100	0000 -100
112h	CM1CON1	C1INTP	C1INTN	C1PCH<1:0>		—	—	C1NCH1	C1NCH0	0000 ---0	0000 ---0
113h	CM2CON0	C2ON	C2OUT	C2OE	C2POL	—	C2SP	C2HYS	C2SYNC	0000 -100	0000 -100
114h	CM2CON1	C2INTP	C2INTN	C2PCH<1:0>		—	—	C2NCH<1:0>		0000 --00	0000 --00
115h	CMOUT	—	—	—	—	—	—	MC2OUT	MC1OUT	---- --00	---- --00
116h	BORCON	SBOREN	—	—	—	—	—	—	BORRDY	1--- ---q	u--- ---u
117h	FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		0q00 0000	0q00 0000
118h	DACCON0	DACEN	DACLPS	DACOE	—	DACPSS<1:0>		—	DACNSS	000- 00-0	000- 00-0
119h	DACCON1	—	—	—	DACR<4:0>					---0 0000	---0 0000
11Ah	SRCON0	SRLEN	SRCLK<2:0>			SRQEN	SRNQEN	SRPS	SRPR	0000 0000	0000 0000
11Bh	SRCON1	SRSPE	SRSCKE	SRSC2E	SRSC1E	SRRPE	SRRCKE	SRRC2E	SRRC1E	0000 0000	0000 0000
11Ch	—	Unimplemented								—	—
11Dh(2)	**APFCON0**	**RXDTSEL**	**—**	**—**	**—**	**T1GSEL**	**TXCKSEL**	**—**	**—**	**000- 0000**	**000- 0000**
11Eh(2)	**APFCON1**	**—**	**—**	**—**	**—**	**P1DSEL**	**P1CSEL**	**P2BSEL**	**CCP2SEL**	**--00 0000**	**--00 0000**
11Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: Registers in bold have functional differences. Please refer to the appropriate chapters in the data sheet for details.

TABLE 4-6: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 3											
180h(1)	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
181h(1)	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
182h(1)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
183h(1)	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
184h(1)	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
185h(1)	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
186h(1)	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
187h(1)	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
188h(1)	BSR	—	—	—	BSR<4:0>					---0 0000	---0 0000
189h(1)	WREG	Working Register								0000 0000	uuuu uuuu
18Ah(1)	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
18Bh(1)	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000
18Ch	ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	---1 -111	---1 -111
18Dh(2)	**ANSELB**	**ANSB7**	**ANSB6**	**ANSB5**	**ANSB4**	**—**	**—**	**—**	**—**	**1111 ----**	**1111 ----**
18Eh(2)	**ANSELC**	**ANSC7**	**—**	**—**	**—**	**ANSC3**	**ANSC2**	**ANSC1**	**ANSC0**	**11-- 1111**	**11-- 1111**
18Fh	—	Unimplemented								—	—
190h	—	Unimplemented								—	—
191h	EEADRL	EEPROM / Program Memory Address Register Low Byte								0000 0000	0000 0000
192h	EEADRH	—	EEPROM / Program Memory Address Register High Byte							-000 0000	-000 0000
193h	EEDATL	EEPROM / Program Memory Read Data Register Low Byte								xxxx xxxx	uuuu uuuu
194h	EEDATH	—	—	EEPROM / Program Memory Read Data Register High Byte						--xx xxxx	--uu uuuu
195h	EECON1	EEPGD	CFGS	LWLO	FREE	WRERR	WREN	WR	RD	0000 x000	0000 q000
196h	EECON2	EEPROM control register 2								0000 0000	0000 0000
197h	—	Unimplemented								—	—
198h	—	Unimplemented								—	—
199h	RCREG	EUSART Receive Data Register								0000 0000	0000 0000
19Ah	TXREG	EUSART Transmit Data Register								0000 0000	0000 0000
19Bh	SPBRGL	BRG<7:0>								0000 0000	0000 0000
19Ch	SPBRGH	BRG<15:8>								0000 0000	0000 0000
19Dh	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
19Eh	TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	0000 0010
19Fh(2)	**BAUDCON**	**ABDOVF**	**RCIDL**	**—**	**SCKP**	**BRG16**	**—**	**WUE**	**ABDEN**	**01-0 0-00**	**01-0 0-00**

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: Registers in bold have functional differences. Please refer to the appropriate chapters in the data sheet for details.

TABLE 4-6: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 4											
200h(1)	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
201h(1)	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
202h(1)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
203h(1)	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
204h(1)	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
205h(1)	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
206h(1)	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
207h(1)	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
208h(1)	BSR	—	—	—	BSR<4:0>					---0 0000	---0 0000
209h(1)	WREG	Working Register								0000 0000	uuuu uuuu
20Ah(1)	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
20Bh(1)	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000
20Ch	WPUA	—	—	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	--11 1111	--11 1111
20Dh(2)	**WPUB**	**WPUB7**	**WPUB6**	**WPUB5**	**WPUB4**	**—**	**—**	**—**	**—**	**1111 ----**	**1111 ----**
20Eh(2)	**WPUC**	**WPUC7**	**WPUC6**	**WPUC5**	**WPUC4**	**WPUC3**	**WPUC2**	**WPUC1**	**WPUC0**	**1111 1111**	**1111 1111**
20Fh	—	Unimplemented								—	—
210h	—	Unimplemented								—	—
211h(2)	**SSP1BUF**	**Don't care**								**xxxx xxxx**	**uuuu uuuu**
212h(2)	**SSP1ADD**	**Don't care**								**0000 0000**	**0000 0000**
213h(2)	**SSP1MSK**	**Don't care**								**1111 1111**	**1111 1111**
214h(2)	**SSP1STAT**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0000 0000**	**0000 0000**
215h(2)	**SSP1CON1**	**0**	**0**	**0**	**0**	**0000**				**0000 0000**	**0000 0000**
216h(2)	**SSP1CON2**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0000 0000**	**0000 0000**
217h(2)	**SSP1CON3**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0000 0000**	**0000 0000**
218h	—	Unimplemented								—	—
219h(2)	**SSP2BUF**	**Don't care**								**xxxx xxxx**	**uuuu uuuu**
21Ah(2)	**SSP2ADD**	**Don't care**								**0000 0000**	**0000 0000**
21Bh(2)	**SSP2MSK**	**Don't care**								**1111 1111**	**1111 1111**
21Ch(2)	**SSP2STAT**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0000 0000**	**0000 0000**
21Dh(2)	**SSP2CON1**	**0**	**0**	**0**	**0**	**0000**				**0000 0000**	**0000 0000**
21Eh(2)	**SSP2CON2**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0000 0000**	**0000 0000**
21Fh(2)	**SSP2CON3**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0000 0000**	**0000 0000**

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: Registers in bold have functional differences. Please refer to the appropriate chapters in the data sheet for details.

TABLE 4-6: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 5											
280h(1)	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
281h(1)	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
282h(1)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
283h(1)	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
284h(1)	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
285h(1)	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
286h(1)	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
287h(1)	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
288h(1)	BSR	—	—	—	BSR<4:0>					---0 0000	---0 0000
289h(1)	WREG	Working Register								0000 0000	uuuu uuuu
28Ah(1)	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
28Bh(1)	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000
28Ch	—	Unimplemented								—	—
28Dh	—	Unimplemented								—	—
28Eh	—	Unimplemented								—	—
28Fh	—	Unimplemented								—	—
290h	—	Unimplemented								—	—
291h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx	uuuu uuuu
292h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx	uuuu uuuu
293h	CCP1CON	P1M<1:0>		DC1B<1:0>		CCP1M<3:0>				0000 0000	0000 0000
294h	PWM1CON	P1RSEN	P1DC<6:0>							0000 0000	0000 0000
295h	CCP1AS	CCP1ASE	CCP1AS<2:0>			PSS1AC<1:0>		PSS1BD<1:0>		0000 0000	0000 0000
296h	PSTR1CON	—	—	—	STR1SYNC	STR1D	STR1C	STR1B	STR1A	---0 0001	---0 0001
297h	—	Unimplemented								—	—
298h	CCPR2L	Capture/Compare/PWM Register 2 (LSB)								xxxx xxxx	uuuu uuuu
299h	CCPR2H	Capture/Compare/PWM Register 2 (MSB)								xxxx xxxx	uuuu uuuu
29Ah	CCP2CON	P2M1	P2M0	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	0000 0000	0000 0000
29Bh	PWM2CON	P2RSEN	P2DC6	P2DC5	P2DC4	P2DC3	P2DC2	P2DC1	P2DC0	0000 0000	0000 0000
29Ch	CCP2AS	CCP2ASE	CCP2AS2	CCP2AS1	CCP2AS0	PSS2AC1	PSS2AC0	PSS2BD1	PSS2BD0	0000 0000	0000 0000
29Dh	PSTR2CON	—	—	—	STR2SYNC	STR2D	STR2C	STR2B	STR2A	---0 0001	---0 0001
29Eh(2)	**CCPTMRS**	**0**	**C4TSEL0**	**C3TSEL1**	**C3TSEL0**	**C2TSEL1**	**C2TSEL0**	**C1TSEL1**	**C1TSEL0**	**0000 0000**	**0000 0000**
29Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: Registers in bold have functional differences. Please refer to the appropriate chapters in the data sheet for details.

TABLE 4-6: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 6											
300h(1)	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
301h(1)	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
302h(1)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
303h(1)	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
304h(1)	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
305h(1)	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
306h(1)	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
307h(1)	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
308h(1)	BSR	—	—	—	BSR<4:0>					---0 0000	---0 0000
309h(1)	WREG	Working Register								0000 0000	uuuu uuuu
30Ah(1)	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
30Bh(1)	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000
30Ch	—	Unimplemented								—	—
30Dh	—	Unimplemented								—	—
30Eh	—	Unimplemented								—	—
30Fh	—	Unimplemented								—	—
310h	—	Unimplemented								—	—
311h	CCPR3L	Capture/Compare/PWM Register 3 (LSB)								xxxx xxxx	uuuu uuuu
312h	CCPR3H	Capture/Compare/PWM Register 3 (MSB)								xxxx xxxx	uuuu uuuu
313h	CCP3CON	—	—	DC3B1	DC3B0	CCP3M3	CCP3M2	CCP3M1	CCP3M0	--00 0000	--00 0000
314h	—	Unimplemented								—	—
315h	—	Unimplemented								—	—
316h	—	Unimplemented								—	—
317h	—	Unimplemented								—	—
318h	CCPR4L	Capture/Compare/PWM Register 4 (LSB)								xxxx xxxx	uuuu uuuu
319h	CCPR4H	Capture/Compare/PWM Register 4 (MSB)								xxxx xxxx	uuuu uuuu
31Ah	CCP4CON	P4M1	P4M0	DC4B1	DC4B0	CCP4M3	CCP4M2	CCP4M1	CCP4M0	--00 0000	--00 0000
31Bh	—	Unimplemented								—	—
31Ch	—	Unimplemented								—	—
31Dh	—	Unimplemented								—	—
31Eh	—	Unimplemented								—	—
31Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: Registers in bold have functional differences. Please refer to the appropriate chapters in the data sheet for details.

TABLE 4-6: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 7											
380h(1)	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
381h(1)	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
382h(1)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
383h(1)	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
384h(1)	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
385h(1)	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
386h(1)	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
387h(1)	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
388h(1)	BSR	—	—	—	BSR<4:0>					---0 0000	---0 0000
389h(1)	WREG	Working Register								0000 0000	uuuu uuuu
38Ah(1)	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
38Bh(1)	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000
38Ch	INLVLA	—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	--00 0100	--00 0100
38Dh	INLVLB	INLVLB7	INLVLB6	INLVLB5	INLVLB4	—	—	—	—	0000 ----	0000 ----
38Eh	INLVLC	INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	11xx xxxx	11xx xxxx
38Fh	—	Unimplemented								—	—
390h	—	Unimplemented								—	—
391h	IOCAP	—	—	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	--00 0000	--00 0000
392h	IOCAN	—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	--00 0000	--00 0000
393h	IOCAF	—	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	--00 0000	--00 0000
394h	IOCBP	IOCBP7	IOCBP6	IOCBP5	IOCBP4	—	—	—	—	0000 ----	0000 ----
395h	IOCBN	IOCBN7	IOCBN6	IOCBN5	IOCBN4	—	—	—	—	0000 ----	0000 ----
396h	IOCBF	IOCBF7	IOCBF6	IOCBF5	IOCBF4	—	—	—	—	0000 ----	0000 ----
397h	—	Unimplemented								—	—
398h	—	Unimplemented								—	—
399h	—	Unimplemented								—	—
39Ah	CLKRCON	CLKREN	CLKROE	CLKRSLR	CLKRDC<1:0>		CLKRDIV<2:0>			0011 0000	0011 0000
39Bh	—	Unimplemented								—	—
39Ch	MDCON	MDEN	MDOE	MDSLR	MDOPOL	MDOUT	—	—	MDBIT	0010 ---0	0010 ---0
39Dh	MDSRC	MDMSODIS	—	—	—	MDMS<3:0>				x--- xxxx	u--- uuuu
39Eh	MDCARL	MDCLODIS	MDCLPOL	MDCLSYNC	—	MDCL<3:0>				xxx- xxxx	uuu- uuuu
39Fh	MDCARH	MDCHODIS	MDCHPOL	MDCHSYNC	—	MDCH<3:0>				xxx- xxxx	uuu- uuuu

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: Registers in bold have functional differences. Please refer to the appropriate chapters in the data sheet for details.

TABLE 4-6: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 8											
400h(1)	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
401h(1)	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
402h(1)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
403h(1)	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
404h(1)	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
405h(1)	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
406h(1)	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
407h(1)	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
408h(1)	BSR	—	—	—	BSR<4:0>					---0 0000	---0 0000
409h(1)	WREG	Working Register								0000 0000	uuuu uuuu
40Ah(1)	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
40Bh(1)	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000
40Ch	—	Unimplemented								—	—
40Dh	—	Unimplemented								—	—
40Eh	—	Unimplemented								—	—
40Fh	—	Unimplemented								—	—
410h	—	Unimplemented								—	—
411h	—	Unimplemented								—	—
412h	—	Unimplemented								—	—
413h	—	Unimplemented								—	—
414h	—	Unimplemented								—	—
415h	TMR4	Timer4 Module Register								0000 0000	0000 0000
416h	PR4	Timer4 Period Register								1111 1111	1111 1111
417h	T4CON	—	T4OUTPS<3:0>				TMR4ON	T4CKPS<1:0>		-000 0000	-000 0000
418h	—	Unimplemented								—	—
419h	—	Unimplemented								—	—
41Ah	—	Unimplemented								—	—
41Bh	—	Unimplemented								—	—
41Ch	TMR6	Timer6 Module Register								0000 0000	0000 0000
41Dh	PR6	Timer6 Period Register								1111 1111	1111 1111
41Eh	T6CON	—	T6OUTPS<3:0>				TMR6ON	T6CKPS<1:0>		-000 0000	-000 0000
41Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: Registers in bold have functional differences. Please refer to the appropriate chapters in the data sheet for details.

TABLE 4-6: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Banks 9-30											
x00h/ x80h(1)	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
x00h/ x81h(1)	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
x02h/ x82h(1)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
x03h/ x83h(1)	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
x04h/ x84h(1)	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
x05h/ x85h(1)	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
x06h/ x86h(1)	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
x07h/ x87h(1)	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
x08h/ x88h(1)	BSR	—	—	—	BSR<4:0>					---0 0000	---0 0000
x09h/ x89h(1)	WREG	Working Register								0000 0000	uuuu uuuu
x0Ah/ x8Ah(1)	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
x0Bh/ x8Bh(1)	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000
x0Ch/ x8Ch — x1Fh/ x9Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: Registers in bold have functional differences. Please refer to the appropriate chapters in the data sheet for details.

TABLE 4-6: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 31											
F80h(1)	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
F81h(1)	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
F82h(1)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
F83h(1)	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
F84h(1)	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
F85h(1)	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
F86h(1)	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
F87h(1)	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
F88h(1)	BSR	—	—	—	BSR<4:0>					---0 0000	---0 0000
F89h(1)	WREG	Working Register								0000 0000	uuuu uuuu
F8Ah(1)	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
F8Bh(1)	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000
F8Ch — FE3h	—	Unimplemented								—	—
FE4h	STATUS_ SHAD	—	—	—	—	—	Z_SHAD	DC_SHAD	C_SHAD	---- -xxx	---- -uuu
FE5h	WREG_ SHAD	Working Register Shadow								0000 0000	uuuu uuuu
FE6h	BSR_ SHAD	—	—	—	Bank Select Register Shadow					---x xxxx	---u uuuu
FE7h	PCLATH_ SHAD	—	Program Counter Latch High Register Shadow							-xxx xxxx	uuuu uuuu
FE8h	FSR0L_ SHAD	Indirect Data Memory Address 0 Low Pointer Shadow								xxxx xxxx	uuuu uuuu
FE9h	FSR0H_ SHAD	Indirect Data Memory Address 0 High Pointer Shadow								xxxx xxxx	uuuu uuuu
FEAh	FSR1L_ SHAD	Indirect Data Memory Address 1 Low Pointer Shadow								xxxx xxxx	uuuu uuuu
FEBh	FSR1H_ SHAD	Indirect Data Memory Address 1 High Pointer Shadow								xxxx xxxx	uuuu uuuu
FECh	—	Unimplemented								—	—
FEDh	STKPTR	—	—	—	Current Stack pointer					---1 1111	---1 1111
FEEh	TOSL	Top-of-Stack Low byte								xxxx xxxx	uuuu uuuu
FEFh	TOSH	—	Top-of-Stack High byte							-xxx xxxx	-uuu uuuu

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: Registers in bold have functional differences. Please refer to the appropriate chapters in the data sheet for details.

5.0 I/O PORTS

5.1 Alternate Pin Function

The Alternate Pin Function Control 0 (APFCON0) and Alternate Pin Function Control 1 (APFCON1) registers are used to steer specific peripheral input and output functions between different pins. It functions the same as described in the *"PIC16(L)F1825/1829 Data Sheet"* (DS41440) with the differences described below.

The APFCON0 and APFCON1 registers are shown in Register 5-1 and Register 5-2. For this device family, the following functions can be moved between different pins.

- RX/DT/TX/CK
- T1G
- P1B/P1C/P1D/P2B
- CCP1/P1A/CCP2

These bits have no effect on the values of any TRIS register. PORT and TRIS overrides will be routed to the correct pin. The unselected pin will be unaffected.

Register Definitions: Alternate Pin Function Control

REGISTER 5-1: APFCON0: ALTERNATE PIN FUNCTION CONTROL REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	U-0	U-0
RXDTSEL	—	—	—	T1GSEL	TXCKSEL	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **RXDTSEL:** Pin Selection bit
0 = RX/DT function is on RB5
1 = Do not use

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **T1GSEL:** Pin Selection bit
0 = T1G function is on RA4
1 = T1G function is on RA3

bit 2 **TXCKSEL:** Pin Selection bit
0 = TX/CK function is on RB7
1 = TX/CK function is on RC4

bit 1-0 **Unimplemented:** Read as '0'

REGISTER 5-2: APFCON1: ALTERNATE PIN FUNCTION CONTROL REGISTER 1

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	P1DSEL	P1CSEL	P2BSEL	CCP2SEL
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **P1DSEL:** Pin Selection bit
- 0 = P1D function is on RC2
- 1 = P1D function is on RC0

bit 2 **P1CSEL:** Pin Selection bit
- 0 = P1C function is on RC3
- 1 = P1C function is on RC1

bit 1 **P2BSEL:** Pin Selection bit
- 0 = P2B function is on RC2
- 1 = P2B function is on RA4

bit 0 **CCP2SEL:** Pin Selection bit
- 0 = CCP2 function is on RC3
- 1 = CCP2 function is on RA5

5.2 PORTB Registers

PORTB is a 4-bit wide, bidirectional port. It functions the same as described in the *"PIC16(L)F1825/1829 Data Sheet"* (DS41440) with the following differences:

- Three bits are dedicated to the LIN transceiver. No pins are associated with this function. Only RB4 is available on a pin. The corresponding data direction register is TRISB. The TRISB bits must be set as '001x 0000'.
- The PORTB Data Latch register (LATB) is also memory-mapped. Read-modify-write operations on the LATB register read and write the latched output value for PORTB.

EXAMPLE 5-1: INITIALIZING PORTB

```
banksel PORTB
MOVLW   0C0h    ; set LINCS and LINTX
                ; high
MOVWF   PORTB   ; Initialize PORTB by
                ; clearing output
                ; data latches
banksel LATB
CLRF    LATB    ; Alternate method
                ; to clear output
                ; data latches
banksel TRISB
MOVLW   030h    ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISB   ; Set RB<7:6> as outputs
                ; and RB<5:4> as inputs
```

Note: On a Power-on Reset, RB<5:4> are configured as analog inputs by default and read as '0'.

5.2.1 ANSELB REGISTER

The ANSELB register (Register 5-6) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELB bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELB bits has no effect on digital output functions. A pin with TRIS clear and ANSELB set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing READ-MODIFY-WRITE instructions on the affected port.

Note: The ANSELB bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

REGISTER 5-3: PORTB: PORTB REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	U-0	U-0	U-0	U-0
LINTX	LINCS	LINRX	RB4	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **LINTX**: Dedicated the LIN Transceiver Transmit Function
bit 6 **LINCS**: Dedicated the LIN Transceiver Chip Select Function
bit 5 **LINRX**: Dedicated the LIN Transceiver Receive Function
bit 4 **RB4**: Port I/O pin bit
bit 3-0 **Unimplemented:** Read as '0'

REGISTER 5-4: TRISB: PORTB TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	U-0	U-0	U-0	U-0
TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **TRISB7**: Must be set to '0', Dedicated the LIN Transceiver Transmit Function
bit 6 **TRISB6**: Must be set to '0', Dedicated the LIN Transceiver Chip Select Function
bit 5 **TRISB5**: Must be set to '1', Dedicated the LIN Transceiver Receive Function
bit 4 **TRISB4:** PORTB4 Tri-State Control bits
1 = PORTB pin configured as an input (tri-stated)
0 = PORTB pin configured as an output
bit 3-0 **Unimplemented:** Read as '0'

REGISTER 5-5: LATB: PORTB DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	U-0	U-0	U-0	U-0
LATB7	LATB6	LATB5	LATB4	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5 **LATB<7:5>**: Dedicated the LIN Transceiver Transmit Function(1)

bit 4 **LATB4**: RB4 Port I/O Output Latch Register bit(1)

bit 3-0 **Unimplemented:** Read as '0'

Note 1: Writes to PORTB are actually written to the corresponding LATB register. Reads from the PORTB register actually return the I/O pin values.

REGISTER 5-6: ANSELB: PORTB ANALOG SELECT REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	U-0	U-0	U-0	U-0
ANSB7	ANSB6	ANSB5	ANSB4	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5 **ANSB<7:5>**: Analog Select between Analog or Digital Function on Pins RB<7:5>
0 = Must be set to '0'. Digital I/O. Pin is assigned to port or digital special function.
1 = Not used

bit 4 **ANSB4**: Analog Select between Analog or Digital Function on Pin RB4
0 = Digital I/O. Pin is assigned to port or digital special function.
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer is disabled.

bit 3-0 **Unimplemented:** Read as '0'

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 5-7: WPUB: WEAK PULL-UP PORTB REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	U-0	U-0	U-0	U-0
WPUB7	WPUB6	WPUB5	WPUB4	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **WPUB<7:4>**: Weak Pull-up Register bits
1 = Pull-up enabled
0 = Pull-up disabled

bit 3-0 **Unimplemented:** Read as '0'

Note 1: Global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is configured as an output.

REGISTER 5-8: INLVLB: PORTB INPUT LEVEL CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0
INLVLB7	INLVLB6	INLVLB5	INLVLB4	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **INLVLB<7:4>:** PORTB Input Level Select bits
For RB<7:4> pins, respectively
1 = ST input used for PORT reads and Interrupt-on-Change
0 = TTL input used for PORT reads and Interrupt-on-Change

bit 3-0 **Unimplemented:** Read as '0'

TABLE 5-1: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELB	ANSB74	ANSB6	ANSB5	ANSB4	—	—	—	—	42
INLVLB	INLVLB7	INLVLB6	INLVLB5	INLVLB4	—	—	—	—	43
LATB	LATB7	LATB6	LATB5	LATB4	—	—	—	—	42
PORTB	LINTX	LINCS	LINRX	RB4	—	—	—	—	41
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	41
WPUB	WPUB7	WPUB6	WPUB5	WPUB4	—	—	—	—	43

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTB.

5.3 PORTC Registers

PORTC is an 8-bit wide, bidirectional port. It functions the same as described in the *"PIC16(L)F1825/1829 Data Sheet"* (DS41440) with the following differences:

- One bit is dedicated to the LIN transceiver and one bit is not available. No pins are associated with this function. Only RC<5:0> are available on pins. The corresponding data direction register is TRISC. The TRISC bits must be set as '1xxx xxxx'.
- The PORTC Data Latch register (LATC) is also memory mapped. Read-modify-write operations on the LATC register read and write the latched output value for PORTC.

Note:	On a Power-on Reset, RC<7:6> and RC<3:0> are configured as analog inputs and read as '0'.

EXAMPLE 5-2: INITIALIZING PORTC

```
banksel PORTC
CLRF    PORTC   ; Initialize PORTC by
                ; clearing output
                ; data latches
banksel LATC
CLRF    LATC    ; Alternate method
                ; to clear output
                ; data latches
banksel TRISC
MOVLW   0FFh    ; Value used to
                ; initialize data
                ; direction
```

5.3.1 ANSELC REGISTER

The ANSELC register (Register 5-12) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELC bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELC bits has no effect on digital output functions. A pin with TRIS clear and ANSELC set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing READ-MODIFY-WRITE instructions on the affected port.

Note:	The ANSELC bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

5.3.2 PORTC FUNCTIONS AND OUTPUT PRIORITIES

Each PORTC pin is multiplexed with other functions. The pins, their combined functions and their output priorities are briefly described here. For additional information, please refer to Table 1-1 and Table 1-2.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the lowest number in the following lists.

Analog input and some digital input functions are not included in the list below (see Table 5-2). These input functions can remain active when the pin is configured as an output. Certain digital input functions override other port functions and are included in the priority list.

TABLE 5-2: PORTC OUTPUT PRIORITY

Pin Name	Function Priority(1)
RC0	P1D(2)
RC1	P1C(2)
RC2	P1D(2) P2B(2)
RC3	CCP2(2) P1C(2) P2A(2)
RC4	MDOUT SRNQ C2OUT P1B
RC5	CCP1/P1A
RC6(3)	Not available
RC7(3)	PWRGD

Note 1: Priority listed from highest to lowest.
2: Pin function is selectable via the APFCON0 or APFCON1 register.
3: RC6 is not available to a pin. RC7 is internally connected to the PWRGD signal from the LIN transceiver.

REGISTER 5-9: PORTC: PORTC REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
PWRGD	—	RC5	RC4	RC3	RC2	RC1	RC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **PWRGD**: Power Good Signal from Voltage Regulator
1 = Voltage Regulator is stable and within operating limits
0 = Voltage Regulator is not stable

bit 6 **No Function**

bit 5-0 **RC<5:0>**: PORTC General Purpose I/O Pin bits
1 = Port pin is $\geq V_{IH}$
0 = Port pin is $\leq V_{IL}$

REGISTER 5-10: TRISC: PORTC TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISC7	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **TRISC7:** PORTC Tri-State Control bit
1 = PORTC pin configured as PWRGD input (tri-stated)
0 = Do not use to avoid internal contention

bit 6 **Don't Care**

bit 5-0 **TRISC<5:0>:** PORTC Tri-State Control bits
1 = PORTC pin configured as an input (tri-stated)
0 = PORTC pin configured as an output

REGISTER 5-11: LATC: PORTC DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
PWRGD	—	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **PWRGD**: Configured as an Input Value; Don't Care

bit 6 **Don't Care**

bit 5-0 **LATC<7:0>**: PORTC Output Latch Value bits(1)

Note 1: Writes to PORTC are actually written to corresponding LATC register. Reads from PORTC register is return of actual I/O pin values.

REGISTER 5-12: ANSELC: PORTC ANALOG SELECT REGISTER

R/W-1/1	R/W-1/1	U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
ANSC7	—	—	—	ANSC3	ANSC2	ANSC1	ANSC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **ANSC7**: Analog Select between Analog or Digital Function on Pin RC7
0 = Set for PWRGD input
1 = Do not use

bit 6-4 **Unimplemented:** Read as '0'

bit 3-0 **ANSC<3:0>**: Analog Select between Analog or Digital Function on Pins RC<3:0>
0 = Digital I/O. Pin is assigned to port or digital special function.
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 5-13: WPUC: WEAK PULL-UP PORTC REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **WPUC<7:0>**: Weak Pull-up Register bits(1, 2)
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: Global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is configured as an output.

REGISTER 5-14: INLVLC: PORTC INPUT LEVEL CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-0/0
INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **INLVLC<7:0>:** PORTC Input Level Select bits
For RC<7:0> pins:
1 = ST input used for port reads and Interrupt-on-change
0 = TTL input used for port reads and Interrupt-on-change

TABLE 5-3: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

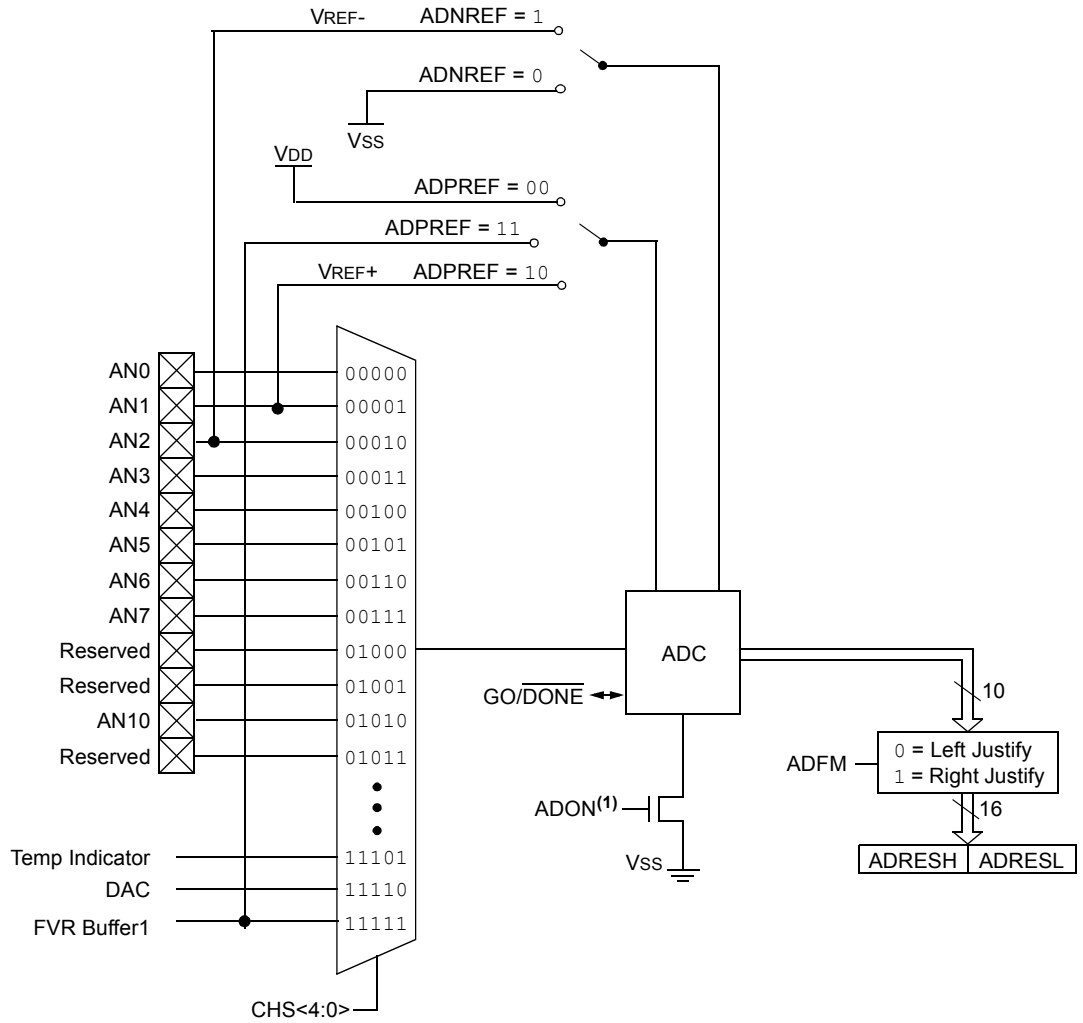
Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELC	ANSC7	—	—	—	ANSC3	ANSC2	ANSC1	ANSC0	46
INLVLC	INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	47
LATC	PWRGD	—	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	46
PORTC	PWRGD	—	RC5	RC4	RC3	RC2	RC1	RC0	45
TRISC	TRISC7	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	45
WPUC	WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	47

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTC.

6.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. It functions the same as described in the *"PIC16(L)F1825/1829 Data Sheet"* (DS41440) with the differences shown in Figure 6-1.

FIGURE 6-1: ADC BLOCK DIAGRAM



Note 1: When ADON = 0, all multiplexer inputs are disconnected.

6.1 ADC Register Definitions

The following registers are used to control the operation of the ADC.

Register Definitions: ADC Control

REGISTER 6-1: ADCON0: A/D CONTROL REGISTER 0

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	CHS<4:0>					GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '0'

bit 6-2 **CHS<4:0>:** Analog Channel Select bits

00000 = AN0
00001 = AN1
00010 = AN2
00011 = AN3
00100 = AN4
00101 = AN5
00110 = AN6
00111 = AN7
01000 = Reserved
01001 = Reserved
01010 = AN10
01011 = Reserved
01100 = Reserved. No channel connected.
•
•
•
11100 = Reserved. No channel connected.
11101 = Temperature Indicator(3)
11110 = DAC output(1)
11111 = FVR (Fixed Voltage Reference) Buffer 1 Output(2)

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
This bit is automatically cleared by hardware when the A/D conversion has completed.
0 = A/D conversion completed/not in progress

bit 0 **ADON:** ADC Enable bit

1 = ADC is enabled
0 = ADC is disabled and consumes no operating current

Note 1: See **Section 17.0 "Digital-to-Analog Converter (DAC) Module"** of the *"PIC16(L)F1825/1829 Data Sheet"* (DS41440) for more information.

2: See **Section 14.0 "Fixed Voltage Reference (FVR)"** of the *"PIC16(L)F1825/1829 Data Sheet"* (DS41440) for more information.

3: See **Section 15.0 "Temperature Indicator Module"** of the *"PIC16(L)F1825/1829 Data Sheet"* (DS41440) for more information.

TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH ADC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	—	CHS<4:0>					GO/$\overline{\text{DONE}}$	ADON	49
ADCON1	ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>		—
ADRESH	A/D Result Register High								—
ADRESL	A/D Result Register Low								—
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	—
ANSELB(1)	ANSB7	ANSB6	ANSB5	ANSB4	—	—	—	—	42
ANSELC	ANSC7	—	—	—	ANSC3	ANSC2	ANSC1	ANSC0	46
CCP4CON	P4M1	P4M0	DC4B1	DC4B0	CCP4M3	CCP4M2	CCP4M1	CCP4M0	—
INLVLA	—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	—
INLVLB(1)	INLVLB7	INLVLB6	INLVLB5	INLVLB4	—	—	—	—	43
INLVLC	INLVLC7(1)	INLVLC6(1)	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	47
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	—
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	—
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	—
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	—
TRISB(1)	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	41
TRISC	TRISC7(1)	TRISC6(1)	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	45
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		—
DACCON0	DACEN	DACLPS	DACOE	—	DACPSS<1:0>		—	DACNSS	—
DACCON1	—	—	—	DACR<4:0>					—

Legend: x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends on condition. Shaded cells are not used for ADC module.

Note 1: TRISC6 is not used as the signal does not come out to a pin. TRISC7 must be set to '1'. TRISB bits should be set as described in Register 5-4.

7.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP1 AND MSSP2) MODULE

7.1 Master SSPx (MSSPx) Module Overview

The Master Synchronous Serial Port (MSSPx) module is not to be used as its operation conflicts with LIN pin functions.

TABLE 7-1: SUMMARY OF REGISTERS ASSOCIATED WITH MSSP OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	—
ANSELB	ANSB7	ANSB6	ANSB5	ANSB4	—	—	—	—	42
ANSELC	ANSC7	—	—	—	ANSC3	ANSC2	ANSC1	ANSC0	46
APFCON0	RXDTSEL	—	—	—	T1GSEL	TXCKSEL	—	—	38
APFCON1	—	—	—	—	P1DSEL	P1CSEL	P2BSEL	CCP2SEL	39
INLVLA	—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	—
INLVLB	INLVLB7	INLVLB6	INLVLB5	INLVLB4	—	—	—	—	43
INLVLC	INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	47
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	—
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	—
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	—
SSP1BUF	Don’t care								—
SSP1CON1	0	0	0	0	0	0	0	0	—
SSP1CON3	0	0	0	0	0	0	0	0	—
SSP1STAT	0	0	0	0	0	0	0	0	—
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	—
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	41
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	45

Legend: — = Unimplemented location, read as ‘0’. Shaded cells are not used by the MSSP1 in SPI mode.

8.0 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is a serial I/O communications peripheral. It functions the same as described in the *"PIC16(L)F1825/1829 Data Sheet"* (DS41440) with the following differences:

- The 9-bit character length and Address detection should not be used.
- Programmable clock and data polarity should not be used.

8.1 Asynchronous Transmission Setup

1. Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see ***Section 26.3, EUSART Baud Rate Generator (BRG)*** in the *"PIC16(L)F1825/1829 Data Sheet"* (DS41440)).
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. TX9 control bit should always be '0' for LIN transmission.
4. Set the SCKP bit if inverted transmit is desired.
5. Enable the transmission by setting the TXEN control bit. This will cause the TXIF interrupt bit to be set.
6. If interrupts are desired, set the TXIE interrupt enable bit of the PIE1 register. An interrupt will occur immediately, provided that the GIE and PEIE bits of the INTCON register are also set.
7. If 9-bit transmission is selected, the ninth bit should be loaded into the TX9D data bit.
8. Load 8-bit data into the TXREG register. This will start the transmission.

TABLE 8-1: SUMMARY OF REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON0	RXDTSEL	—	—	—	T1GSEL	TXCKSEL	—	—	38
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	56
INLVLA	—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	—
INLVLB	INLVLB7	INLVLB6	INLVLB5	INLVLB4	—	—	—	—	43
INLVLC	INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	47
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	—
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	—
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	—
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	55
SPBRGL	BRG<7:0>								52*
SPBRGH	BRG<15:8>								52*
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	—
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	41
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	45
TXREG	EUSART Transmit Data Register								52*
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	54

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Asynchronous Transmission.
* Page provides register information.

8.2 Asynchronous Reception Setup

1. Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 26.3, EUSART Baud Rate Generator (BRG)** in the *"PIC16(L)F1825/1829 Data Sheet"* (DS41440)).
2. Clear the ANSEL bit for the RX pin (if applicable).
3. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
4. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
5. If 9-bit reception is desired, set the RX9 bit.
6. Enable reception by setting the CREN bit.
7. The RCIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
8. Read the RCSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
9. Get the received eight Least Significant data bits from the receive buffer by reading the RCREG register.
10. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

TABLE 8-2: SUMMARY OF REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON0	RXDTSEL	—	—	—	T1GSEL	TXCKSEL	—	—	38
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	56
INLVLA	—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	—
INLVLB	INLVLB7	INLVLB6	INLVLB5	INLVLB4	—	—	—	—	43
INLVLC	INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	47
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	—
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	—
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	—
RCREG	EUSART Receive Data Register								53*
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	55
SPBRGL	BRG<7:0>								52, 53*
SPBRGH	BRG<15:8>								52, 53*
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	—
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	41
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	45
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	54

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Asynchronous Reception.
* Page provides register information.

REGISTER 8-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-1/1	R/W-0/0
CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **CSRC:** Must be '0'

bit 6 **TX9:** Must be '0'

bit 5 **TXEN:** Transmit Enable bit
1 = Transmit enabled
0 = Transmit disabled

bit 4 **SYNC:** Must be '0'

bit 3 **SENDB:** Send BREAK Character bit
1 = Send Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission completed

bit 2 **BRGH:** High Baud Rate Select bit
1 = High speed
0 = Low speed

bit 1 **TRMT:** Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

bit 0 **TX9D:** Must be '0'

REGISTER 8-2: RCSTA: RECEIVE STATUS AND CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-0/0	R-0/0	R-x/x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **SPEN:** Serial Port Enable bit
1 = Serial port enabled (configures RX/DT and TX/CK pins as serial port pins)
0 = Serial port disabled (held in Reset)

bit 6 **RX9:** Must be '0'

bit 5 **SREN:** Don't Care

bit 4 **CREN:** Continuous Receive Enable bit
1 = Enables receiver
0 = Disables receiver

bit 3 **ADDEN:** Must be '0'

bit 2 **FERR:** Framing Error bit
1 = Framing error (can be updated by reading RCREG register and receive next valid byte)
0 = No framing error

bit 1 **OERR:** Overrun Error bit
1 = Overrun error (can be cleared by clearing bit CREN)
0 = No overrun error

bit 0 **RX9D:** Must be '0'

REGISTER 8-3: BAUDCON: BAUD RATE CONTROL REGISTER

R-0/0	R-1/1	U-0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0
ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **ABDOVF:** Auto-Baud Detect Overflow bit
Asynchronous mode:
1 = Auto-baud timer overflowed
0 = Auto-baud timer did not overflow
Synchronous mode:
Don't care

bit 6 **RCIDL**: Receive Idle Flag bit
Asynchronous mode:
1 = Receiver is Idle
0 = Start bit has been received and the receiver is receiving
Synchronous mode:
Don't care

bit 5 **Unimplemented:** Read as '0'

bit 4 **SCKP:** Must be '0'

bit 3 **BRG16:** 16-bit Baud Rate Generator bit
1 = 16-bit Baud Rate Generator is used
0 = 8-bit Baud Rate Generator is used

bit 2 **Unimplemented:** Read as '0'

bit 1 **WUE:** Wake-up Enable bit
1 = Receiver is waiting for a falling edge. No character will be received, byte RCIF will be set. WUE will automatically clear after RCIF is set.
0 = Receiver is operating normally

bit 0 **ABDEN**: Auto-Baud Detect Enable bit
1 = Auto-Baud Detect mode is enabled (clears when auto-baud is complete)
0 = Auto-Baud Detect mode is disabled

9.0 CONSIDERATION OF SPLIT POWER SUPPLIES AND DURING DEBUG

When the microcontroller is powered by a source other than the LIN Voltage Regulator, the following should be observed. This also applies when debugging and power the microcontroller from the emulator.

Leaving RB7/TX or RB6/LINCS outputs in a high state ('1') will source current into the internal voltage regulator and prevent the RESET circuit from detecting a Power-on-event. Always drive RB7/TX low when putting the transceiver into Power-Down mode by controlling RB6/CS = 0.

If the microcontroller is supplied by the debugging tool, be aware that the VBAT must be applied to the VBAT pin for the transceiver to operate.

10.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings(†)

Ambient temperature under bias.....-40°C to +125°C
Storage temperature.....-65°C to +150°C
Voltage on V_{DD} with respect to V_{SS}.....-0.3V to +6.5V
Voltage on $\overline{MCLR}$ with respect to Vss.....-0.3V to +9.0V
Voltage on all other logic level pins with respect to V_{SS}.....-0.3V to (V_{DD} + 0.3V)
Total power dissipation (**Note 5**).....800 mW
Maximum current out of V_{SS} pin, -40°C ≤ T_A ≤ +125°C for extended..... 35 mA
Maximum current into V_{DD} pin, -40°C ≤ T_A ≤ +125°C for extended..... 30 mA
Clamp current, I_K (V_{PIN} < 0 or V_{PIN} > V_{DD}).....± 20 mA
Maximum output current sunk by any I/O pin.....25 mA
Maximum output current sourced by any I/O pin.....25 mA
V_{BB} Battery Voltage, non-operating (LIN bus recessive, no regulator load, t < 60s)..... -0.3 to +43V
V_{BB} Battery Voltage, transient ISO 7637 Test 1 ..... -200V
V_{BB} Battery Voltage, transient ISO 7637 Test 2a .....+150V
V_{BB} Battery Voltage, transient ISO 7637 Test 3a ..... -300V
V_{BB} Battery Voltage, transient ISO 7637 Test 3b .....+200V
V_{BB} Battery Voltage, continuous ..... -0.3 to +30V
V_{LBUS} Bus Voltage, continuous..... -18 to +30V
V_{LBUS} Bus Voltage, transient (**Note 1**) ..... -27 to +43V
I_{LBUS} Bus Short Circuit Current Limit .....200 mA
ESD protection on LIN, V_{BB} (IEC 61000-4-2, 330 Ohm, 150 pF) (**Note 3**)..... Minimum ±9 kV
ESD protection on LIN, V_{BB} (Charge Device Model) (**Note 2**).....±1500V
ESD protection on LIN, VBB (Human Body Model, 1 kOhm, 100 pF) (**Note 4**) .....±8 kV
ESD protection on LIN, V_{BB} (Machine Model) (**Note 2**).....±800V
ESD protection on all other pins (Human Body Model) (**Note 2**) .....> 4 kV
Maximum Junction Temperature.....150°C
Storage Temperature.....-55 to +150°C

Note 1: ISO 7637/1 load dump compliant (t < 500 ms).

2: According to JESD22-A114-B.

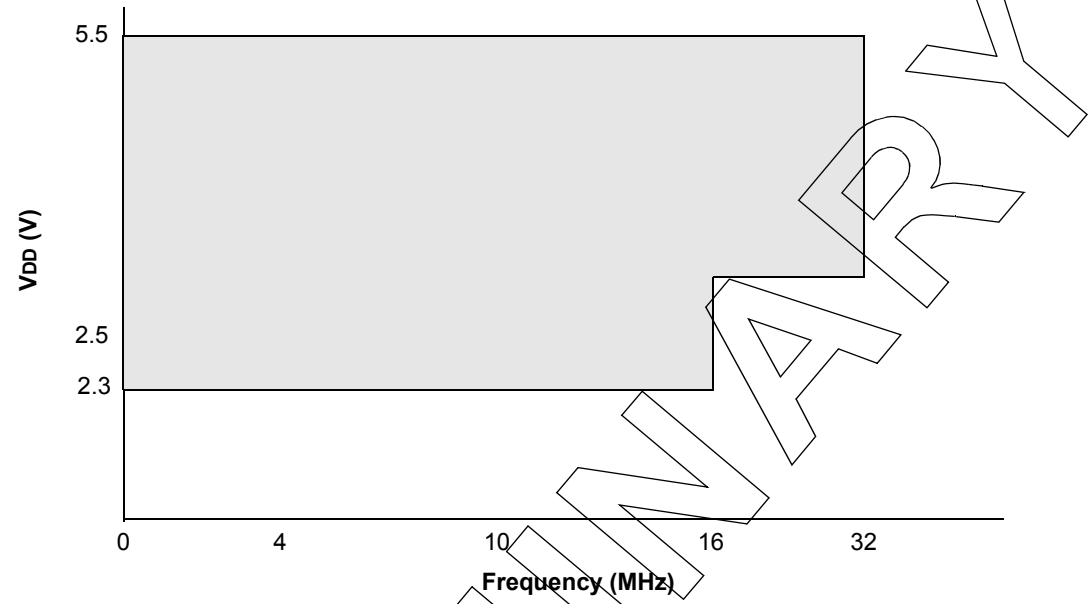
3: According to IBEE, without bus filter.

4: Limited by Test Equipment.

5: Power dissipation is calculated as follows:
$P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

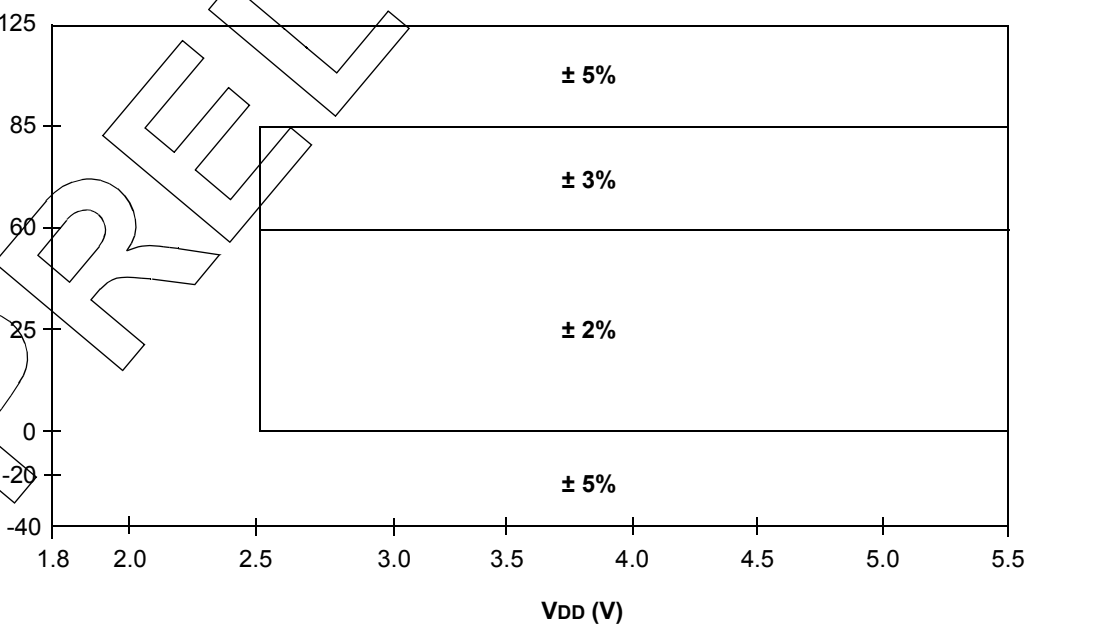
FIGURE 10-1: PIC16F1829LIN VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency of the microcontroller only. When powered by the internal voltage regulator, the microcontroller is operated only in the 4.5-5.5V range.

2: Refer to Table 30-1 in the *"PIC16(L)F1825/1829 Data Sheet"* (DS41440) for each Oscillator mode's supported frequen-

FIGURE 10-2: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE



10.1 DC Characteristics: PIC16F1829LIN-E (Extended)

PIC16F1829LIN			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended				
Param. No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
		Supply Voltage					
D001	VDD	PIC16F1829LIN	2.3	—	5.5	V	FOSC ≤ 32 MHz **(Note 1)**

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: PLL required for 32 MHz operation.

10.2 DC Characteristics: PIC16F1829LIN-E (Extended)

PIC16F1829LIN			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param. No.	Symbol	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
							VDD	Note
		Current for Transceiver and Voltage Regulator(1)						
TBD	IBBQ	VBB Quiescent Operating Current	—	115	210	µA	5.0	IOUT = 0 mA, LBUS recessive
TBD	IBBTO	VBB Transmitter-off Current	—	90	190	µA	5.0	With V_{REG} on, transmitter off, receiver on, $\overline{FAULT}$/TXE = VIL, CS = VIH
TBD	IBBPD	VBB Power-down Current	—	16	26	µA	5.0	With VREG powered-off, receiver on and transmitter off, $\overline{FAULT}$/TXE = VIH, TXD = VIH, CS = VIL)
TBD	IBBNO-GND	VBB Current with VSS Floating	-1	—	1	mA	5.0	VBB = 12V, GND to VBB, VLIN = 0-18V
		Supply Current (IDD)(2, 3)						
D010			—	5.5	15	µA	1.8	FOSC = 32 kHz LP Oscillator
			—	7.8	18	µA	3.0	
D010			—	20	55	µA	1.8	FOSC = 32 kHz LP Oscillator
			—	25	60	µA	3.0	
			—	27	65	µA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TBD = To be determined

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Maximum values should be used when calculating total current consumption.

2: The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

4: 8 MHz internal RC oscillator with 4x PLL enabled.

5: 8 MHz crystal oscillator with 4x PLL enabled.

6: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ..

10.2 DC Characteristics: PIC16F1829LIN-E (Extended) (Continued)

PIC16F1829LIN				Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended				
Param. No.	Symbol	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
							VDD	Note
		Supply Current (IDD)(2, 3)						
D011			—	83	140	µA	1.8	FOSC = 1 MHz XT Oscillator
			—	130	230	µA	3.0	
D011			—	105	160	µA	1.8	FOSC = 1 MHz XT Oscillator
			—	160	250	µA	3.0	
			—	230	320	µA	5.0	
D012			—	220	310	µA	1.8	FOSC = 4 MHz XT Oscillator
			—	378	540	µA	3.0	
D012			—	240	300	µA	1.8	FOSC = 4 MHz XT Oscillator
			—	400	500	µA	3.0	
			—	590	760	µA	5.0	
D013			—	46	160	µA	1.8	FOSC = 1 MHz EC Oscillator Medium-Power mode
			—	90	230	µA	3.0	
D013			—	70	180	µA	1.8	FOSC = 1 MHz EC Oscillator Medium-Power mode
			—	120	240	µA	3.0	
			—	190	320	µA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TBD = To be determined

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Maximum values should be used when calculating total current consumption.

2: The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

4: 8 MHz internal RC oscillator with 4x PLL enabled.

5: 8 MHz crystal oscillator with 4x PLL enabled.

6: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ..

10.2 DC Characteristics: PIC16F1829LIN-E (Extended) (Continued)

PIC16F1829LIN			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param. No.	Symbol	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
							VDD	Note
		Supply Current (IDD)(2, 3)						
D014			—	192	250	µA	1.8	FOSC = 4 MHz EC Oscillator Medium-Power mode
			—	336	430	µA	3.0	
D014			—	210	275	µA	1.8	FOSC = 4 MHz EC Oscillator Medium-Power mode
			—	356	450	µA	3.0	
			—	430	650	µA	5.0	
D015			—	6.5	18	µA	1.8	FOSC = 31 kHz LFINTOSC
			—	9.0	20	µA	3.0	
D015			—	20	60	µA	1.8	FOSC = 31 kHz LFINTOSC
			—	25	65	µA	3.0	
			—	27	70	µA	5.0	
D016			—	110	170	µA	1.8	FOSC = 500 kHz MFINTOSC
			—	130	200	µA	3.0	
D016			—	125	180	µA	1.8	FOSC = 500 kHz MFINTOSC
			—	155	250	µA	3.0	
			—	160	280	µA	5.0	
D017*			—	0.6	0.85	mA	1.8	FOSC = 8 MHz HFINTOSC
			—	0.9	1.25	mA	3.0	
D017*			—	0.6	0.85	mA	1.8	FOSC = 8 MHz HFINTOSC
			—	0.96	1.35	mA	3.0	
			—	1.03	1.55	mA	5.0	
D018			—	0.9	1.2	mA	1.8	FOSC = 16 MHz HFINTOSC
			—	1.4	1.95	mA	3.0	
D018			—	0.92	1.2	mA	1.8	FOSC = 16 MHz HFINTOSC
			—	1.49	1.9	mA	3.0	
			—	1.58	2.4	mA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TBD = To be determined

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Maximum values should be used when calculating total current consumption.

2: The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

4: 8 MHz internal RC oscillator with 4x PLL enabled.

5: 8 MHz crystal oscillator with 4x PLL enabled.

6: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ..

10.2 DC Characteristics: PIC16F1829LIN-E (Extended) (Continued)

PIC16F1829LIN				Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended				
Param. No.	Symbol	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
							VDD	Note
		Supply Current (IDD)(2, 3)						
D019			—	2.8	3.6	mA	3.0	FOSC = 32 MHz HFINTOSC **(Note 4)**
			—	3.4	3.9	mA	3.6	
D019			—	2.8	4.0	mA	3.0	FOSC = 32 MHz HFINTOSC **(Note 4)**
			—	3.0	4.5	mA	5.0	
D020			—	2.7	3.6	mA	3.0	FOSC = 32 MHz HS Oscillator **(Note 5)**
			—	3.2	4.2	mA	3.6	
D020			—	2.7	4.0	mA	3.0	FOSC = 32 MHz HS Oscillator **(Note 5)**
			—	3.2	4.3	mA	5.0	
D021			—	222	350	μA	1.8	FOSC = 4 MHz EXTRC **(Note 6)**
			—	400	690	μA	3.0	
D021			—	240	500	μA	1.8	FOSC = 4 MHz EXTRC **(Note 6)**
			—	416	800	μA	3.0	
			—	497	900	μA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TBD = To be determined

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Maximum values should be used when calculating total current consumption.

2: The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

4: 8 MHz internal RC oscillator with 4x PLL enabled.

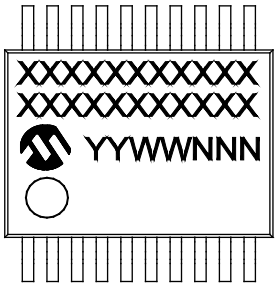
5: 8 MHz crystal oscillator with 4x PLL enabled.

6: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ..

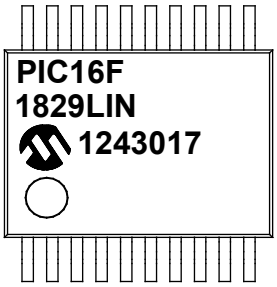
11.0 PACKAGING INFORMATION

11.1 Package Marking Information

20-Lead SSOP (5.30 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

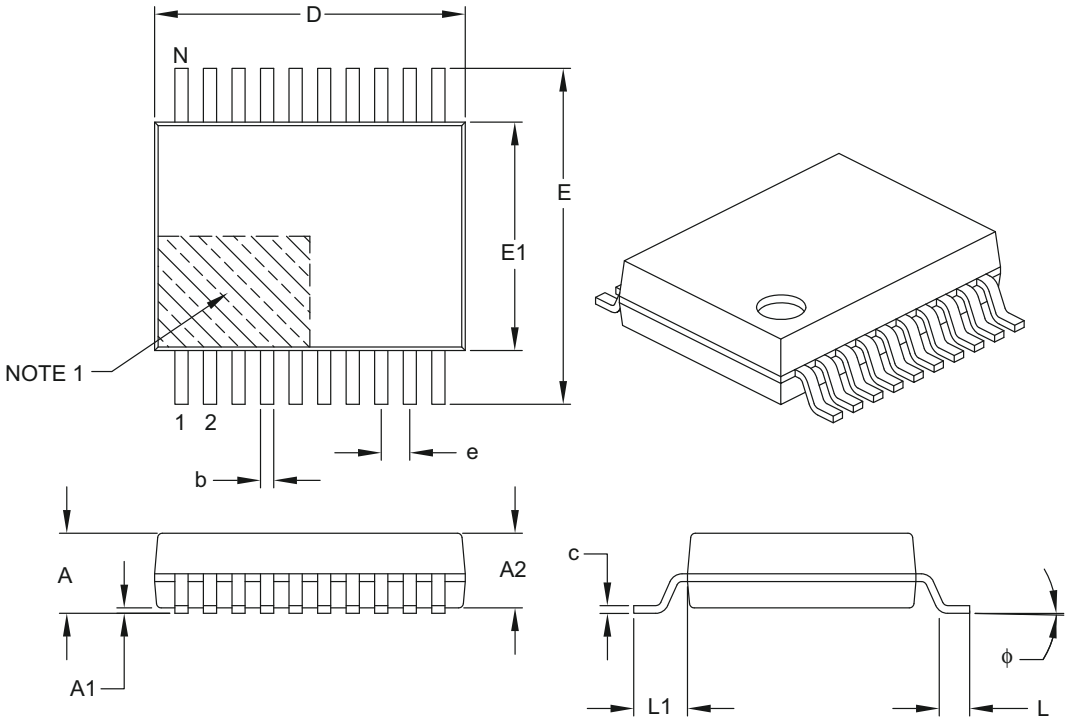
* Standard PIC® device marking consists of Microchip part number, year code, week code, and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

11.2 Package Details

The following sections give the technical details of the packages.

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

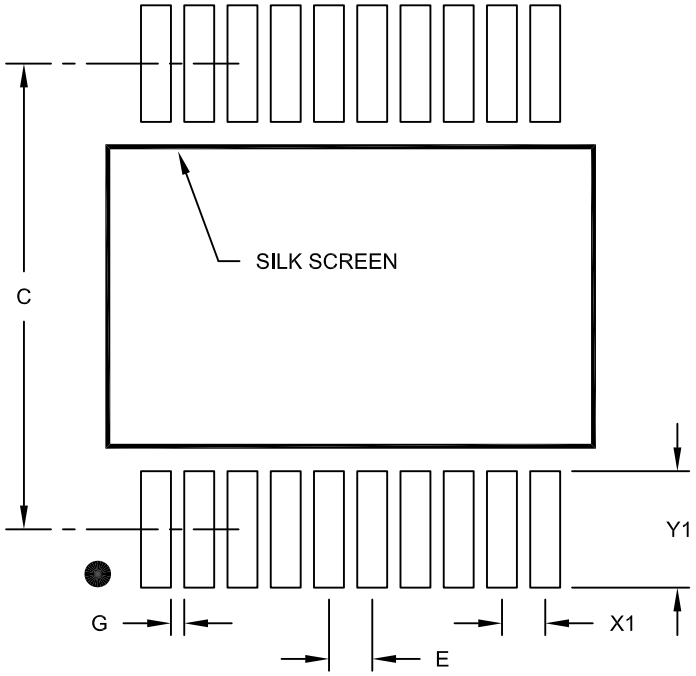
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072A

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A (12/2012)

Initial release.

INDEX

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Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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- Distributor or Representative
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- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

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It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

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Device: PIC16F1829LIN Literature Number: DS41673A

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-	X	/XX	XXX
Device	Tape and Reel Option		Temperature Range	Package	Pattern

Device:	PIC16F1829LIN	
Tape and Reel Option:	Blank T	= Standard packaging (tube or tray) = Tape and Reel(1)
Temperature Range:	E	= -40°C to +125°C (Extended)
Package:(2)	SS	= SSOP
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC16F1829LIN - E/SS
Extended temperature,
SSOP package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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ISO/TS 16949

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