

# PCS3P2537A

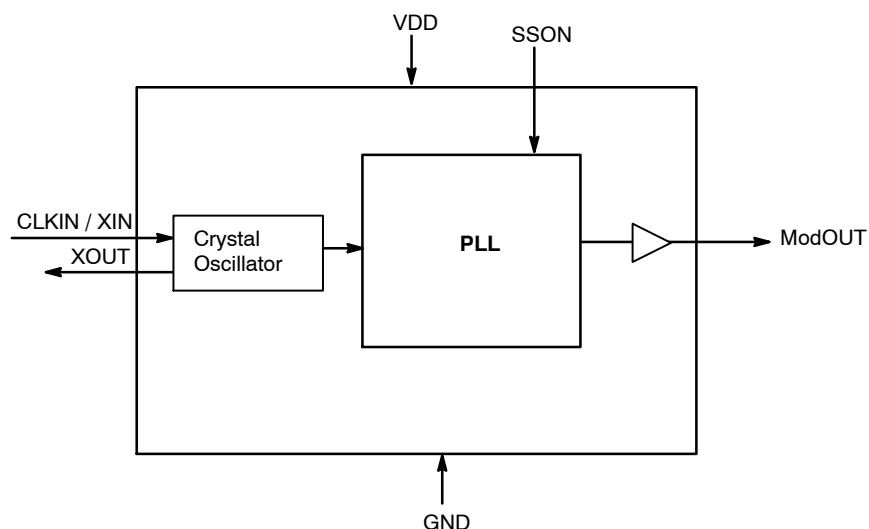


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	CLKIN / XIN	Input	External reference Clock input or Crystal connection. This pin has dual functions. It can be connected either to an external crystal or an external reference clock.
2	XOUT	Output	Crystal connection. If using an external reference, this pin must be left unconnected.
3	SSON	Input	When SSON is HIGH, the spread spectrum is enabled and when LOW, it turns off the spread spectrum.
4	NC		No Connect.
5	GND	Power	Ground Connection.
6	ModOUT	Output	Spread Spectrum Clock Output.
7	NC		No Connect.
8	VDD	Power	Power supply for the entire chip.

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD, V <sub>IN</sub>	Voltage with any pin with respect to Ground	-0.5 to +4.6	V
T <sub>STG</sub>	Storage temperature	-65 to +125	°C
T <sub>s</sub>	Max. Soldering Temperature (10 sec)	260	°C
T <sub>J</sub>	Junction Temperature	150	°C
T <sub>DV</sub>	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. OPERATING CONDITIONS

Parameter	Description	Min	Max	Unit
VDD	Supply Voltage	3.0	3.6	V
T <sub>A</sub>	Operating Temperature (Ambient Temperature)	0	70	°C
C <sub>L</sub>	Load Capacitance		15	pF
C <sub>IN</sub>	Input Capacitance		7	pF

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**Table 4. DC ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY**

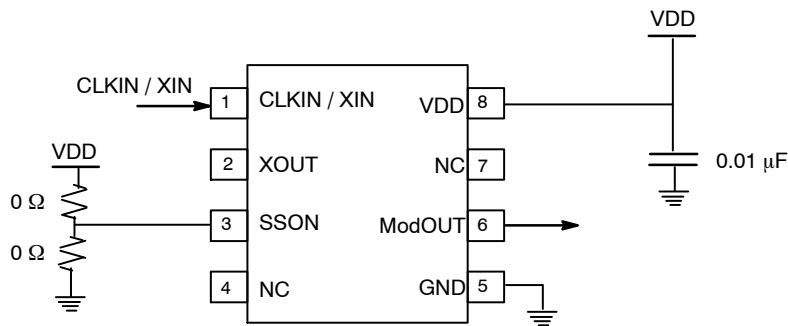
Symbol	Parameter	Min	Typ	Max	Units
V <sub>IL</sub>	Input low voltage	VSS – 0.3		0.8	V
V <sub>IH</sub>	Input high voltage	2.0		VDD + 0.3	V
I <sub>IL</sub>	Input low current			–35	μA
I <sub>IH</sub>	Input high current			35	μA
V <sub>OL</sub>	Output low voltage (VDD = 3.3 V, I <sub>OL</sub> = 8 mA)			0.4	V
V <sub>OH</sub>	Output high voltage (VDD = 3.3 V, I <sub>OH</sub> = 8 mA)	2.5			V
I <sub>DD</sub>	Static supply current (Note 1)			2.5	mA
I <sub>CC</sub>	Dynamic supply current (3.3 V, 27 MHz and no load)		5	8	mA
VDD	Operating Voltage	3	3.3	3.6	Ω
t <sub>ON</sub>	Power-up time (first locked cycle after power-up)			5	mS
Z <sub>OUT</sub>	Output impedance		36		Ω

1. CLKIN is pulled to GND.

**Table 5. AC ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY**

Symbol	Parameter	Min	Typ	Max	Units
CLKIN	Input frequency	18	27	36	MHz
ModOUT	Output frequency	18	27	36	MHz
f <sub>d</sub>	Frequency Deviation @ 27 MHz	–0.2	–0.25	–0.3	%
MR	Modulation Rate @ 27 MHz	30		33	KHz
t <sub>LH</sub> (Note 2)	Output rise time (measured from 20% to 80%)			2	nS
t <sub>HL</sub> (Note 2)	Output fall time (measured at 80% to 20%)			1.5	nS
t <sub>JC</sub>	Cycle-to-Cycle Jitter at 27 MHz		±200	±300	pS
t <sub>D</sub>	Output duty cycle	45	50	55	%

2. t<sub>LH</sub> and t<sub>HL</sub> are measured into a capacitive load of 15 pF.



Note: Refer to Pin Description table for Functionality Details.

**Figure 2. Typical Application Schematic**

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## PCB Layout Recommendation

For optimum device performance, the following guidelines are recommended.

- Dedicated VDD and GND planes.
- The device must be isolated from system power supply noise. A 0.01  $\mu\text{F}$  decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The

PCB trace to VDD pin and the ground via should be kept as short as possible. All the VDD pins should have decoupling capacitors.

- In an optimum layout all components are on the same side of the board, minimizing vias through other signal layers.

A typical layout is shown in the Figure 3.

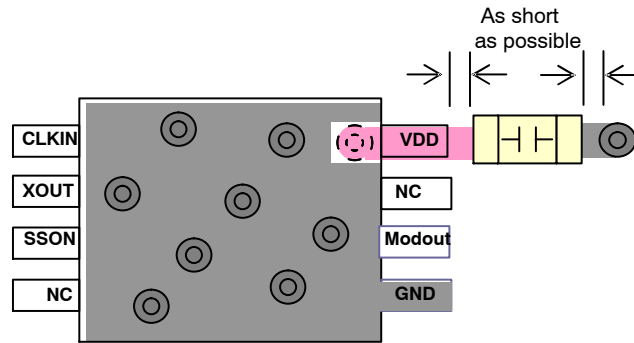
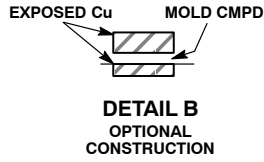
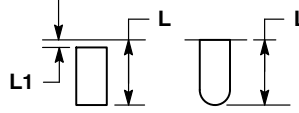
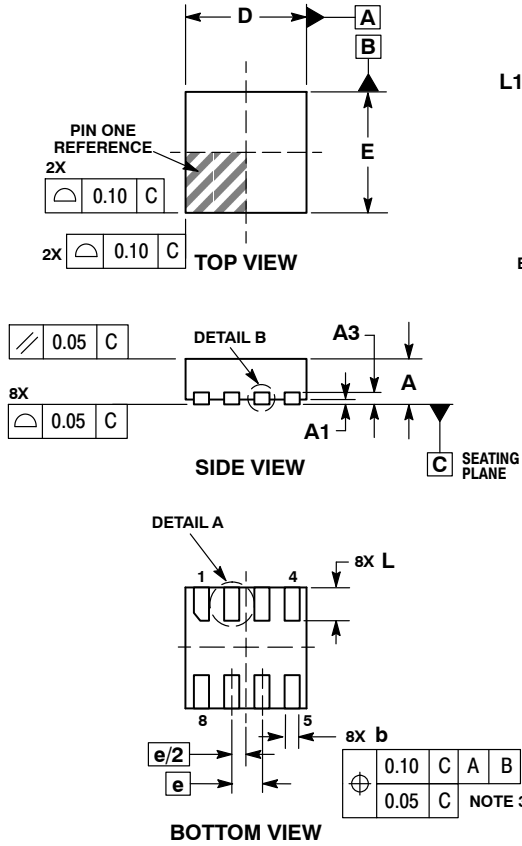


Figure 3. Typical Layout

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## PACKAGE DIMENSIONS

WDFN8 2x2, 0.5P  
CASE 511AQ  
ISSUE A

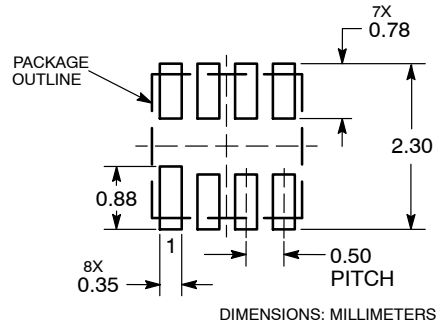


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.50	0.60
L1	---	0.15

### RECOMMENDED SOLDERING FOOTPRINT\*




\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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**Table 6. ORDERING INFORMATION**

Part Number	Top Marking	Package Type	Temperature
PCS3P2537AG-08CR	AM	8L-WDFN (8L-TDFN) – TAPE & REEL, Green	0°C to +70°C

NOTE: A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free

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