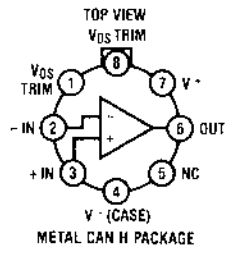
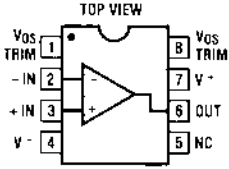


ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 22V
Internal Power Dissipation	500mW
Input Voltage	Equal to Supply Voltage
Output Short Circuit Duration	Indefinite
Differential Input Current (Note 8)	± 25mA
Lead Temperature (Soldering, 10 sec.)	300°C
Operating Temperature Range	
OP-27/OP-37 A, C	– 55°C to 125°C
OP-27/OP-37 E, G	– 25°C to 85°C
Junction Temperature Range	
OP-27/OP-37 A, C	– 55°C to 150°C
OP-27/OP-37 E, G	– 25°C to 125°C
Storage Temperature Range	
OP-27/OP-37 A, C, E, G	– 65°C to 150°C

PACKAGE/ORDER INFORMATION

TOP VIEW		ORDER PART NUMBER	
 METAL CAN H PACKAGE		OBSOLETE PACKAGE	
		OP-27AH	OP-37AH
		OP-27CH	OP-37CH
		OP-27EH	OP-37EH
		OP-27GH	OP-37GH
TOP VIEW			
 HERMETIC DIP J8 PACKAGE PLASTIC DIP N8 PACKAGE		OP-27AJ8	OP-37EJ8
		OP-27CJ8	OP-37GJ8
		OP-27EJ8	OP-27EN8
		OP-27GJ8	OP-27GN8
		OP-37AJ8	OP-37EN8
		OP-37CJ8	OP-37GN8

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-27A,E/OP-37A,E			OP-27C,G/OP-37C,G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)		10	25		30	100	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Offset Voltage Stability	(Note 2)		0.2	1.0		0.4	2.0	$\mu V/ Mo$
I_{OS}	Input Offset Current			7	35		12	75	nA
I_B	Input Bias Current			± 10	± 40		± 15	± 80	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Notes 3 and 5)		0.08	0.18		0.09	0.25	$\mu V/p$
	Input Noise Voltage Density	$f_o = 10Hz$ (Note 3)		3.5	5.5		3.8	8.0	nV/ $\sqrt{Hz}$
		$f_o = 30Hz$ (Note 3)		3.1	4.5		3.3	5.6	nV/ $\sqrt{Hz}$
		$f_o = 1000Hz$ (Note 3)		3.0	3.8		3.2	4.5	nV/ $\sqrt{Hz}$
i_n	Input Noise Current Density	$f_o = 10Hz$ (Notes 3 and 6)		1.7	4.0		1.7		pA/ $\sqrt{Hz}$
		$f_o = 30Hz$ (Notes 3 and 6)		1.0	2.3		1.0		pA/ $\sqrt{Hz}$
		$f_o = 1000Hz$ (Notes 3 and 6)		0.4	0.6		0.4	0.6	pA/ $\sqrt{Hz}$
	Input Resistance—Common Mode			3			2		GΩ
	Input Voltage Range		± 11.0	± 12.3		± 11.0	± 12.3		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11V$	114	126		100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	100	120		94	118		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	1000	1800		700	1500		V/mV
		$R_L \geq 1k\Omega$, $V_O = \pm 10V$	800	1500			1500		V/mV
		$R_L = 600\Omega$, $V_O = \pm 1V$	250	700		200	500		V/mV
		$V_S = \pm 4V$ (Note 4)							
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	± 12.0	± 13.8		± 11.5	± 13.5		V
		$R_L \geq 600\Omega$	± 10.0	± 11.5		± 10.0	± 11.5		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Note 4)	1.7	2.8		1.7	2.8		V/ μs
		$A_{VOL} \geq 5$ (Note 4)	11	17		11	17		V/ μs
GBW	Gain-Bandwidth Product	$f_o = 100kHz$ (Note 4)	5.0	8.0		5.0	8.0		MHz
		$f_o = 10kHz$ (Note 4)	45	63		45	63		MHz
		$f_o = 1MHz$ ($A_{VOL} \geq 5$)		40			40		MHz
Z_O	Open Loop Output Resistance	$V_O = 0$, $I_O = 0$		70			70		Ω
P_d	Power Dissipation			90	140		100	170	mW

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		OP-27A/OP-37A			OP-27C/OP-37C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	●		30	60		70	300	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●		0.2	0.6		0.4	1.8	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●		15	50		30	135	nA
I_B	Input Bias Current		●		± 20	± 60		± 35	± 150	nA
	Input Voltage Range		●	± 10.3	± 11.5		± 10.2	± 11.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	108	122		94	116		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	96	116		86	110		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	●	600	1200		300	800		V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 11.5	± 13.5		± 10.5	± 13.0		V

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq 85^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		OP-27E/OP-37E			OP-27G/OP-37G			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	●		20	50		55	220	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●		0.2	0.6		0.4	1.8	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●		10	50		20	135	nA
I_B	Input Bias Current		●		± 14	± 60		± 25	± 150	nA
	Input Voltage Range		●	± 10.5	± 11.8		± 10.5	± 11.8		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	110	124		96	118		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	97	118		90	114		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	●	750	1500		450	1000		V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 11.7	± 13.6		± 11.0	± 13.3		V

The ● denotes the specifications which apply over full operating temperature range.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 seconds after application of power. A and E grades are guaranteed fully warmed up.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically $2.5\mu V$ —refer to typical performance curve.

Note 3: Sample tested. Contact factory for 100% testing of 10Hz voltage noise.

Note 4: Parameter is guaranteed by design and is not tested.

Note 5: See test circuit and frequency response curve for 0.1Hz to 10Hz tester in Applications Information section.

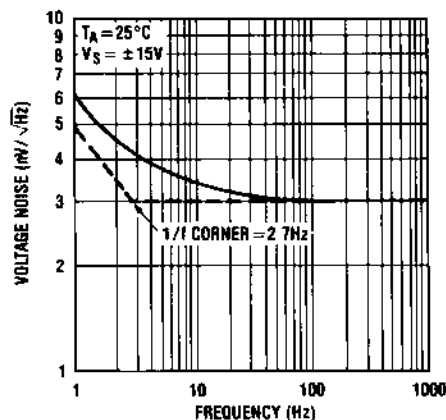
Note 6: See test circuit for current noise measurement in Applications Information section.

Note 7: The Average Input Offset Drift performance is within the specifications unnullled or when nullled with a pot having a range of $8k\Omega$ to $20k\Omega$.

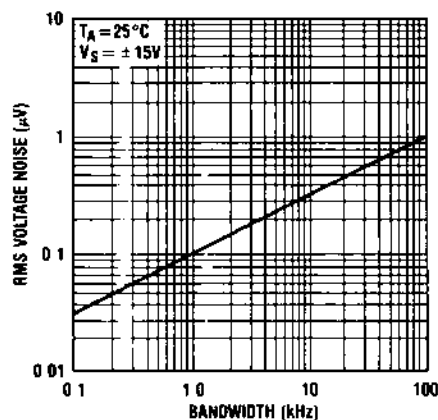
Note 8: The OP-27/37's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds $\pm 0.7V$, the input current should be limited to 25mA.

TYPICAL PERFORMANCE CHARACTERISTICS

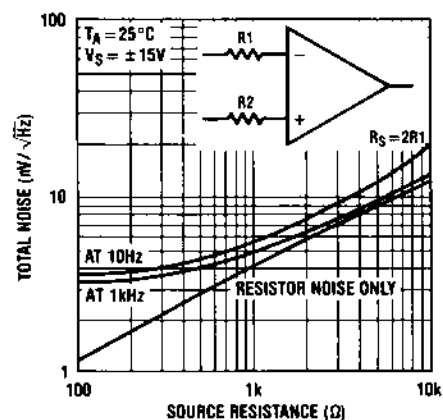
Voltage Noise vs Frequency



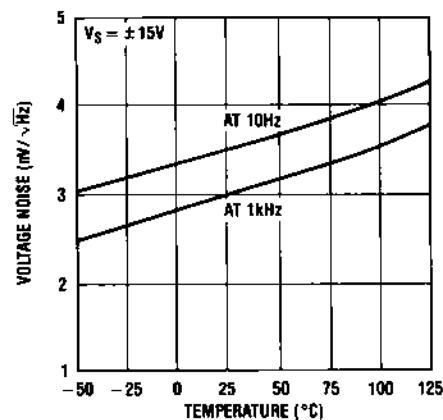
Input Wideband Voltage Noise vs Bandwidth (0.1Hz to Frequency Indicated)



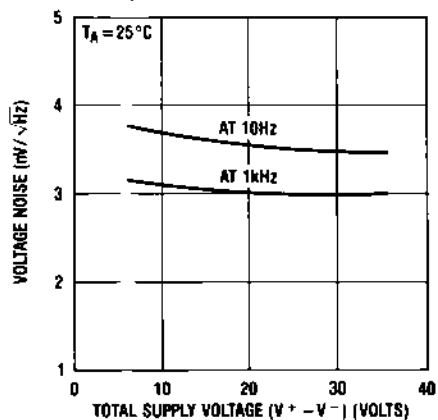
Total Noise vs Source Resistance



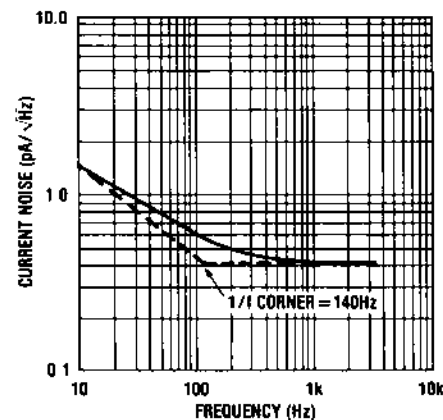
Voltage Noise vs Temperature



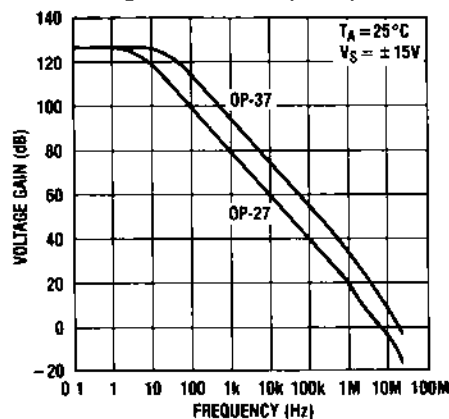
Voltage Noise vs Supply Voltage



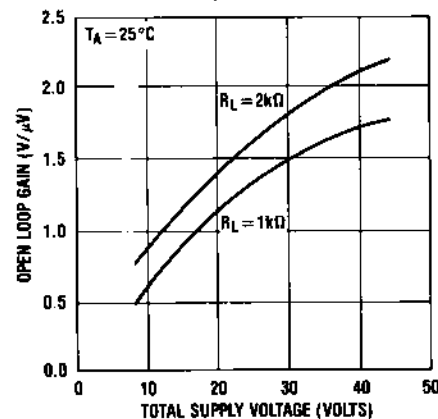
Current Noise vs Frequency



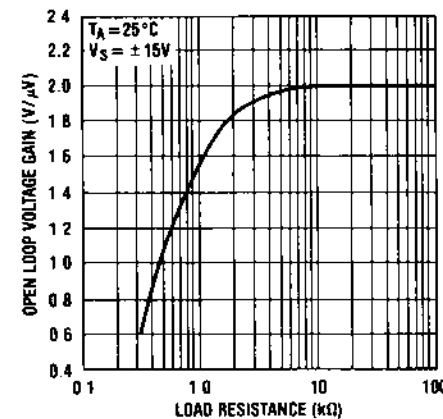
Voltage Gain vs Frequency



Open Loop Voltage Gain vs Supply Voltage

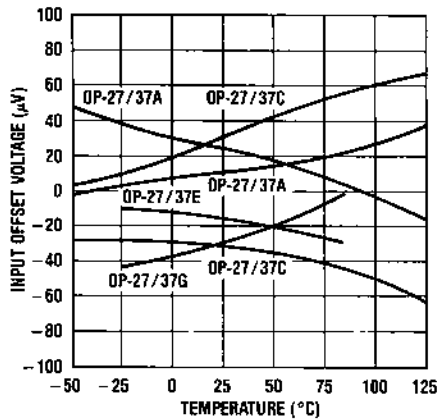


Open Loop Voltage Gain vs Load Resistance

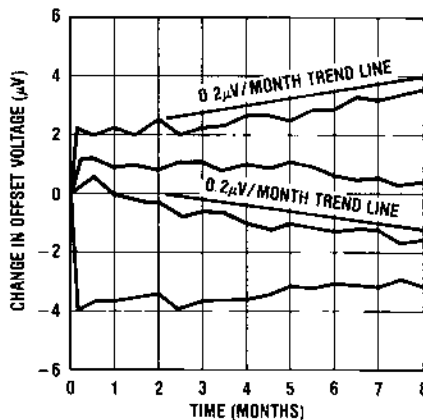


TYPICAL PERFORMANCE CHARACTERISTICS

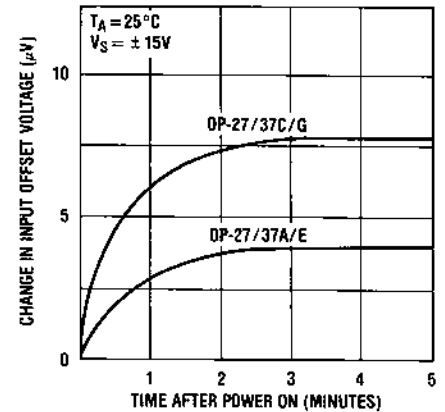
Offset Voltage Drift of Representative Units



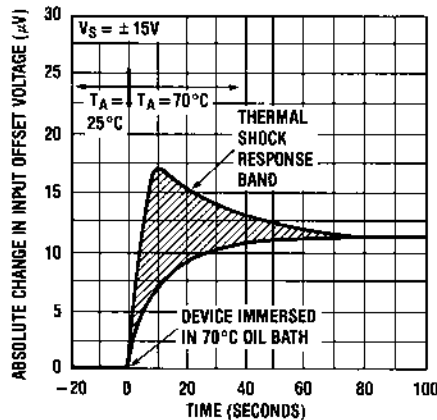
Long Term Drift of Representative Units



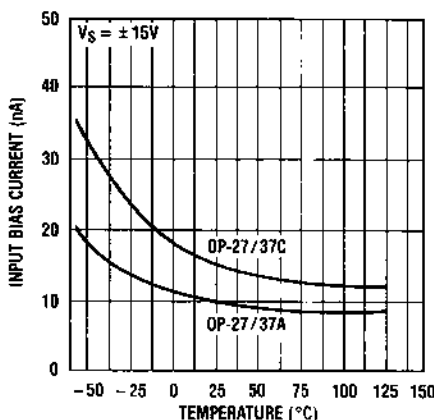
Warm-Up Drift



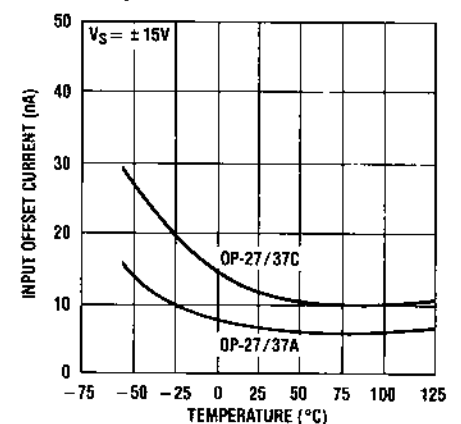
Offset Voltage Change Due to Thermal Shock



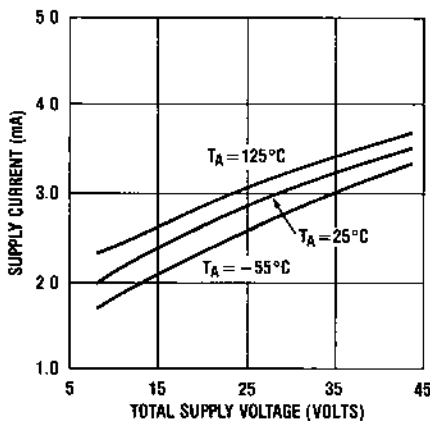
Input Bias Current vs Temperature



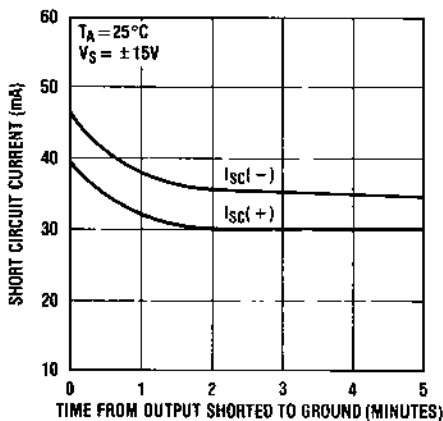
Input Offset Current vs Temperature



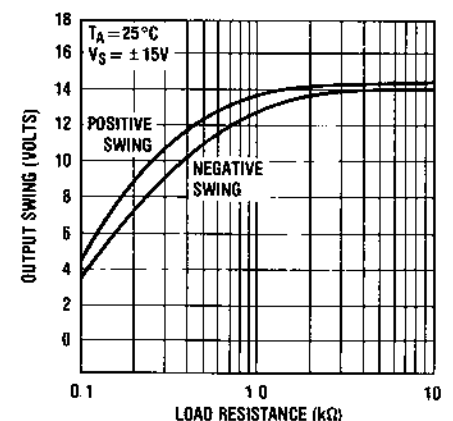
Supply Current vs Supply Voltage



Short Circuit Current vs Time

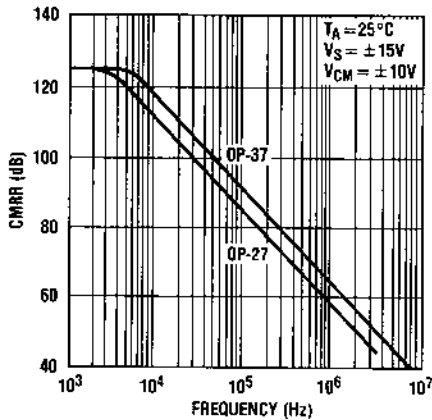


Maximum Output Swing vs Resistive Load

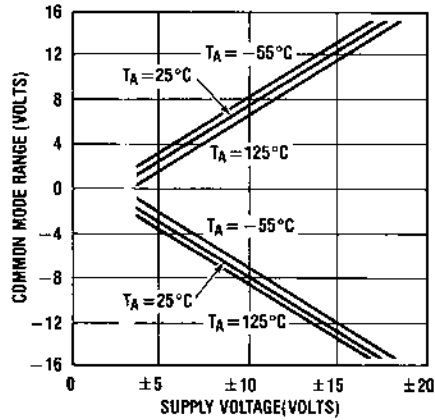


TYPICAL PERFORMANCE CHARACTERISTICS

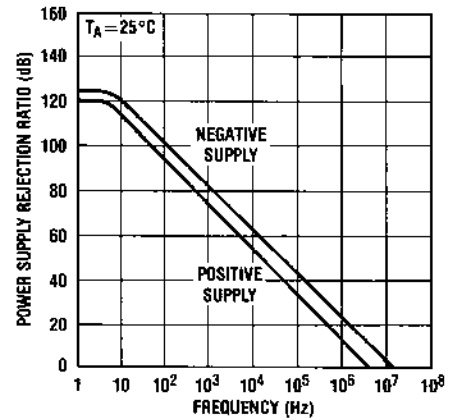
Common Mode Rejection vs Frequency



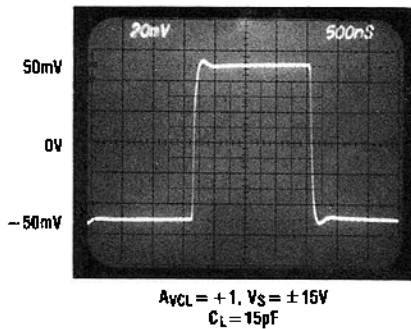
Common Mode Input Range vs Supply Voltage



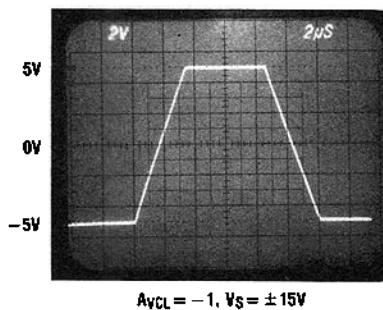
PSRR vs Frequency



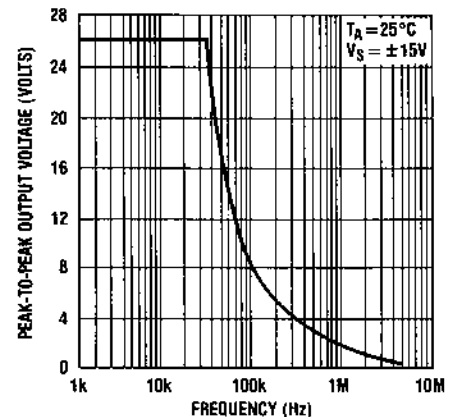
OP-27 Small Signal Transient Response



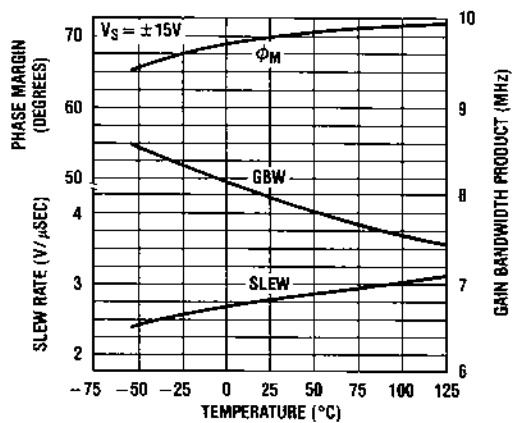
OP-27 Large Signal Transient Response



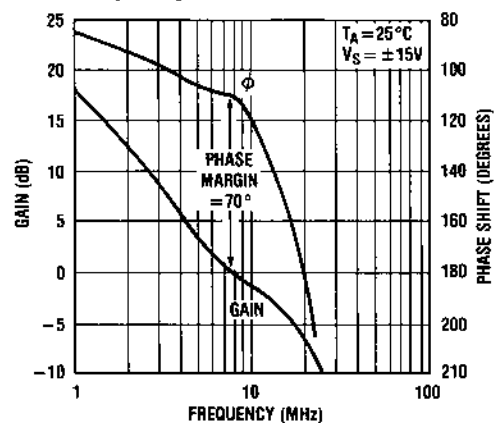
OP-27 Maximum Undistorted Output vs Frequency



OP-27 Slew Rate, Gain Bandwidth Product, Phase Margin vs Temperature

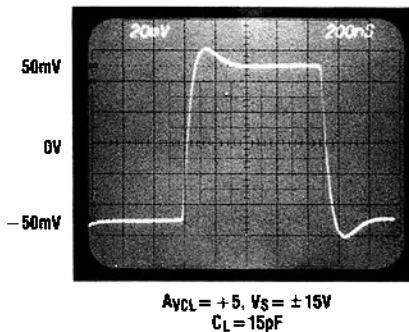


OP-27 Gain, Phase Shift vs Frequency

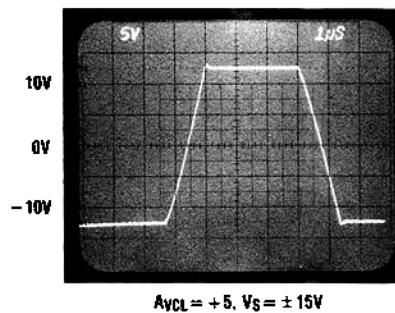


TYPICAL PERFORMANCE CHARACTERISTICS

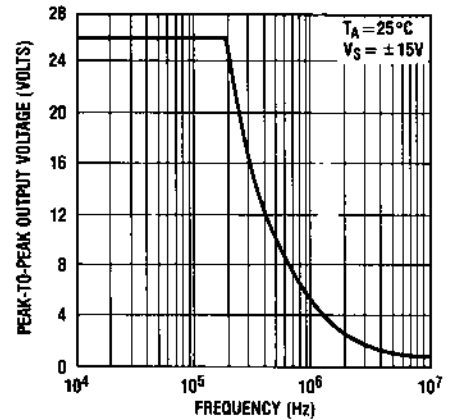
OP-37 Small Signal
Transient Response



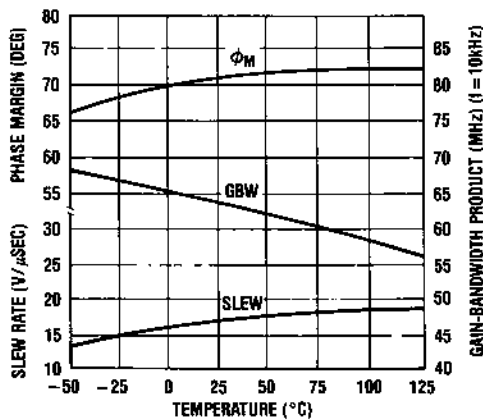
OP-37 Large Signal Response



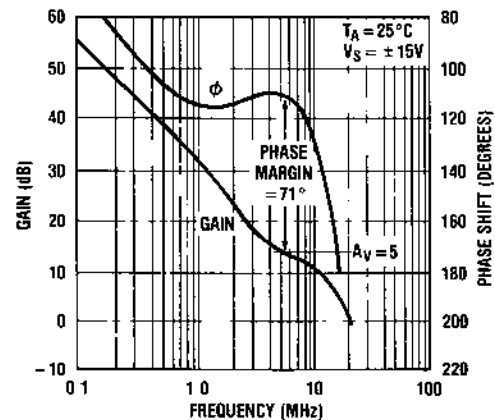
OP-37 Maximum
Undistorted Output vs
Frequency



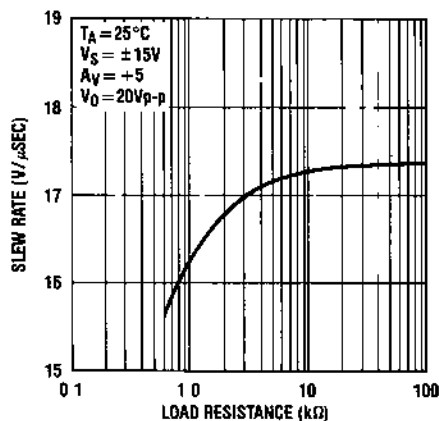
OP-37 Slew Rate, Gain
Bandwidth Product, Phase
Margin vs Temperature



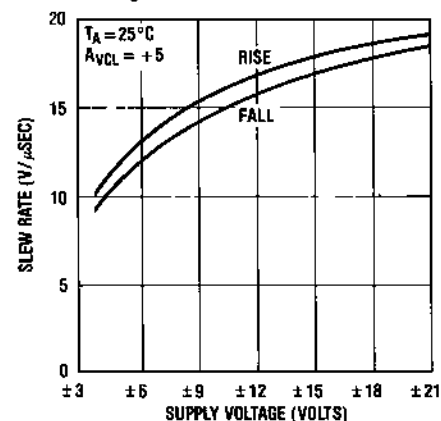
OP-37 Gain, Phase Shift vs
Frequency



OP-37 Slew Rate vs Load



OP-37 Slew Rate vs Supply
Voltage



APPLICATIONS INFORMATION

General

The OP-27/37 series devices may be inserted directly into OP-07, OP-05, 725, and 5534 sockets with or without removal of external compensation or nulling components. In addition, the OP-27/37 may be fitted to 741 sockets with the removal or modification of external nulling components.

Noise Testing

The 0.1Hz to 10Hz peak-to-peak noise of the OP-27/OP-37 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

Measuring the typical 80nV peak-to-peak noise performance of the OP-27/37 requires special test precautions:

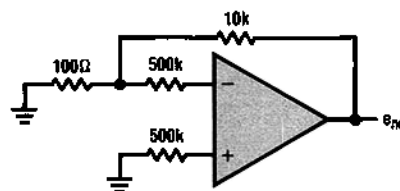
- The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 4μV due to its chip temperature increasing 10°C to 20°C from the moment the power supplies are turned on. In the 10 second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

- For similar reasons, the device must be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.
- Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

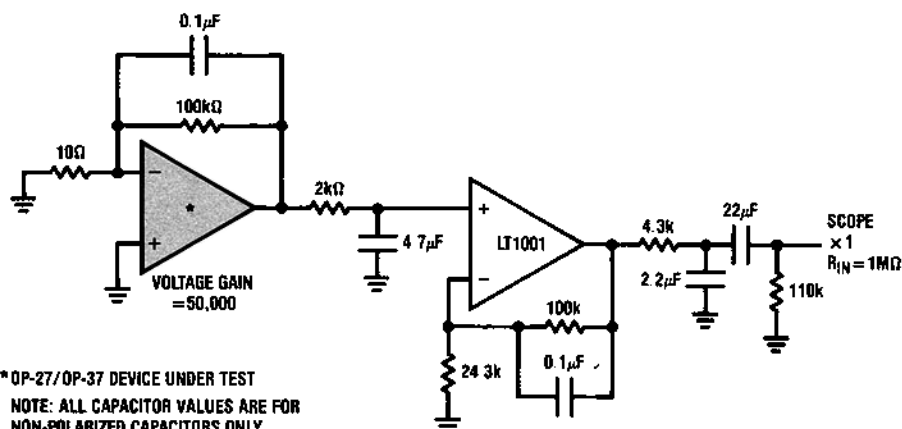
A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

Current noise is measured and calculated by the following formula:

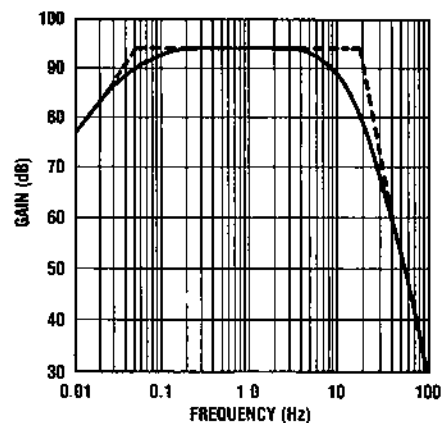
$$i_n = \frac{[e^2_{no} - (130\text{nV})^2]^{1/2}}{1\text{M}\Omega \times 100}$$



0.1Hz to 10Hz Noise Test Circuit



0.1Hz to 10Hz p-p Noise Tester Frequency Response

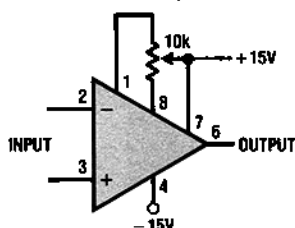


APPLICATIONS INFORMATION

Offset Voltage Adjustment

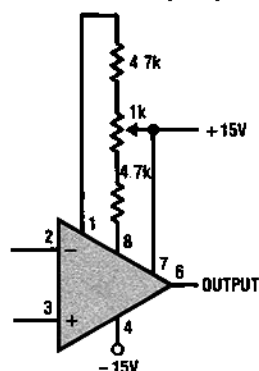
The input offset voltage of the OP-27/37, and its drift with temperature, are permanently trimmed at wafer testing to a low level. However, if further adjustment of V_{OS} is necessary, the use of a 10k nulling potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of $(V_{OS}/300) \mu\text{V}/^\circ\text{C}$, e.g., if V_{OS} is adjusted to $300 \mu\text{V}$, the change in drift will be $1 \mu\text{V}/^\circ\text{C}$.

Standard Adjustment



The adjustment range with a 10k pot is approximately $\pm 2.5\text{mV}$. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example has an approximate null range of $\pm 200 \mu\text{V}$.

Improved Sensitivity Adjustment

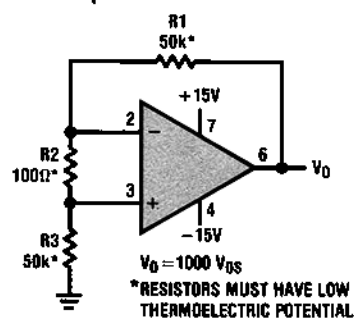


Offset Voltage and Drift

Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

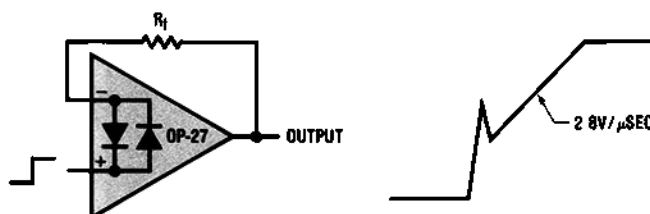
The circuit shown to measure offset voltage is also used as the burn-in configuration for the OP-27/37, with the supply voltages increased to $\pm 20\text{V}$, $R_1 = R_3 = 10\text{k}$, $R_2 = 200\Omega$, $A_V = 100$.

Test Circuit for Offset Voltage and Offset Voltage Drift with Temperature



Unity Gain Buffer Applications (OP-27 Only)

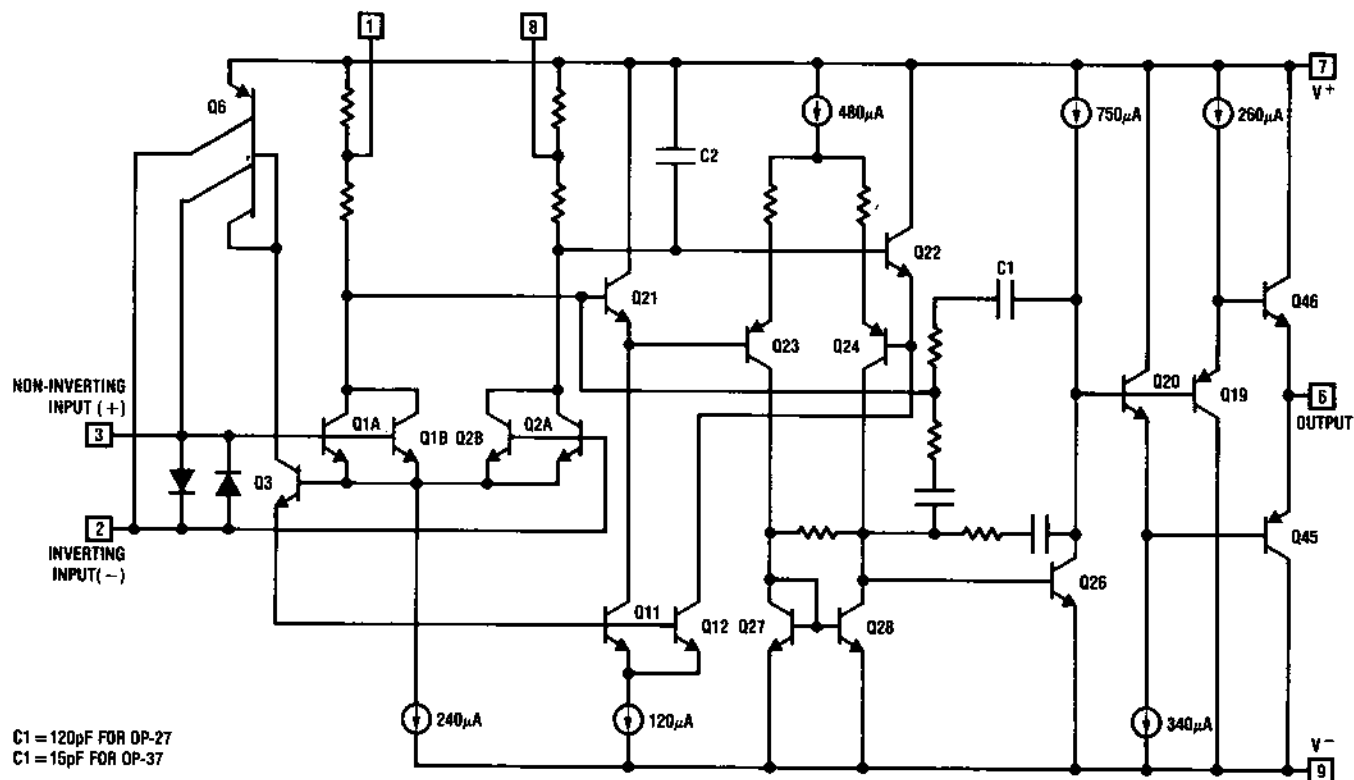
When $R_f \leq 100\Omega$ and the input is driven with a fast, large signal pulse ($> 1\text{V}$), the output waveform will look as shown in the pulsed operation diagram.



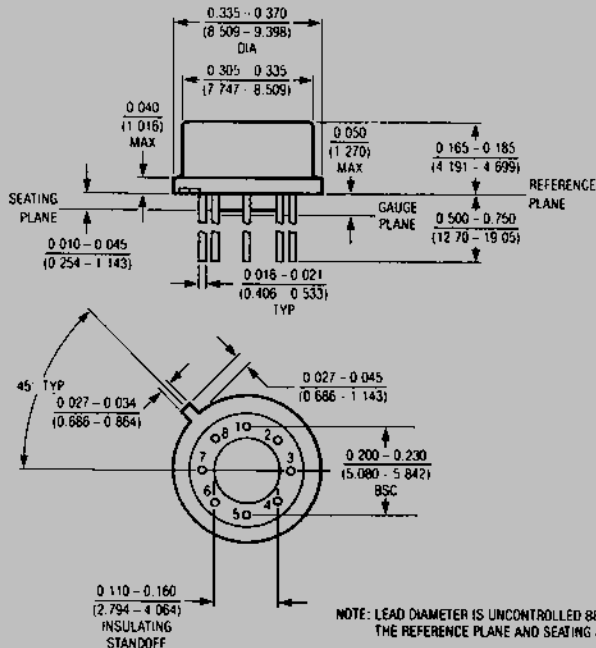
During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20\text{mA}$ at 10V) and the amplifier stays in its active mode and a smooth transition will occur.

As with all operational amplifiers when $R_f > 2\text{k}\Omega$, a pole will be created with R_f and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20pF to 50pF) in parallel with R_f will eliminate this problem.

SCHEMATIC DIAGRAM

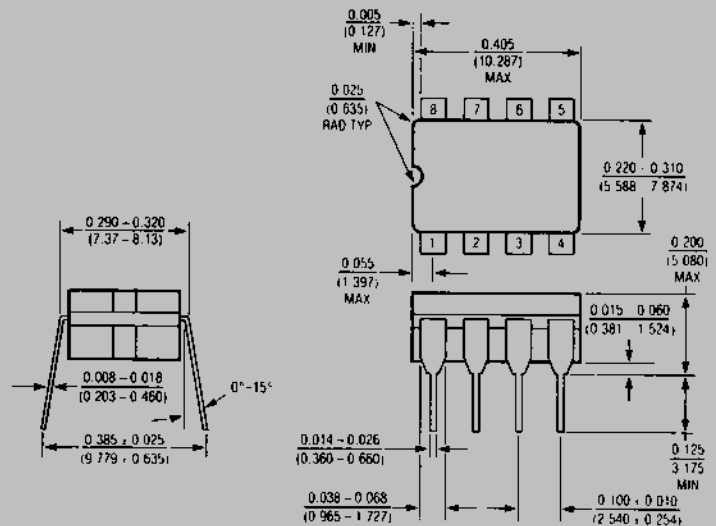


PACKAGE DESCRIPTION

H Package
Metal Can

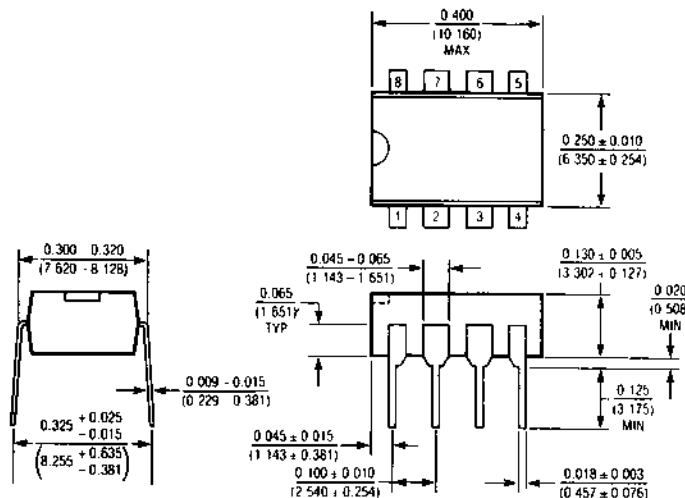
NOTE: DIMENSIONS IN INCHES (MILLIMETERS)

T_{max}	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

J8 Package
8 Lead Hermetic DIPNOTE: DIMENSIONS IN INCHES (MILLIMETERS) UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

OBSOLETE PACKAGE

T_{max}	θ_{ja}
150°C	100°C/W

N8 Package
8 Lead PlasticNOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{max}	θ_{ja}
100°C	130°C/W

NOTES
