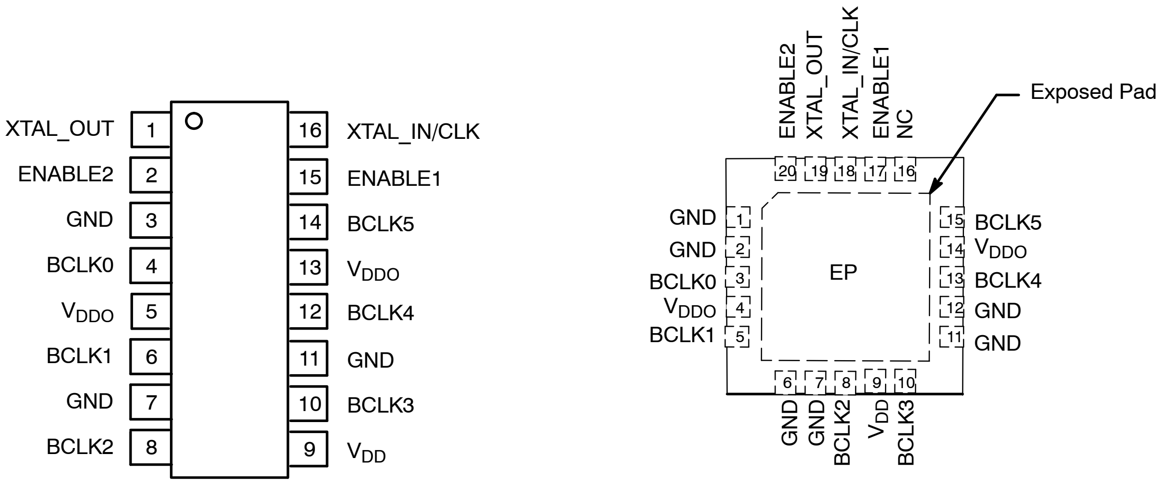


SOIC−16/TSSOP−16

QFN20

Figure 2. Pinout Configuration (Top View)

Table 1. PIN DESCRIPTION

SOIC−16 / TSSOP−16	QFN−20	Name	I/O	Description
1	19	XTAL_OUT	Crystal Interface	Oscillator Output to drive Crystal
2	20	ENABLE 2	LVTTL / LVCMOS Input	Synchronous Enable Input for BCLK5 Output. Switches only when HIGH. Open default condition HIGH due to an internal pullup resistor to V_{CC}.
3, 7, 11	1, 2, 6, 7, 11, 12	GND	GND	GND Supply pins. All GND, V_{DD} and V_{DDO} pins must be externally connected to power supply to guarantee proper operation.
4, 6, 8, 10, 12, 14	3, 5, 8, 10, 13, 15	BCLK0, 1, 2, 3, 4, 5	LVCMOS Outputs	Buffered Clock Outputs
5, 13	4, 14	V_{DDO}	POWER	Positive Supply voltage for outputs. All GND, V_{DD} and V_{DDO} pins must be externally connected to power supply to guarantee proper operation. Bypass with 0.01 μF cap to GND.
9	9	V_{DD}	POWER	Positive Supply voltage for core. All GND, V_{DD} and V_{DDO} pins must be externally connected to power supply to guarantee proper operation. Bypass with 0.01 μF cap to GND.
–	16	NC		No Connect
15	17	ENABLE 1	LVTTL / LVCMOS Input	Synchronous Enable Input for BCLK0/1/2/3/4 Output block. Switches only when HIGH. Open default condition HIGH due to an internal pullup resistor to V_{CC}
16	18	XTAL_IN/ CLK	Crystal Interface	Oscillator Input from Crystal. Single ended Clock Input.
–	EP		–	The Exposed Pad (EP) on the QFN−20 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to GND on the PC board.

Table 2. CLOCK ENABLE FUNCTION TABLE

Control Inputs		Outputs	
ENABLE1*	**ENABLE2***	**BCLK0:BCLK4**	**BCLK5**
0	0	LOW	LOW
0	1	LOW	Toggling
1	0	Toggling	LOW
1	1	Toggling	Toggling

*Defaults HIGH when floating open.

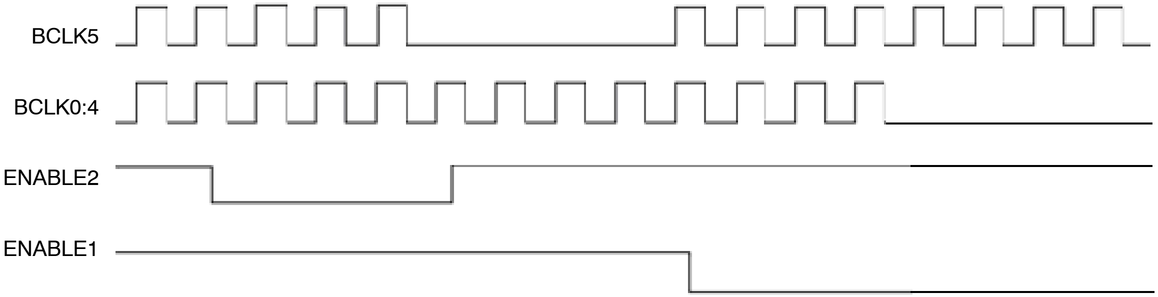


Figure 3. ENABLEx Control Timing Diagram

The ENABLEx control inputs will synchronously enable or disable the selected output(s). This control detects the falling edge of the internal signal and asserts or de−asserts the output after 3 clock cycles. When ENABLEx is LOW, the outputs are disabled to a LOW state. When ENABLEx is HIGH, the outputs are enabled to toggle.

Table 3. RECOMMENDED CRYSTAL PARAMETERS

Crystal	Fundamental AT−Cut
Frequency	10 to 40 MHz
Load Capacitance*	16−20 pF
Shunt Capacitance, C0	7 pF Max
Equivalent Series Resistance	50 Ω Max
Drive Level	1 mW

*See APPLICATION INFORMATION; Crystal Input Interface for CL loading

Table 4. ATTRIBUTES (Note 1)

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating	Oxygen Index	UL−94 code V−0 A 1/8” 28 to 34
Transistor Count		213 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 5. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 1	Rating	Unit
V_{DDx}	Positive Power Supply	GND = 0 V		4.6	V
V_I	Input Voltage			$-0.5 \leq V_I \leq V_{DD} + 0.5$	V
T_A	Operating Temperature Range, Industrial			-40 to $\leq +85$	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	SOIC−16 SOIC−16	80 55	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 3)	SOIC−16	33−36	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	TSSOP−16 TSSOP−16	138 108	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 3)	TSSOP−16	33−36	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	QFN−20 QFN−20	47 33	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 3)	QFN−20	18	°C/W
T_{sol}	Wave Solder	3 sec @ 248°C		265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 6. DC CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Unit
$V_{DD} = V_{DDO}$ = 3.135 V to 3.465 V (3.3 V ±5%); GND = 0 V, T_A = −40°C to +85°C					
IDD	Core Quiescent Power Supply Current (ENABLEx = LOW)			10	mA
IDDO	Output Quiescent Power Supply Current (ENABLEx = LOW)			5	mA
V_{IH}	Input HIGH Voltage ENABLEx, XTAL_IN/CLK	2		V_{DD} + 0.3 V	V
V_{IL}	Input LOW Voltage ENABLEx, XTAL_IN/CLK	−0.3		0.8	V
V_{OH}	Output HIGH Voltage (Note 4)	2.6			V
V_{OL}	Output LOW Voltage (Note 4)			0.5	V
C_{IN}	Input Capacitance		4		pF
C_{PD}	Power Dissipation Capacitance (per Output) (Note 4)		19		pF
R_{OUT}	Output Impedance (Note 4)		7		Ω
$V_{DD} = V_{DDO}$ = 2.375 V to 2.625 V (2.5 V ±5%); GND = 0 V, T_A = −40°C to +85°C					
IDD	Core Quiescent Power Supply Current (ENABLEx = LOW)			8	mA
IDDO	Output Quiescent Power Supply Current (ENABLEx = LOW)			4	mA
V_{IH}	Input HIGH Voltage ENABLEx, XTAL_IN/CLK	1.7		V_{DD} + 0.3 V	V
V_{IL}	Input LOW Voltage ENABLEx, XTAL_IN/CLK	−0.3		0.7	V
V_{OH}	Output HIGH Voltage (I_{OH} = −1 mA) Output HIGH Voltage (Note 4)	2.0 1.8			V
V_{OL}	Output LOW Voltage (I_{OL} = 1 mA) Output LOW Voltage (Note 4)			0.4 0.45	V
C_{IN}	Input Capacitance		4		pF
C_{PD}	Power Dissipation Capacitance (per Output) (Note 4)		18		pF
R_{OUT}	Output Impedance (Note 4)		7		Ω
$V_{DD} = V_{DDO}$ = 1.6 V to 2.0 V (1.8 V ±0.2 V); GND = 0 V, T_A = −40°C to +85°C					
IDD	Core Quiescent Power Supply Current (ENABLEx = LOW)			5	mA
IDDO	Output Quiescent Power Supply Current (ENABLEx = LOW)			3	mA
V_{IH}	Input HIGH Voltage ENABLEx, XTAL_IN/CLK	$0.65*V_{DD}$		V_{DD} + 0.3 V	V
V_{IL}	Input LOW Voltage ENABLEx, XTAL_IN/CLK	−0.3		$0.35*V_{DD}$	V
V_{OH}	Output HIGH Voltage (Note 4)	$V_{DDO}-0.3$			V
V_{OL}	Output LOW Voltage (Note 4)			0.35	V
C_{IN}	Input Capacitance		4		pF
C_{PD}	Power Dissipation Capacitance (per Output) (Note 4)		16		pF
R_{OUT}	Output Impedance (Note 4)		10		Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Parallel terminated 50 Ω to $V_{DDO}/2$ (see Figure 5).

Table 6. DC CHARACTERISTICS (continued)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{DD} = 3.135 V to 3.465 V (3.3 V ±5%); V_{DDO} = 2.375 V to 2.625 V (2.5 V ±5%); GND = 0 V, T_A = −40°C to +85°C					
IDD	Core Quiescent Power Supply Current (ENABLEx = LOW)			10	mA
IDDO	Output Quiescent Power Supply Current (ENABLEx = LOW)			4	mA
V_{IH}	Input HIGH Voltage ENABLEx, XTAL_IN/CLK	2		V_{DD} + 0.3 V	V
V_{IL}	Input LOW Voltage ENABLEx, XTAL_IN/CLK	−0.3		0.8	V
V_{OH}	Output HIGH Voltage (I_{OH} = −1 mA) Output HIGH Voltage (Note 4)	2.0 1.8			V
V_{OL}	Output LOW Voltage (I_{OL} = 1 mA) Output LOW Voltage (Note 4)			0.4 0.45	V
C_{IN}	Input Capacitance		4		pF
C_{PD}	Power Dissipation Capacitance (per Output) (Note 4)		18		pF
R_{OUT}	Output Impedance (Note 4)		7		Ω
V_{DD} = 3.135 V to 3.465 V (3.3 V ±5%); V_{DDO} = 1.6 V to 2.0 V (1.8 V ±0.2 V.); GND = 0 V, T_A = −40°C to +85°C					
IDD	Core Quiescent Power Supply Current (ENABLEx = LOW)			10	mA
IDDO	Output Quiescent Power Supply Current (ENABLEx = LOW)			3	mA
V_{IH}	Input HIGH Voltage ENABLEx, XTAL_IN/CLK	2		V_{DD} + 0.3 V	V
V_{IL}	Input LOW Voltage ENABLEx, XTAL_IN/CLK	−0.3		0.8	V
V_{OH}	Output HIGH Voltage (Note 4)	V_{DDO}−0.3			V
V_{OL}	Output LOW Voltage (Note 4)			0.35	V
C_{IN}	Input Capacitance		4		pF
C_{PD}	Power Dissipation Capacitance (per Output) (Note 4)		16		pF
R_{OUT}	Output Impedance (Note 4)		10		Ω
V_{DD} = 2.375 V to 2.625 V (2.5 V ±5%); V_{DDO} = 1.6 V to 2.0 V (1.8 V ±0.2 V); GND = 0 V, T_A= −40°C to +85°C					
IDD	Core Quiescent Power Supply Current (ENABLEx = LOW)			8	mA
IDDO	Output Quiescent Power Supply Current (ENABLEx = LOW)			3	mA
V_{IH}	Input HIGH Voltage ENABLEx, XTAL_IN/CLK	1.7		V_{DD} + 0.3 V	V
V_{IL}	Input LOW Voltage ENABLEx, XTAL_IN/CLK	−0.3		0.7	V
V_{OH}	Output HIGH Voltage (Note 4)	V_{DDO}−0.3			V
V_{OL}	Output LOW Voltage (Note 4)			0.35	V
C_{IN}	Input Capacitance		4		pF
C_{PD}	Power Dissipation Capacitance (per Output) (Note 4)		16		pF
R_{OUT}	Output Impedance (Note 4)		10		Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Parallel terminated 50 Ω to $V_{DDO}/2$ (see Figure 5).

Table 7. AC CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Unit
V_{DD} = V_{DDO} = 3.135 V to 3.465 V (3.3 V ± 5%); GND = 0 V, T_A = −40°C to +85°C (Note 5)					
F_{max}	Input Frequency Crystal	3		40	MHz
	Input Frequency Clock (XTAL_IN/CLK)	DC		100	
t_{EN} / t_{DIS}	Delay for Output Enable / Disable Time ENABLEx to BCLKn			4	Cycles
$tSKEW_{DC}$	Duty Cycle Skew (See Figure 4)	48		52	%
$tSKEW_{O-O}$	Output to Output Skew Within A Device (same conditions)	0	50	80	ps
ΦNOISE	Phase−Noise Performance f_{out} = 25 MHz 100 Hz off Carrier 1 kHz off Carrier 10 kHz off Carrier 100 kHz off Carrier		 −123 −142 −153 −164		dBc/Hz
tJIT(Φ)	RMS Phase Jitter 25 MHz carrier, Integration Range 12 kHz to 20 MHz 25 MHz carrier, Integration Range 100 Hz to 1 MHz		 0.08 0.08		ps
tr/tf	Output rise and fall times (20%; 80%)	200		800	ps
V_{DD} = V_{DDO} = 2.375 V to 2.625 V (2.5 V ± 5%); GND = 0 V, T_A = −40°C to +85°C (Note 5)					
F_{max}	Input Frequency Crystal	3		40	MHz
	Input Frequency Clock (XTAL1)	DC		100	
t_{EN} / t_{DIS}	Delay for Output Enable / Disable Time ENABLEx to BCLKn			4	Cycles
$tSKEW_{DC}$	Duty Cycle Skew (See Figure 4)	47		53	%
$tSKEW_{O-O}$	Output to Output Skew Within A Device (same conditions)	0	50	80	ps
ΦNOISE	Phase−Noise Performance f_{out} = 25 MHz 100 Hz off Carrier 1 kHz off Carrier 10 kHz off Carrier 100 kHz off Carrier		 −118 −137 −151 −165		dBc/Hz
tJIT(Φ)	RMS Phase Jitter 25 MHz carrier, Integration Range 12 kHz to 20 MHz 25 MHz carrier, Integration Range 100 Hz to 1 MHz		 0.13 0.13		ps
tr/tf	Output rise and fall times (20%; 80%)	200		800	ps
V_{DD} = V_{DDO} = 1.6 V to 2.0 V (1.8 V ± 0.2 V); GND = 0 V, T_A = −40°C to +85°C (Note 5)					
F_{max}	Input Frequency Crystal	3		40	MHz
	Input Frequency Clock (XTAL1)	DC		100	
t_{EN} / t_{DIS}	Delay for Output Enable / Disable Time ENABLEx to BCLKn			4	Cycles
$tSKEW_{DC}$	Duty Cycle Skew (See Figure 4)	47		53	%
$tSKEW_{O-O}$	Output to Output Skew Within A Device (same conditions)	0	50	80	ps
ΦNOISE	Phase−Noise Performance f_{out} = 25 MHz 100 Hz off Carrier 1 kHz off Carrier 10 kHz off Carrier 100 kHz off Carrier		 −129 −145 −147 −157		dBc/Hz
tJIT(Φ)	RMS Phase Jitter 25 MHz carrier, Integration Range 12 kHz to 20 MHz 25 MHz carrier, Integration Range 100 Hz to 1 MHz		 0.27 0.27		ps
tr/tf	Output rise and fall times (20%; 80%)	200		900	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Crystal inputs ≤ F_{max}. Outputs loaded with 50 Ω to $V_{DDO}/2$. CLOCK (LVCMOS levels at XTAL1 input) 50% duty cycle. See Figures 4 and 7. See APPLICATION INFORMATION; Crystal Input Interface for CL loading.

Table 7. AC CHARACTERISTICS (continued)

Symbol	Characteristic	Min	Typ	Max	Unit

V_{DD} = 3.135 V to 3.465 V (3.3 V ±5%); V_{DDO} = 2.375 V to 2.625 V (2.5 V ±5%); GND = 0 V, T_A = –40°C to +85°C (Note 5)

F_{max}	Input Frequency Crystal	3		40	MHz
	Input Frequency Clock (XTAL_IN/CLK)	DC		100	
t_{EN} / t_{DIS}	Delay for Output Enable / Disable Time ENABLEx to BCLKn			4	Cycles
$tSKEW_{DC}$	Duty Cycle Skew (See Figure 4)	48		52	%
$tSKEW_{O-O}$	Output to Output Skew Within A Device (same conditions)	0	50	80	ps
ΦNOISE	Phase–Noise Performance f_{out} = 25 MHz 100 Hz off Carrier 1 kHz off Carrier 10 kHz off Carrier 100 kHz off Carrier		 –129 –145 –147 –157		dBc/Hz
tJIT(Φ)	RMS Phase Jitter 25 MHz carrier, Integration Range 12 kHz to 20 MHz 25 MHz carrier, Integration Range 100 Hz to 1 MHz		 0.14 0.14		ps
tr/tf	Output rise and fall times (20%; 80%)	200		800	ps

V_{DD} = 3.135 V to 3.465 V (3.3 V ±5%); V_{DDO} = 1.6 V to 2.0 V (1.8 V ±0.2 V); GND = 0 V, T_A = –40°C to +85°C (Note 5)

F_{max}	Input Frequency Crystal	3		40	MHz
	Input Frequency Clock (XTAL1)	DC		100	
t_{EN} / t_{DIS}	Delay for Output Enable / Disable Time ENABLEx to BCLKn			4	Cycles
$tSKEW_{DC}$	Duty Cycle Skew (See Figure 4)	48		52	%
$tSKEW_{O-O}$	Output to Output Skew Within A Device (same conditions)	0	50	80	ps
ΦNOISE	Phase–Noise Performance f_{out} = 25 MHz 100 Hz off Carrier 1 kHz off Carrier 10 kHz off Carrier 100 kHz off Carrier		 –129 –145 –147 –157		dBc/Hz
tJIT(Φ)	RMS Phase Jitter 25 MHz carrier, Integration Range 12 kHz to 20 MHz 25 MHz carrier, Integration Range 100 Hz to 1 MHz		 0.18 0.18		ps
tr/tf	Output rise and fall times (20%; 80%)	200		900	ps

V_{DD} = 2.375 V to 2.625 V (2.5 V ±5%); V_{DDO} = 1.6 V to 2.0 V (1.8 V ±0.2 V); GND = 0 V, T_A = –40°C to +85°C (Note 5)

F_{max}	Input Frequency Crystal	3		40	MHz
	Input Frequency Clock (XTAL1)	DC		100	
t_{EN} / t_{DIS}	Delay for Output Enable / Disable Time ENABLEx to BCLKn			4	Cycles
$tSKEW_{DC}$	Duty Cycle Skew (See Figure 4)	47		53	%
$tSKEW_{O-O}$	Output to Output Skew Within A Device (same conditions)	0	50	80	ps
ΦNOISE	Phase–Noise Performance f_{out} = 25 MHz/ 100 Hz off Carrier 1 kHz off Carrier 10 kHz off Carrier 100 kHz off Carrier		 –129 –145 –147 –157		dBc/Hz
tJIT(Φ)	RMS Phase Jitter 25 MHz carrier, Integration Range 12 kHz to 20 MHz 25 MHz carrier, Integration Range 100 Hz to 1 MHz		 0.19 0.19		ps
tr/tf	Output rise and fall times (20%; 80%)	200		900	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Crystal inputs ≤ F_{max}. Outputs loaded with 50 Ω to $V_{DDO}/2$. CLOCK (LVCMOS levels at XTAL1 input) 50% duty cycle. See Figures 4 and 7. See APPLICATION INFORMATION; Crystal Input Interface for CL loading.

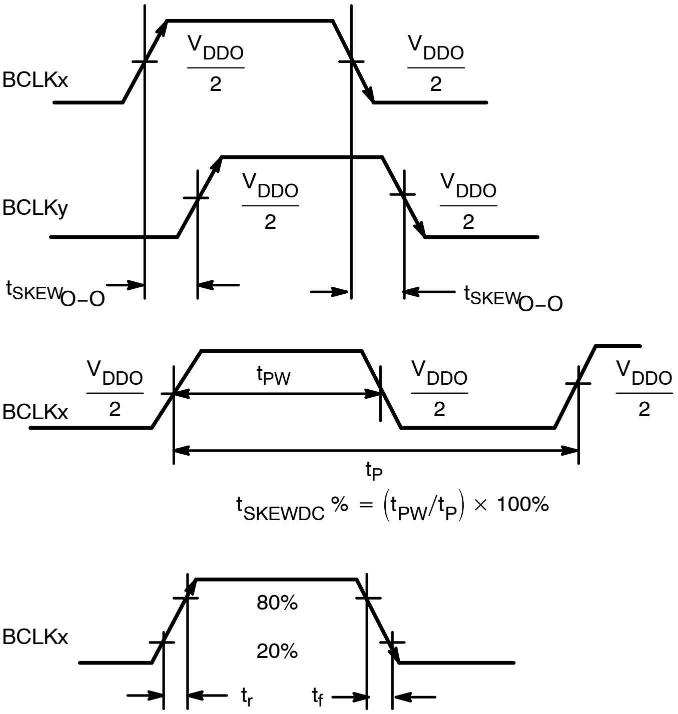
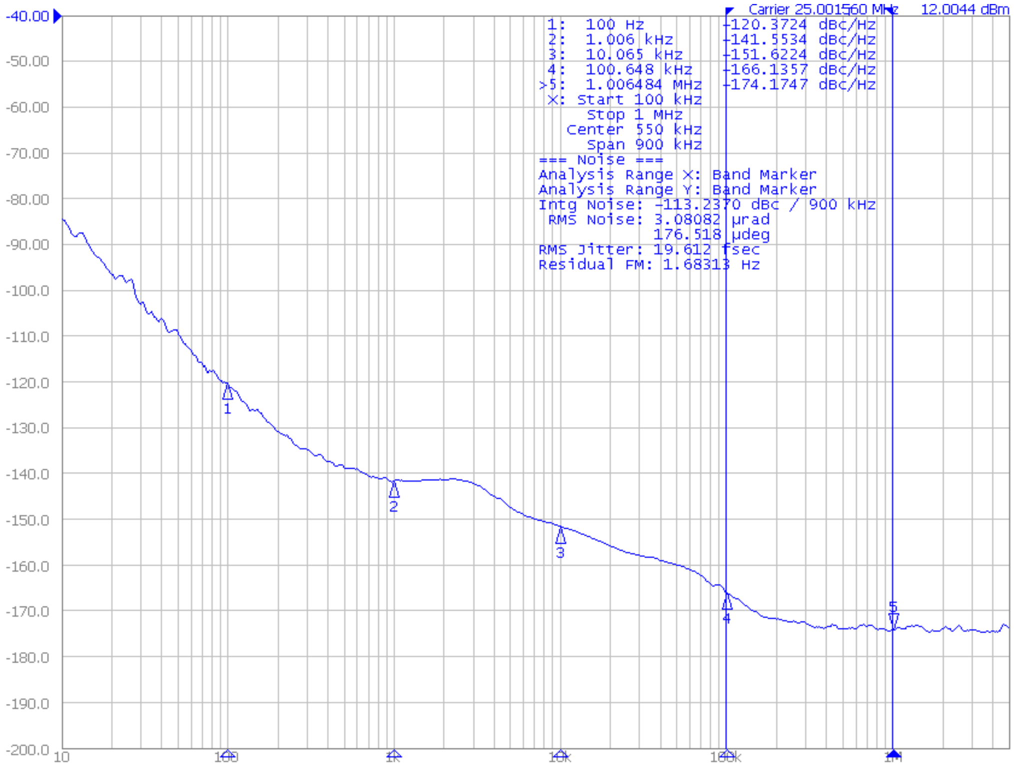


Figure 4. AC Reference Measurement



```
Carrier 25.001560 MHz    12.0044 dBm
 1:  100 Hz            -120.3724 dBc/Hz
 2:  1.006 kHz         -141.5534 dBc/Hz
 3:  10.065 kHz        -151.6224 dBc/Hz
 4:  100.648 kHz       -166.1357 dBc/Hz
>5:  1.006484 MHz      -174.1747 dBc/Hz
 X: Start 100 kHz
      Stop 1 MHz
    Center 550 kHz
      Span 900 kHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -113.2370 dBc / 900 kHz
 RMS Noise: 3.08082 µrad
            176.518 µdeg
RMS Jitter: 19.612 fsec
Residual FM: 1.68313 Hz
```

Figure 5. Typical Phase Noise Plot of the NB3H83905C Operating at 25 MHz $V_{DD} = V_{DDO} = 3.3$ V

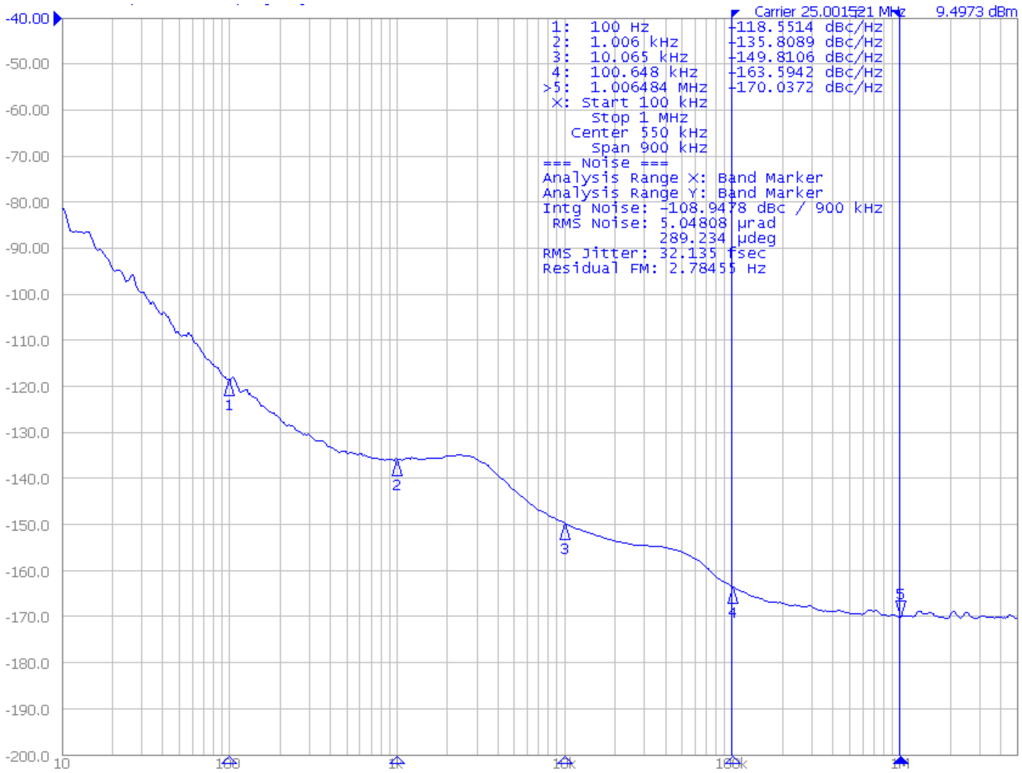


Figure 6. Typical Phase Noise Plot of the NB3H83905C Operating at 25 MHz $V_{DD} = V_{DDO} = 2.5$ V

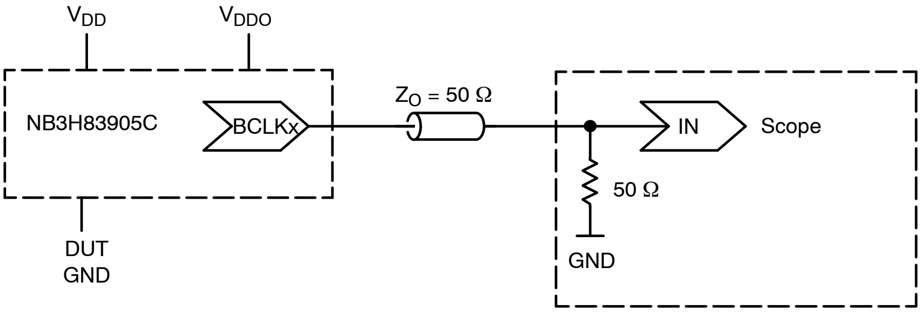


Figure 7. Typical Device Evaluation and Termination Setup – See Table 8

Table 8. TEST SUPPLY SETUP. V_{DDO} SUPPLY MAY BE CENTERED ON 0.0 V (SCOPE GND) TO PERMIT DIRECT CONNECTION INTO “50 Ω TO GND” SCOPE MODULE. V_{DD} SUPPLY TRACKS DUT GND PIN

Spec Condition:	Test Setup V_{DD}:	Test Setup V_{DDO}:	Test Setup DUT GND:
$V_{DD} = V_{DDO}$ = 3.135 V to 3.465 V (3.3 V ±5%)	1.56 to 1.73 V	1.56 to 1.73 V	–1.56 to –1.73 V
$V_{DD} = V_{DDO}$ = 2.375 V to 2.625 V (2.5 V ±5%)	1.1875 to 1.3125 V	1.1875 to 1.3125 V	–1.1875 to –1.3125 V
$V_{DD} = V_{DDO}$ = 1.6 V to 2.0 V (1.8 V ±0.2 V)	0.8 to 1.0 V	0.8 to 1.0 V	–0.8 to –1.0 V
V_{DD} = 3.135 V to 3.465 V (3.3 V ±5%); V_{DDO} = 2.375 V to 2.625 V (2.5 V ±5%)	1.955 to 2.1525 V	1.1875 to 1.3125 V	–1.1875 to –1.3125 V
V_{DD} = 3.135 V to 3.465 V (3.3 V ±5%); V_{DDO} = 1.6 V to 2.0 V (1.8 V ±0.2 V)	2.335 to 2.465 V	0.8 to 1.0 V	–0.8 to –1.0 V
V_{DD} = 2.375 V to 2.625 V (2.5 V ±5%); V_{DDO} = 1.6 V to 2.0 V (1.8 V ±0.2 V)	1.575 to 1.625 V	0.8 to 1.0 V	–0.8 to –1.0 V

APPLICATION INFORMATION

Crystal Input Interface

Figure 8 shows the NB3H83905C device crystal oscillator interface using a typical parallel resonant crystal. A parallel crystal with loading capacitance C_L = 18 pF would use C1 = 32 pF and C2 = 32 pF as nominal values, assuming 4 pF of stray cap per line. The frequency accuracy and duty cycle skew can be fine tuned by adjusting the C1 and C2 values. For example, increasing the C1 and C2 values will reduce the operational frequency. Note R1 is optional and may be 0 Ω.

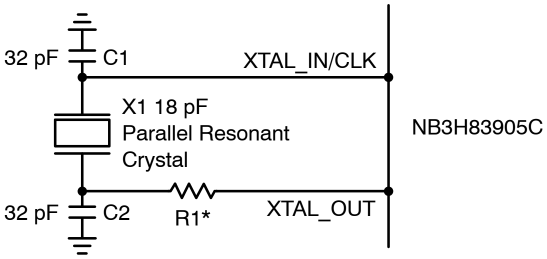


Figure 8. NB3H83905C Crystal Oscillator Interface
*** R1 is optional**

Termination

NB3H83905C device output series termination may be used by locating a 28 Ω series resistor at the driver pin as shown in Figure 9. Alternatively, a Thevenin Parallel termination may be used by locating a 100 Ω pullup resistor to V_{DD} and a 100 Ω pullup resistor to GND at the receiver pin, instead of an Rs source termination resistor, Figure 10.

Unused Input and Output Pins

All LVCMOS control pins have internal pull–ups or pull–downs; additional external resistors are not required (optionally 1 kΩ resistors may be used). All unused LVCMOS outputs can be left floating with no trace attached.

Bypass

The V_{DD} and V_{DDO} supply pins should be bypassed with both a 10 μF and a 0.1 μF cap from supply pins to GND.

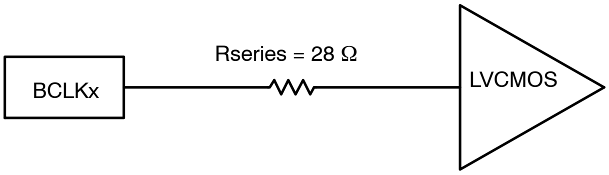


Figure 9. Series Termination

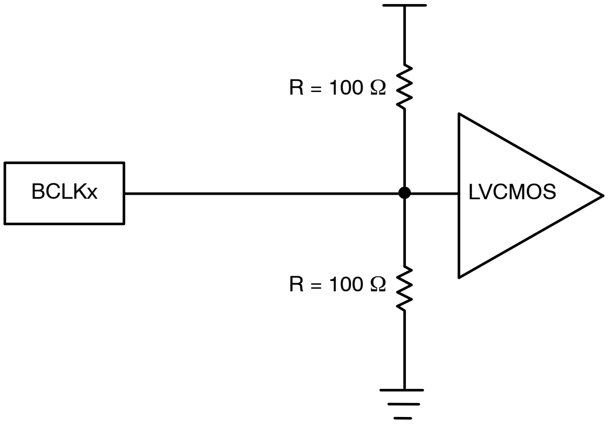
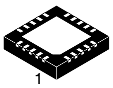


Figure 10. Optional Thevenin Termination

ORDERING INFORMATION

Device	Package	Shipping†
NB3H83905CDG	SOIC–16 (Pb – Free)	48 Units / Rail
NB3H83905CDR2G	SOIC–16 (Pb – Free)	2500 Units / Tape & Reel
NB3H83905CDTG	TSSOP–16 (Pb – Free)	96 Units /Rail
NB3H83905CDTR2G	TSSOP–16 (Pb – Free)	2500 Units / Tape & Reel
NB3H83905CMNG	QFN–20 (Pb–Free)	92 Units / Rail
NB3H83905CMNTXG	QFN–20 Pb–Free)	3000 / Tape & Reel

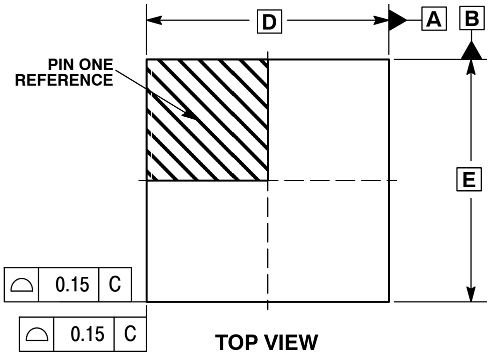
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



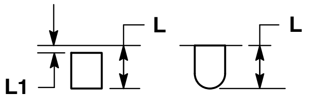
SCALE 2:1

QFN20 4x4, 0.5P
CASE 485BH−01
ISSUE O

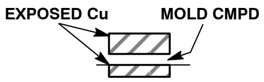
DATE 19 FEB 2010



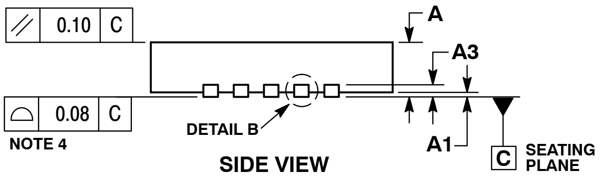
TOP VIEW



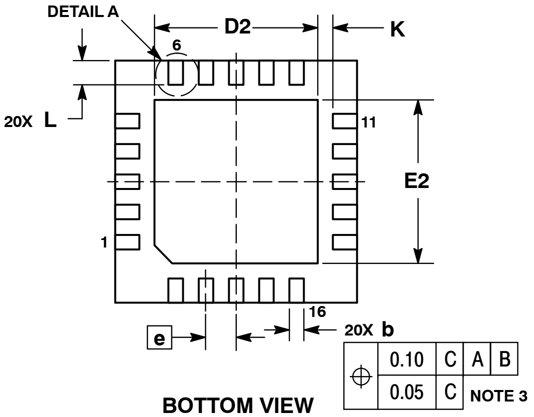
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION



SIDE VIEW

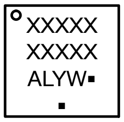


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.60	2.80
E	4.00 BSC	
E2	2.60	2.80
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	0.00	0.15

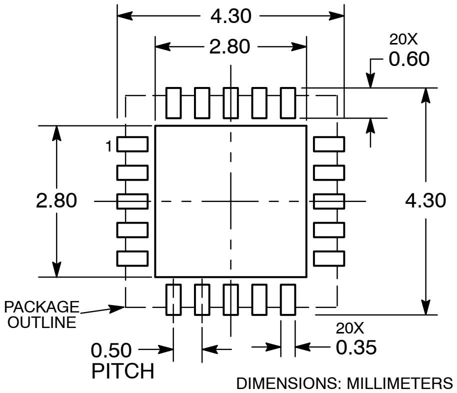
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

MOUNTING FOOTPRINT

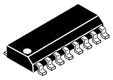


DIMENSIONS: MILLIMETERS

DOCUMENT NUMBER:	**98AON48317E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**QFN20 4X4, 0.5P**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

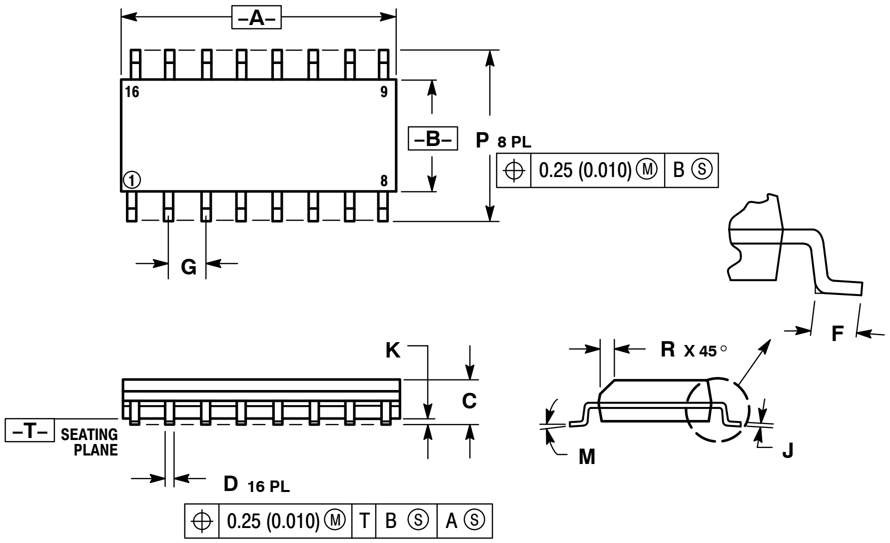
ON Semiconductor®



SCALE 1:1

SOIC−16
CASE 751B−05
ISSUE K

DATE 29 DEC 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

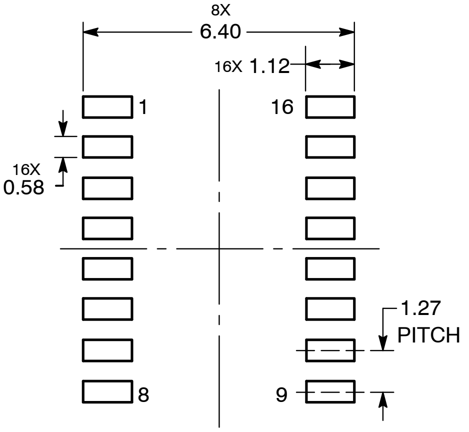
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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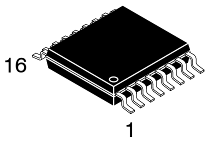
DESCRIPTION:	**SOIC−16**	**PAGE 1 OF 1**

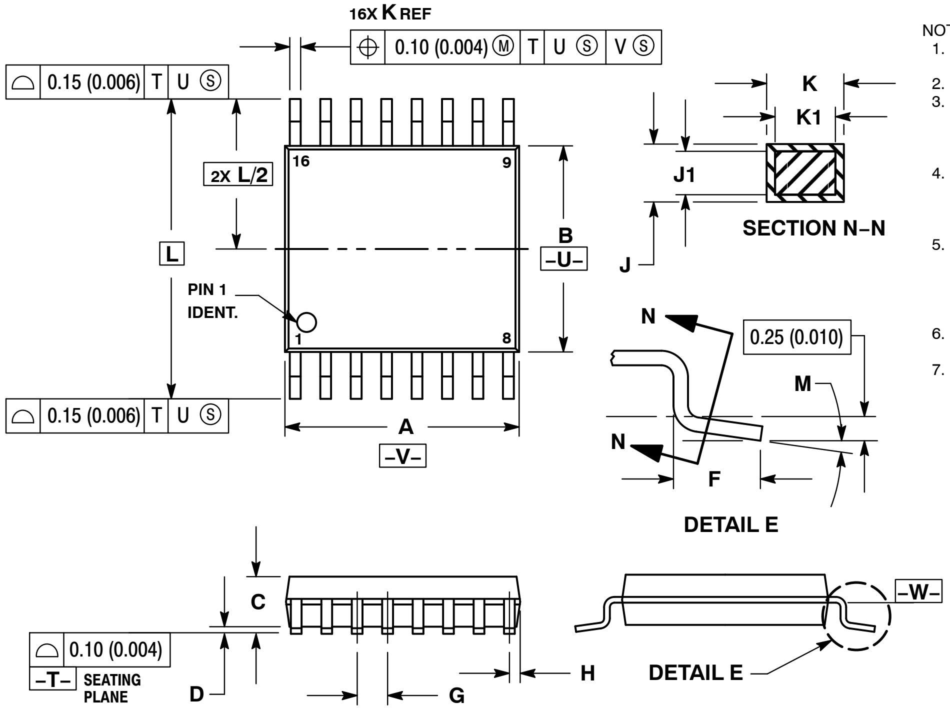


SCALE 2:1

TSSOP−16

CASE 948F−01
ISSUE B

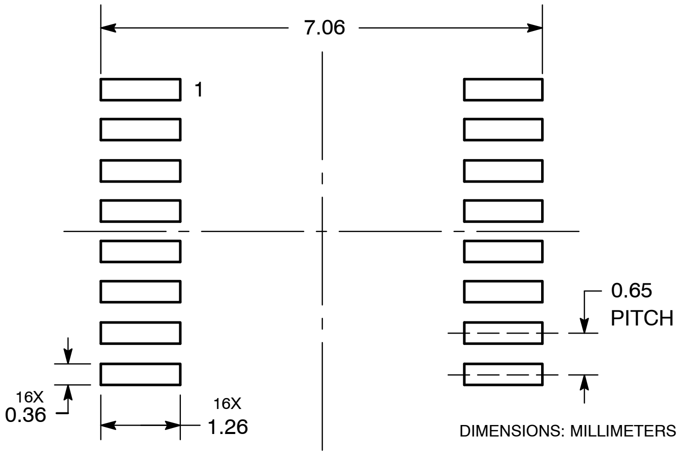
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

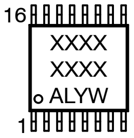
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**TSSOP−16**	**PAGE 1 OF 1**

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