ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage (I_C = 100 μAdc, V_{BE} = 0)		$V_{(BR)CES}$	30	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)		I_{CBO}	–	100	nAdc
Emitter Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}	–	100	nAdc
ON CHARACTERISTICS (Note 3)					
DC Current Gain		h_{FE}			–
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	MMBTA13		5000	–	
	MMBTA14		10,000	–	
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	MMBTA13		10,000	–	
	MMBTA14		20,000	–	
Collector−Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 0.1 mAdc)		$V_{CE(sat)}$	–	1.5	Vdc
Base−Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)		V_{BE}	–	2.0	Vdc
SMALL−SIGNAL CHARACTERISTICS					
Current−Gain − Bandwidth Product (Note 4) (I_C = 10 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	125	–	MHz

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
4. $f_T = |h_{fe}| \bullet f_{test}$.

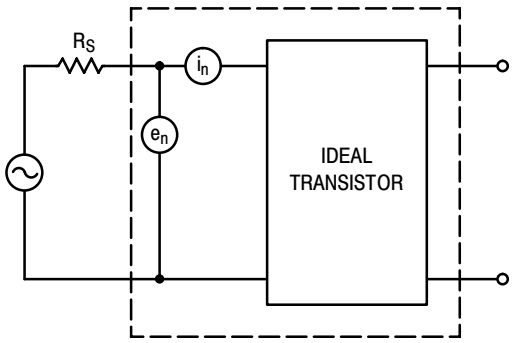


Figure 1. Transistor Noise Model

NOISE CHARACTERISTICS

(V_{CE} = 5.0 Vdc, T_A = 25°C)

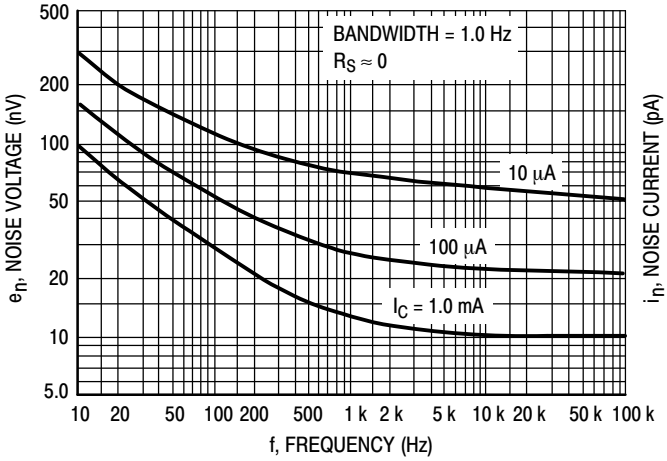


Figure 2. Noise Voltage

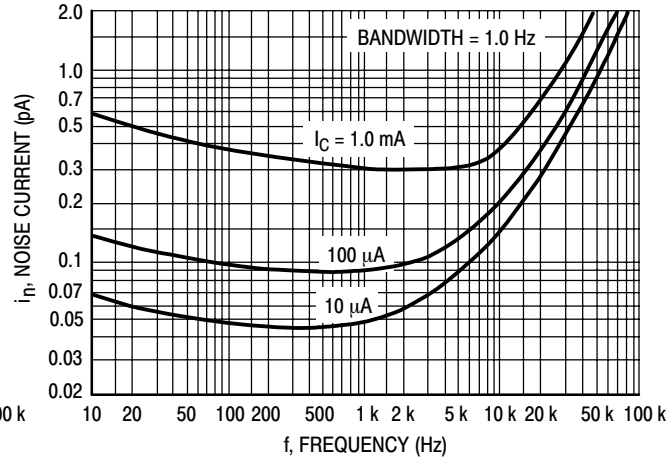


Figure 3. Noise Current

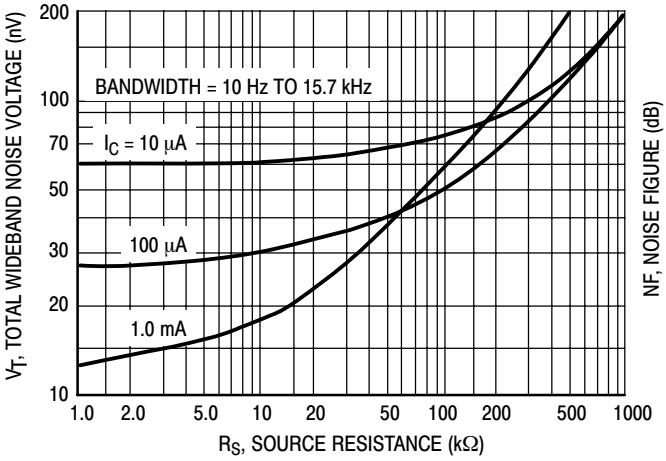


Figure 4. Total Wideband Noise Voltage

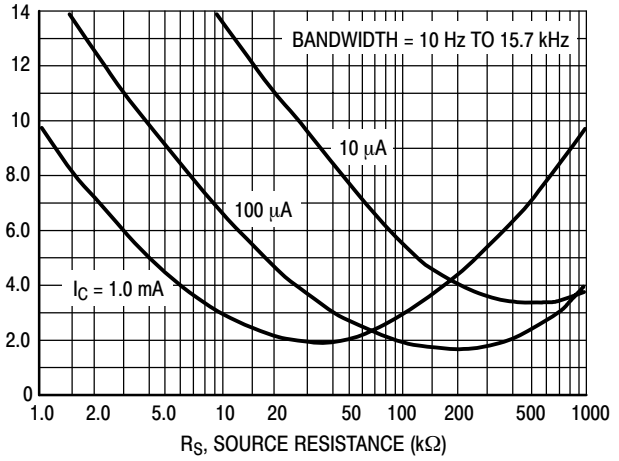


Figure 5. Wideband Noise Figure

SMALL−SIGNAL CHARACTERISTICS

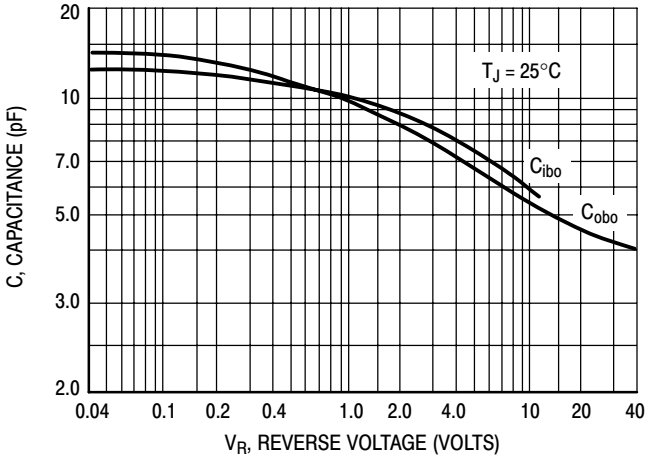


Figure 6. Capacitance

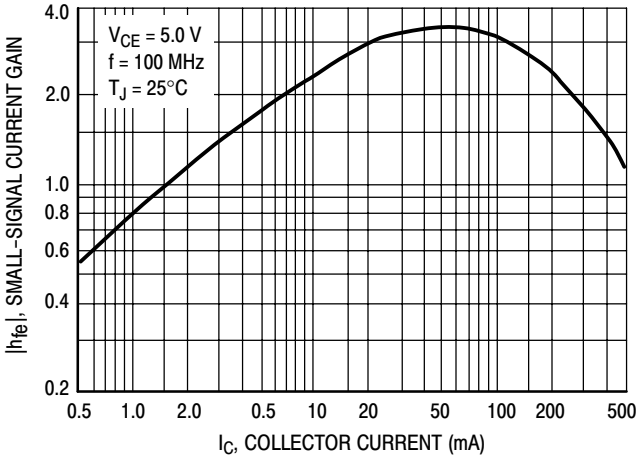


Figure 7. High Frequency Current Gain

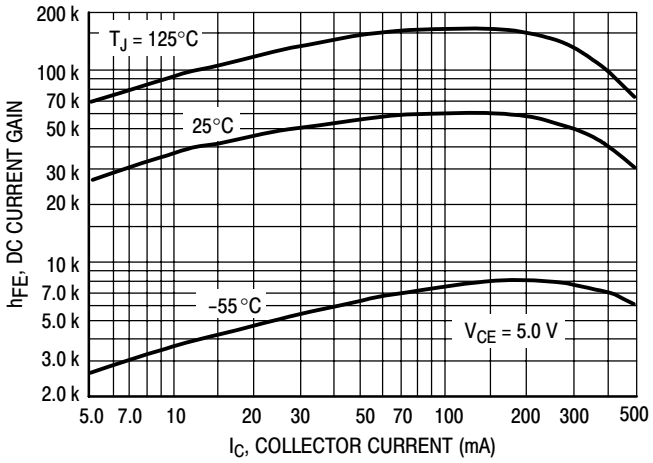


Figure 8. DC Current Gain

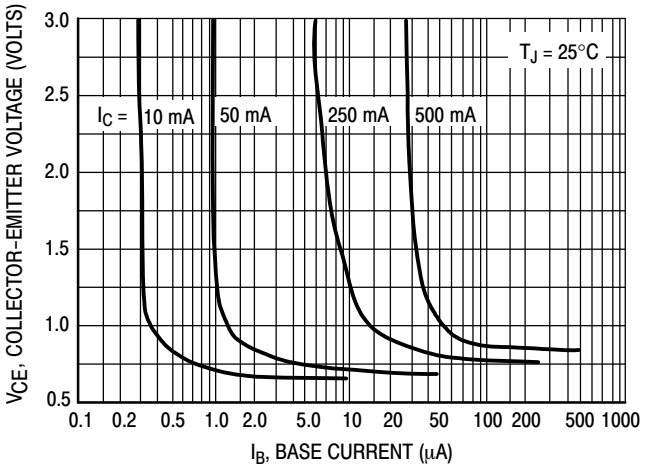


Figure 9. Collector Saturation Region

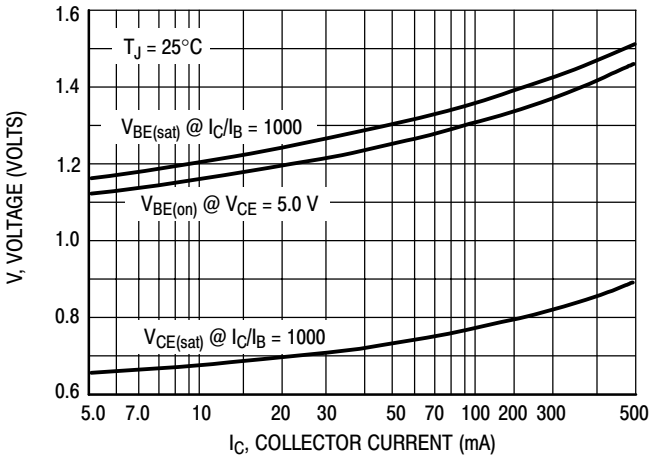


Figure 10. “On” Voltages

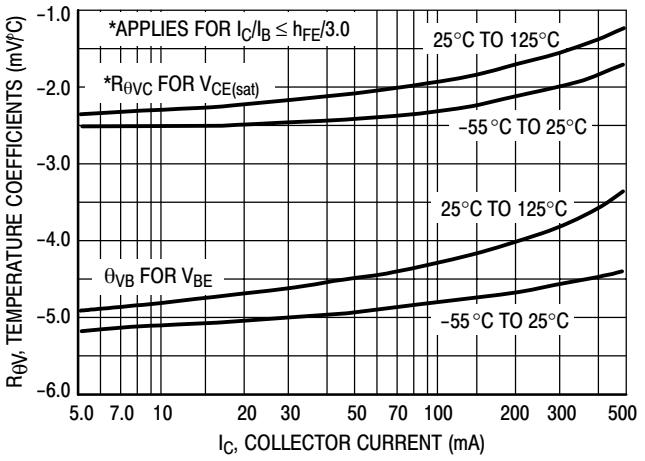


Figure 11. Temperature Coefficients

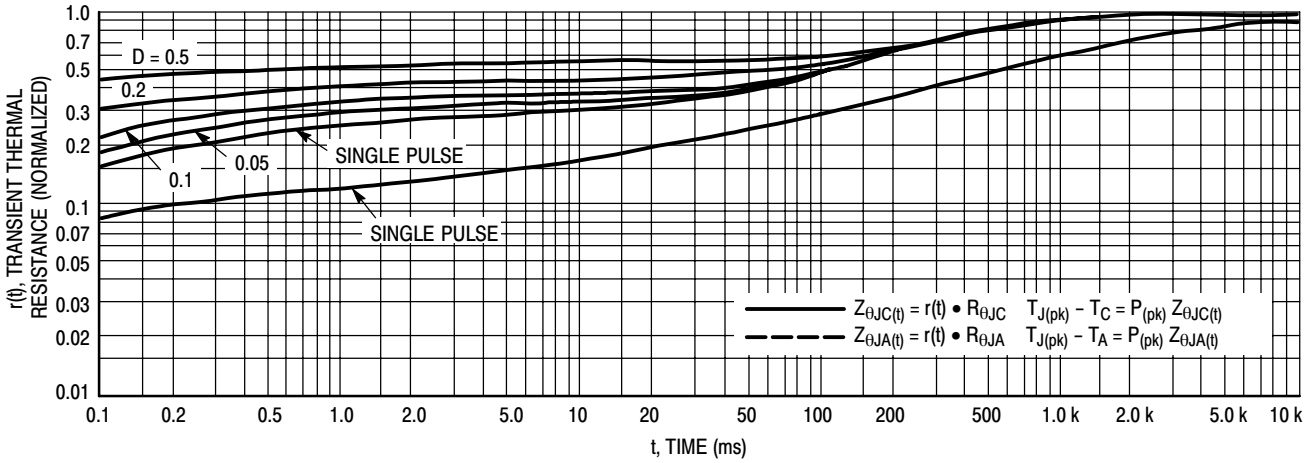


Figure 12. Thermal Response

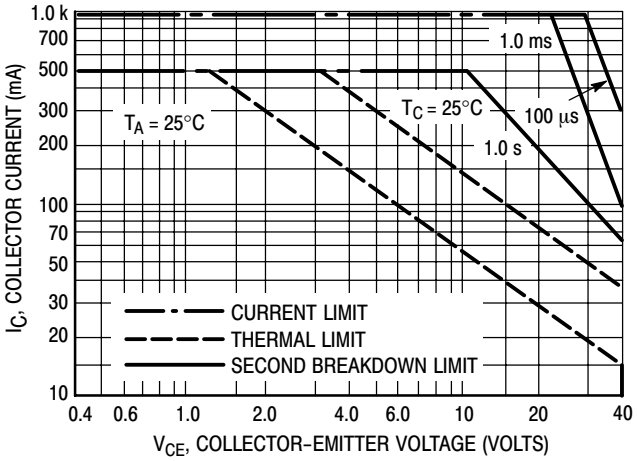
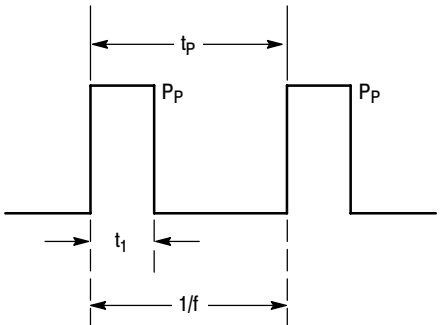


Figure 13. Active Region Safe Operating Area

FIGURE A



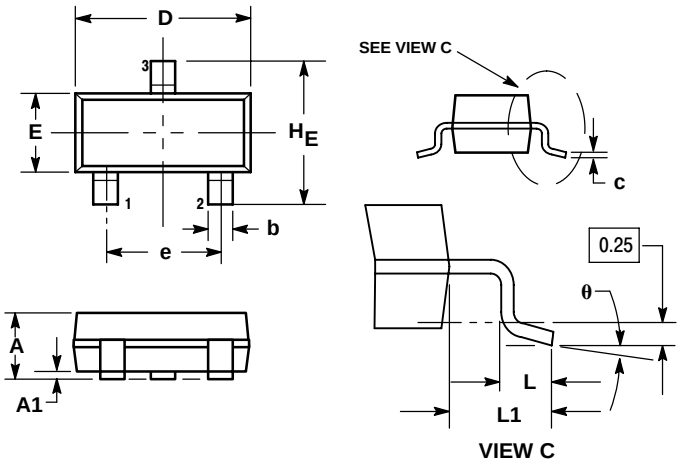
DUTY CYCLE $= t_1 f = \frac{t_1}{t_P}$

PEAK PULSE POWER = P_P

Design Note: Use of Transient Thermal Resistance Data

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AN

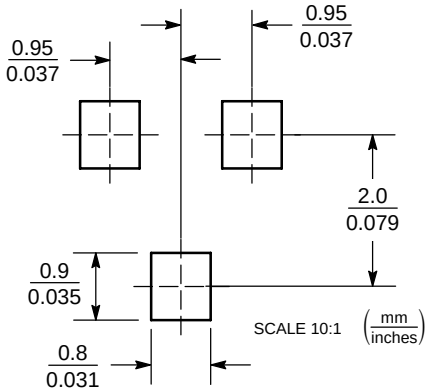


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01 THRU −07 AND −09 OBSOLETE, NEW STANDARD 318−08.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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