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MM74HC175 Quad D-Type Flip-Flop With Clear

General Description

The MM74HC175 high speed D-type flip-flop with complementary outputs utilizes advanced silicon-gate CMOS technology to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Information at the \underline{D} inputs of the MM74HC175 is transferred to the Q and \overline{Q} outputs on the positive going edge of the clock pulse. Both true and complement outputs from each flip flop are externally available. All four flip-flops are controlled by a common clock and a common CLEAR. Clearing is accomplished by a negative pulse at the CLEAR input. All four Q outputs are cleared to a logical "0" and all four \overline{Q} outputs to a logical "1."

The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide operating supply voltage range: 2-6V
- Low input current: 1 µA maximum
- Low quiescent supply current: 80 µA maximum (74HC)
- High output drive current: 4 mA minimum (74HC)

Ordering Code:

Order Number	Package Number	Package Description
MM74HC175M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC175SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC175MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC175N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP VCC 4Q 4Q 4Q 4Q 4Q 4D 3D 3Q 3Q CLOCK 16 15 14 13 12 11 10 9 CLEAR 1Q 1Q 1D 2D 2Q 2Q GND Top View

Truth Table

(Each Flip-Flop)								
ı	nputs		Out	puts				
Clear	Clock	D	Q	Q				
L	Х	Х	L	Н				
Н	1	Н	Н	L				
Н	1	L	L	Н				
Н	L	Х	Q_0	\overline{Q}_0				

- H = HIGH Level (steady state)
- L = LOW Level (steady state)
- X = Irrelevant
- Transition from LOW-to-HIGH level
- $\mathbf{Q}_0 = \text{The level of Q}$ before the indicated steady-state input conditions were established

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MM74HC175 Logic Diagram

Absolute Maximum Ratings(Note 1)

Power Dissipation (P_D)

(Note 2)

 (Note 3)
 600 mW

 S.O. Package only
 500 mW

Lead Temperature (T_L)

(Soldering 10 seconds) 260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V _{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T _A)	-40	+85	°C
Input Rise or Fall Times			
$(t_r, t_f) V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns
Note 1: Absolute Maximum Ratings are those	values	hevond wh	ich dam-

age to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: –
12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = -40 to 85°C	T _A = -55 to 125°C	Units	
			*CC	Тур	Guaranteed Limits			Units	
V _{IH}	Minimum HIGH Level		2.0V		1.5	1.5	1.5	V	
	Input Voltage		4.5V		3.15	3.15	3.15	V	
			6.0V		4.2	4.2	4.2	V	
V _{IL}	Maximum LOW Level		2.0V		0.5	0.5	0.5	V	
	Input Voltage		4.5V		1.35	1.35	1.35	V	
			6.0V		1.8	1.8	1.8	V	
V _{OH}	Minimum HIGH Level	$V_{IN} = V_{IH}$ or V_{IL}							
	Output Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	2.0	1.9	1.9	1.9	V	
			4.5V	4.5	4.4	4.4	4.4	V	
			6.0V	6.0	5.9	5.9	5.9	V	
		$V_{IN} = V_{IH}$ or V_{IL}							
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	4.2	3.98	3.84	3.7	V	
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	5.7	5.48	5.34	5.2	V	
V _{OL}	Maximum LOW Level	$V_{IN} = V_{IH}$ or V_{IL}							
	Output Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	0	0.1	0.1	0.1	V	
			4.5V	0	0.1	0.1	0.1	V	
			6.0V	0	0.1	0.1	0.1	V	
		$V_{IN} = V_{IH}$ or V_{IL}							
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	0.2	0.26	0.33	0.4	V	
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	0.2	0.26	0.33	0.4	V	
I _{IN}	Maximum Input	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μΑ	
	Current								
I _{CC}	Maximum Quiescent	$V_{IN} = V_{CC}$ or GND	6.0V		8	80	160	μА	
	Supply Current	$I_{OUT} = 0 \mu A$							

Note 4: For a power supply of 5V \pm 10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

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AC Electrical Characteristics

 $V_{CC} = 5V$, $T_A = 25^{\circ}C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

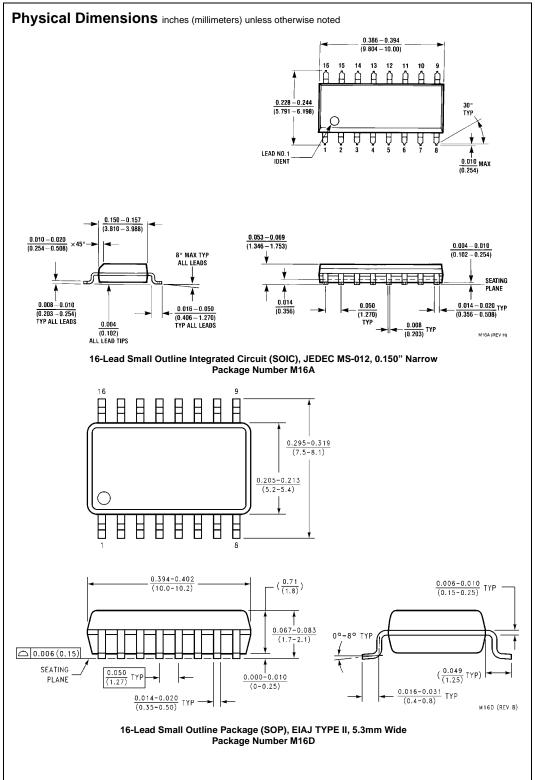
Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Units
f _{MAX}	Maximum Operating		60	35	MHz
	Frequency				
t _{PHL} , t _{PLH}	Maximum Propagation		15	25	ns
	Delay, Clock to Q or Q				
t _{PHL} , t _{PLH}	Maximum Propagation		13	21	ns
	Delay, Reset to Q or Q				
t _{REC}	Minimum Removal			20	ns
	Time, Clear to Clock				
t _S	Minimum Setup Time, Data to Clock			20	ns
t _H	Minimum Hold Time, Data from Clock			0	ns
t _W	Minimum Pulse Width, Clock or Clear		10	16	ns

AC Electrical Characteristics

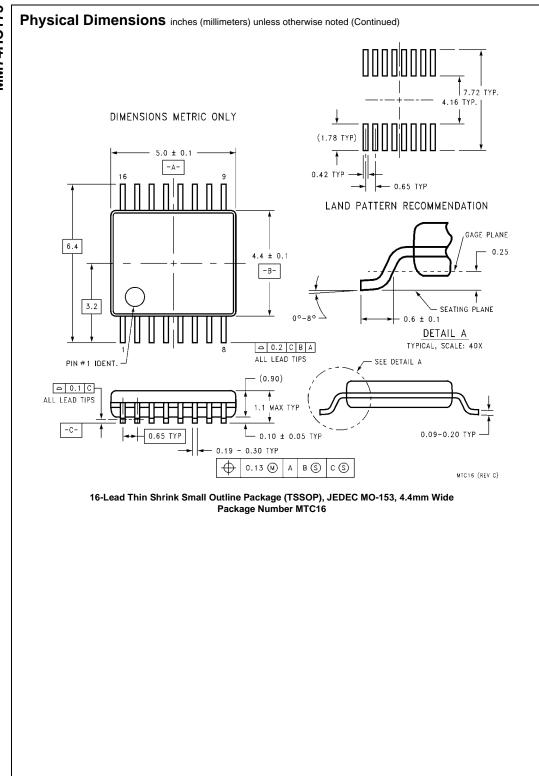
 $\rm V_{CC} = 2.0V$ to 6.0V, $\rm C_L = 50$ pF, $\rm t_f = t_f = 6$ ns (unless otherwise specified)

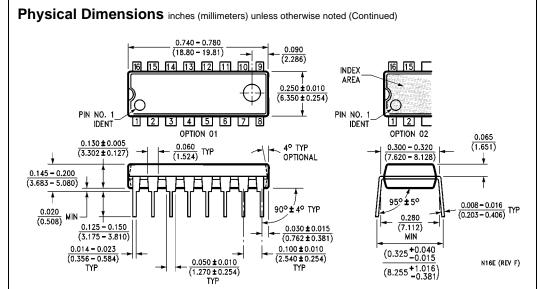
Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = -40 to 85°C	T _A = -55 to 125°C	Units
			• • • • • • • • • • • • • • • • • • • •	Тур	Typ Guaranteed Limits			Oiiita
f _{MAX}	Maximum Operating		2.0V	12	6	5	4	MHz
	Frequency		4.5V	60	30	24	20	MHz
			6.0V	70	35	28	24	MHz
t _{PHL} , t _{PLH}	Maximum Propagation		2.0V	80	150	190	225	ns
	Delay, Clock to Q or Q		4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t _{PHL} , t _{PLH}	Maximum Propagation		2.0V	64	125	158	186	ns
	Delay, Reset to Q or Q		4.5V	14	25	32	37	ns
			6.0V	12	21	27	32	ns
t _{REM}	Minimum Removal Time		2.0V		100	125	150	ns
	Clear to Clock		4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t _S	Minimum Setup Time		2.0V		100	125	150	ns
	Data to Clock		4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t _H	Minimum Hold Time		2.0V		0	0	0	ns
	Data from Clock		4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t _W	Minimum Pulse Width		2.0V	30	80	100	120	ns
	Clear or Clock		4.5V	9	16	20	24	ns
			6.0V	8	14	17	20	ns
t _r , t _f	Maximum Input Rise and		2.0V		1000	1000	1000	ns
	Fall Time		4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{TLH} , t_{THL}	Maximum		2.0V	30	75	95	110	ns
	Output Rise and		4.5V	9	15	19	22	ns
	Fall Time		6.0V	8	13	16	19	ns
C _{PD}	Power Dissipation Capacitance (Note 5)	(per package)		150				pF
C _{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} \ V_{CC}^2 + I_{CC} \ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \ V_{CC} \ f + I_{CC}$.



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16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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