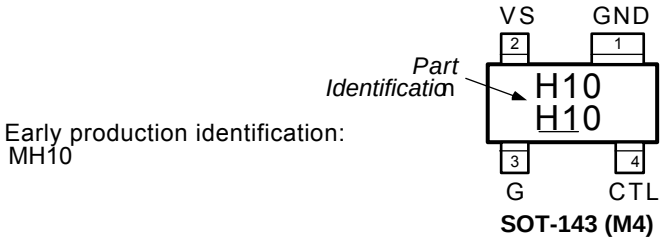
Ordering Information

Part Number		Making		Temp. Range	Package
Standard	**Pb-Free**	**Standard**	**Pb-Free**		
MIC5018BM4	MIC5018YM4	H10	H10	–40°C to +85°C	SOT-143

Pin Configuration



SOT-143 (M4)

Pin Description

Pin Number	Pin Name	Pin Function
1	GND	Ground: Power return.
2	VS	Supply (Input): +2.7V to +9V supply.
3	G	Gate (Output): Gate connection to external MOSFET.
4	CTL	Control (Input): TTL compatible on/off control input. Logic high drives the gate output above the supply voltage. Logic low forces the gate output near ground.

Absolute Maximum Ratings

Supply Input Voltage (V_{SUPPLY}) ..... +10V
Control Voltage (V_{CTL}) ..... –0.6V to +16V
Gate Voltage (V_G) ..... +16V
Ambient Temperature Range (T_A) ..... –40°C to +85°C

Operating Ratings

Lead Temperature, soldering 10 sec 300ºC
Package Thermal Resistance
SOT-143 (θ_{JA}) ..... 220°C/W
SOT-143 (θ_{JC}) ..... 130°C/W

Electrical Characteristics

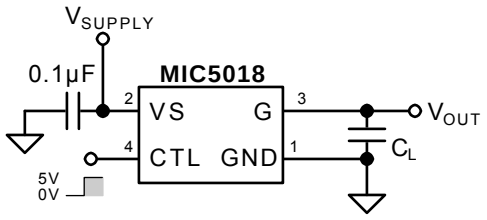
Parameter	Conditions[1]		Min	Typ	Max	Units
Supply Current	V_{SUPPLY} = 3.3V	V_{CTL} = 0V V_{CTL} = 3.3V		0.01 70	1 140	µA µA
	V_{SUPPLY} = 5V	V_{CTL} = 0V V_{CTL} = 5V		0 150	1 300	µA µA
Control Input Voltage	2.7V ≤ V_{SUPPLY} ≤ 9V	V_{CTL} for logic 0 input	0		0.8	V
	2.7V ≤ V_{SUPPLY} ≤ 5V	V_{CTL} for logic 1 input	2.0		V_{SUPPLY}	V
	5V ≤ V_{SUPPLY} ≤ 9V	V_{CTL} for logic 1 input	2.4		V_{SUPPLY}	V
Control Input Current	2.7V ≤ V_{SUPPLY} ≤ 9V			0.01	1	µA
Control Input Capacitance	[2]			5		pF
Zener Diode Output Clamp	V_{SUPPLY} = 9V		13	16	19	V
Gate Output Voltage	V_{SUPPLY} = 2.7V		6.3	7.1		V
	V_{SUPPLY} = 3.0V		7.1	8.2		V
	V_{SUPPLY} = 4.5V		11.4	13.4		V
Gate Output Current	V_{SUPPLY} = 5V	V_{OUT} = 10V[3]		9.5		µA
Gate Turn-On Time	V_{SUPPLY} = 4.5V	C_L = 1000pF[4] C_L = 3000pF[4]		0.75 2.1	1.5 4.2	Ms ms
Gate Turn-Off Time	V_{SUPPLY} = 4.5V	C_L = 1000pF[5] C_L = 3000pF[5]		10 30	20 60	µs µs

Notes:

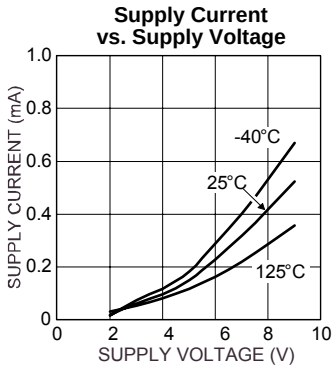
General Note: Devices are ESD protected, however handling precautions are recommended.

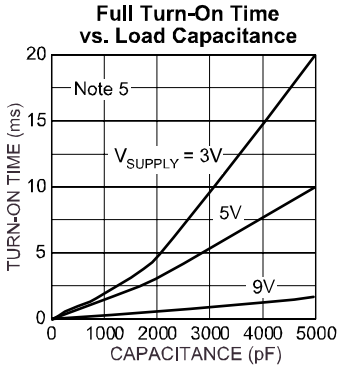
1. Typical values at T_A = 25°C. Minimum and maximum values indicate performance at –40°C ≥ T_A ≥ +85°C. Parts production tested at 25°C.
2. Guaranteed by design.
3. Resistive load selected for V_{OUT} = 10V.
4. Turn-on time is the time required for gate voltage to rise to 4V greater than the supply voltage. This represents a typical MOSFET gate threshold voltage.
5. Turn-off time is the time required for the gate voltage to fall to 4V above the supply voltage. This represents a typical MOSFET gate threshold voltage.

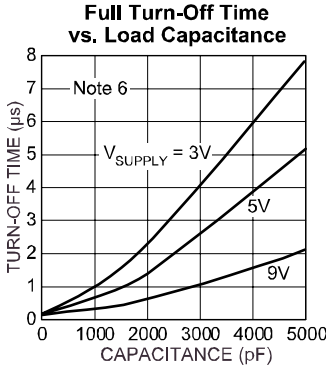
Test Circuit

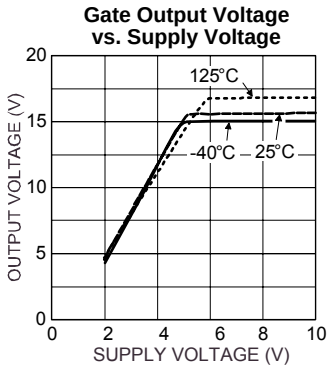


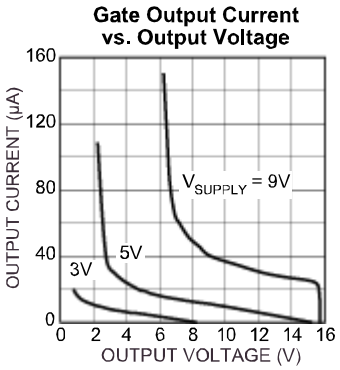
Typical Characteristics[4]

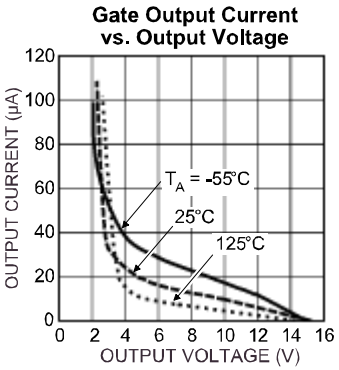










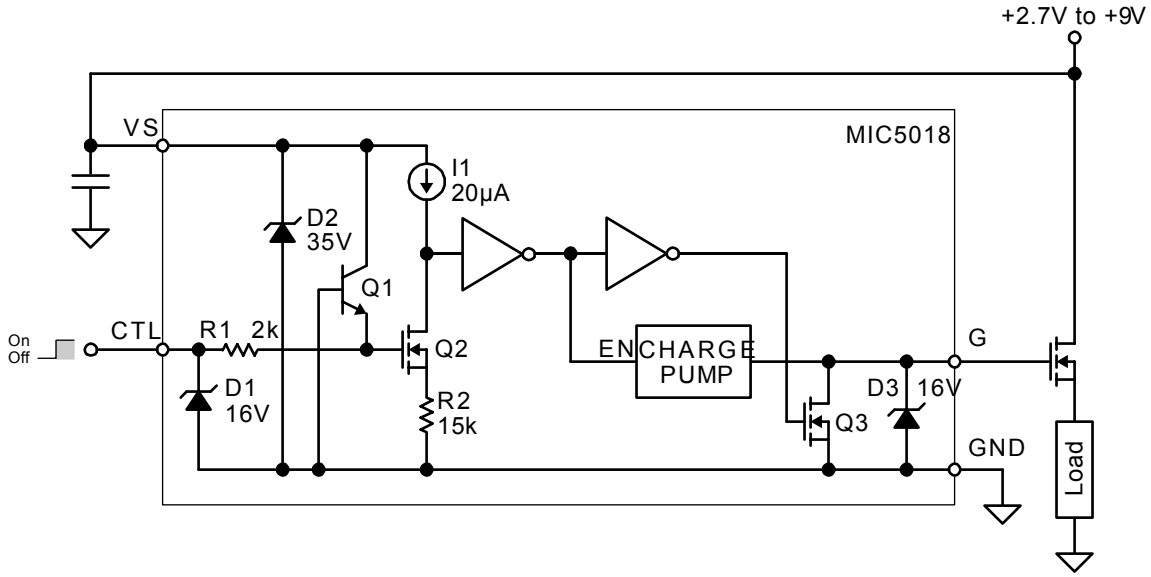


Note 4: T_A = 25°C, V_{SUPPLY} = 5V unless noted.

Note 5: Full turn-on time is the time between V_{CTL} rising to 2.5V and the V_G rising to 90% of its steady on-state value.

Note 6: Full turn-off time is the time between V_{CTL} falling to 0.5V and the V_G falling to 10% of its steady on-state value.

Functional Diagram



Functional Diagram with External Components
(High-Side Driver Configuration)

Functional Description

Refer to the functional diagram.

The MIC5018 is a noninverting device. Applying a logic high signal to CTL (control input) produces gate drive output. The G (gate) output is used to turn on an external N-channel MOSFET.

Supply

VS (supply) is rated for +2.7V to +9V. An external capacitor is recommended to decouple noise.

Control

CTL (control) is a TTL compatible input. CTL must be forced high or low by an external signal. A floating input may cause unpredictable operation.

A high input turns on Q2, which sinks the output of current source I1, making the input of the first inverter low. The inverter output becomes high enabling the charge pump.

Charge Pump

The charge pump is enabled when CTL is logic high. The charge pump consists of an oscillator and voltage quadrupler (4×). Output voltage is limited to 16V by a zener diode. The charge pump output voltage will be approximately:

$$V_G = 4 \times V_{SUPPLY} - 2.8V, \text{ but not exceeding } 16V$$

The oscillator operates from approximately 70kHz to approximately 100kHz depending upon the supply voltage and temperature.

Gate Output

The charge pump output is connected directly to the G (gate) output. The charge pump is active only when CTL is high. When CTL is low, Q3 is turned on by the second inverter and discharges the gate of the external MOSFET to force it off.

If CTL is high, and the voltage applied to VS drops to zero, the gate output will be floating (unpredictable).

ESD Protection

D1 and D2 clamp positive and negative ESD voltages. R1 isolates the gate of Q2 from sudden changes on the CTL input. Q1 turns on if the emitter (CTL input) is forced below ground to provide additional input protection. Zener D3 also clamps ESD voltages for the gate (G) output.

Application Information

Supply Bypass

A capacitor from VS to GND is recommended to control switching and supply transients. Load current and supply lead length are some of the factors that affect capacitor size requirements.

A 4.7µF or 10µF aluminum electrolytic or tantalum capacitor is suitable for many applications.

The low ESR (equivalent series resistance) of tantalum capacitors makes them especially effective, but also makes them susceptible to uncontrolled inrush current from low impedance voltage sources (such as NiCd batteries or automatic test equipment). Avoid instantaneously applying voltage, capable of high peak current, directly to or near tantalum capacitors without additional current limiting. Normal power supply turn-on (slow rise time) or printed circuit trace resistance is usually adequate for normal product usage.

MOSFET Selection

The MIC5018 is designed to drive N-channel enhancement type MOSFETs. The gate output (G) of the MIC5018 provides a voltage, referenced to ground, that is greater than the supply voltage. Refer to the "Typical Characteristics: Gate Output Voltage vs. Supply Voltage" graph.

The supply voltage and the MOSFET drain-to-source voltage drop determine the gate-to-source voltage.

$$V_{GS} = V_G - (V_{SUPPLY} - V_{DS})$$

where:

V_{GS} = gate-to-source voltage (enhancement)

V_G = gate voltage (from graph)

V_{SUPPLY} = supply voltage

V_{DS} = drain-to-source voltage
(approx. 0V at low current, or when fully enhanced)

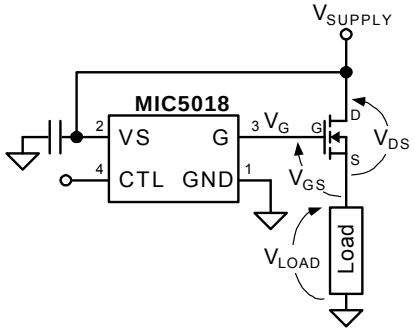


Figure 1. Voltages

The performance of the MOSFET is determined by the gate-to-source voltage. Choose the type of MOSFET according to the calculated gate-to-source voltage.

Standard MOSFET

Standard MOSFETs are fully enhanced with a gate-to-source voltage of about 10V. Their absolute maximum gate-to-source voltage is ±20V.

With a 5V supply, the MIC5018 produces a gate output of approximately 15V. Figure 2 shows how the remaining voltages conform. The actual drain-to-source voltage drop across an IRFZ24 is less than 0.1V with a 1A load and 10V enhancement. Higher current increases the drain-to-source voltage drop, increasing the gate-to-source voltage.

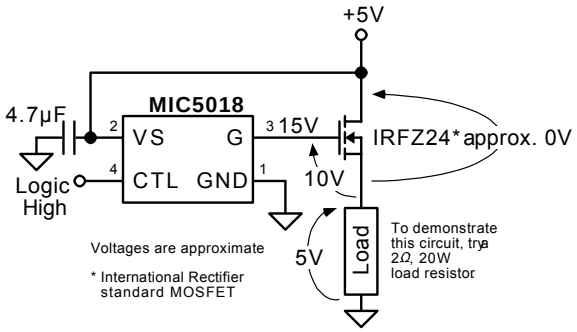


Figure 2. Using a Standard MOSFET

The MIC5018 has an internal zener diode that limits the gate-to-ground voltage to approximately 16V.

Lower supply voltages, such as 3.3V, produce lower gate output voltages which will not fully enhance standard MOSFETs. This significantly reduces the maximum current that can be switched. Always refer to the MOSFET data sheet to predict the MOSFET's performance in specific applications.

Logic-Level MOSFET

Logic-level N-channel MOSFETs are fully enhanced with a gate-to-source voltage of approximately 5V and generally have an absolute maximum gate-to-source voltage of ±10V.

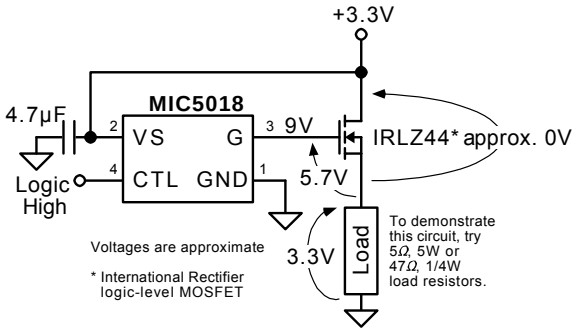


Figure 3. Using a Logic-Level MOSFET

Refer to Figure 3 for an example showing nominal voltages. The maximum gate-to-source voltage rating of a logic-level MOSFET can be exceeded if a higher

supply voltage is used. An external zener diode can clamp the gate-to-source voltage as shown in Figure 4. The zener voltage, plus its tolerance, must not exceed the absolute maximum gate voltage of the MOSFET.

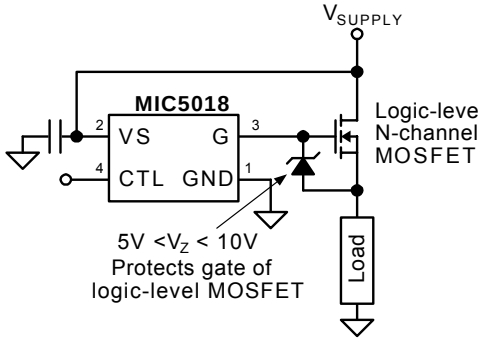


Figure 4. Gate-to-Source Protection

A gate-to-source zener may also be required when the maximum gate-to-source voltage could be exceeded due to normal part-to-part variation in gate output voltage. Other conditions can momentarily increase the gate-to-source voltage, such as turning on a capacitive load or shorting a load.

Inductive Loads

Inductive loads include relays, and solenoids. Long leads may also have enough inductance to cause adverse effects in some circuits.

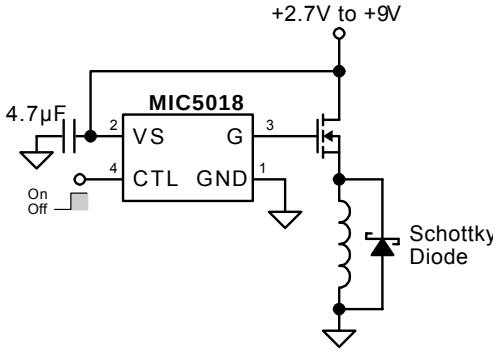


Figure 5. Switching an Inductive Load

Switching off an inductive load in a high-side application momentarily forces the MOSFET source negative (as the inductor opposes changes to current). This voltage spike can be very large and can exceed a MOSFET's gate-to-source and drain-to-source ratings. A Schottky diode across the inductive load provides a discharge current path to minimize the voltage spike. The peak current rating of the diode should be greater than the load current.

In a low-side application, switching off an inductive load will momentarily force the MOSFET drain higher than the supply voltage. The same precaution applies.

Split Power Supply

Refer to Figure 6. The MIC5018 can be used to control a 12V load by separating the driver supply from the load supply.

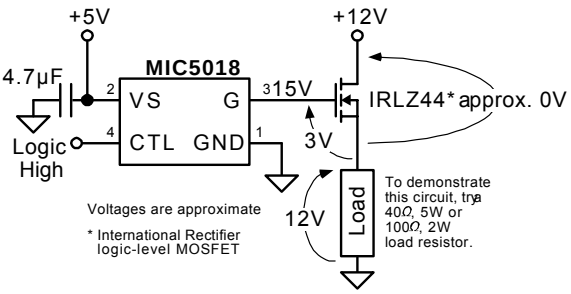


Figure 6. 12V High-Side Switch

A logic-level MOSFET is required. The MOSFET's maximum current is limited slightly because the gate is not fully enhanced. To predict the MOSFETs performance for any pair of supply voltages, calculate the gate-to-source voltage and refer to the MOSFET data sheet.

$$V_{GS} = V_G - (V_{LOAD\ SUPPLY} - V_{DS})$$

V_G is determined from the driver supply voltage using the "Typical Characteristics: Gate Output Voltage vs. Supply Voltage" graph.

Low-Side Switch Configuration

The low-side configuration makes it possible to switch a voltage much higher than the MIC5018's maximum supply voltage.

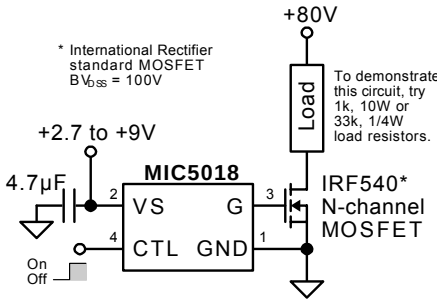
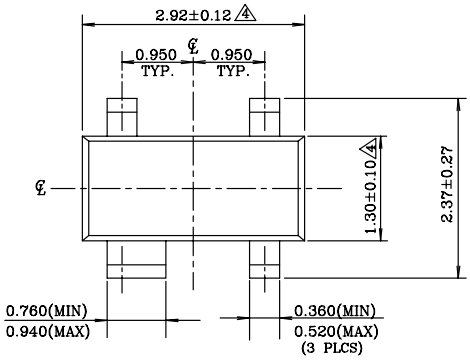


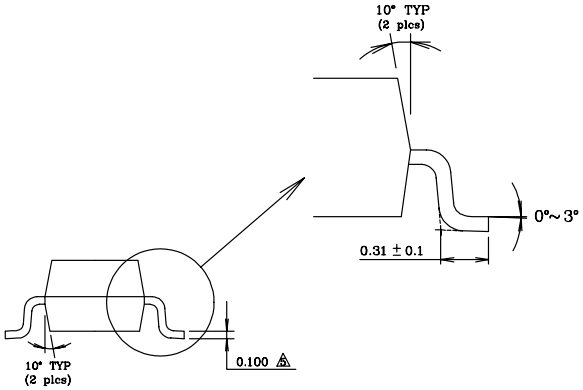
Figure 7. Low-Side Switch Configuration

The maximum switched voltage is limited only by the MOSFET's maximum drain-to-source ratings.

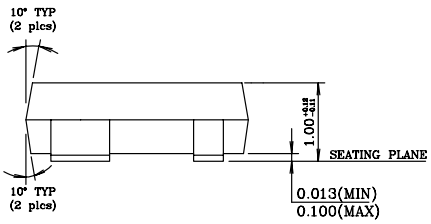
Package Information



TOP VIEW



END VIEW



SIDE VIEW

NOTE:

1. Dimensions and tolerances are as per ANSI Y14.5M, 1982.
2. Package surface to be mirror finish.
3. Die is facing up for mold & trim/form.
4. Dimension are exclusive of mold flash and gate burr.
5. Dimension are exclusive of solder plating.

SOT-143 (M4)

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