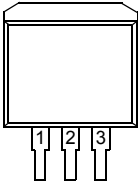


MCP1790/MCP1791

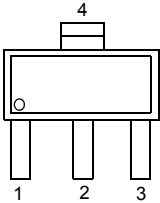
Package Types

MCP1790

DDPAK-3



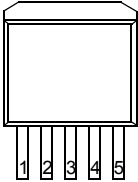
SOT-223-3



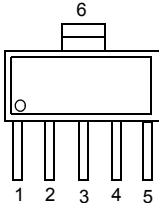
Pin	
1	V_{IN}
2	GND (TAB)
3	V_{OUT}
4	GND (TAB)

MCP1791

DDPAK-5

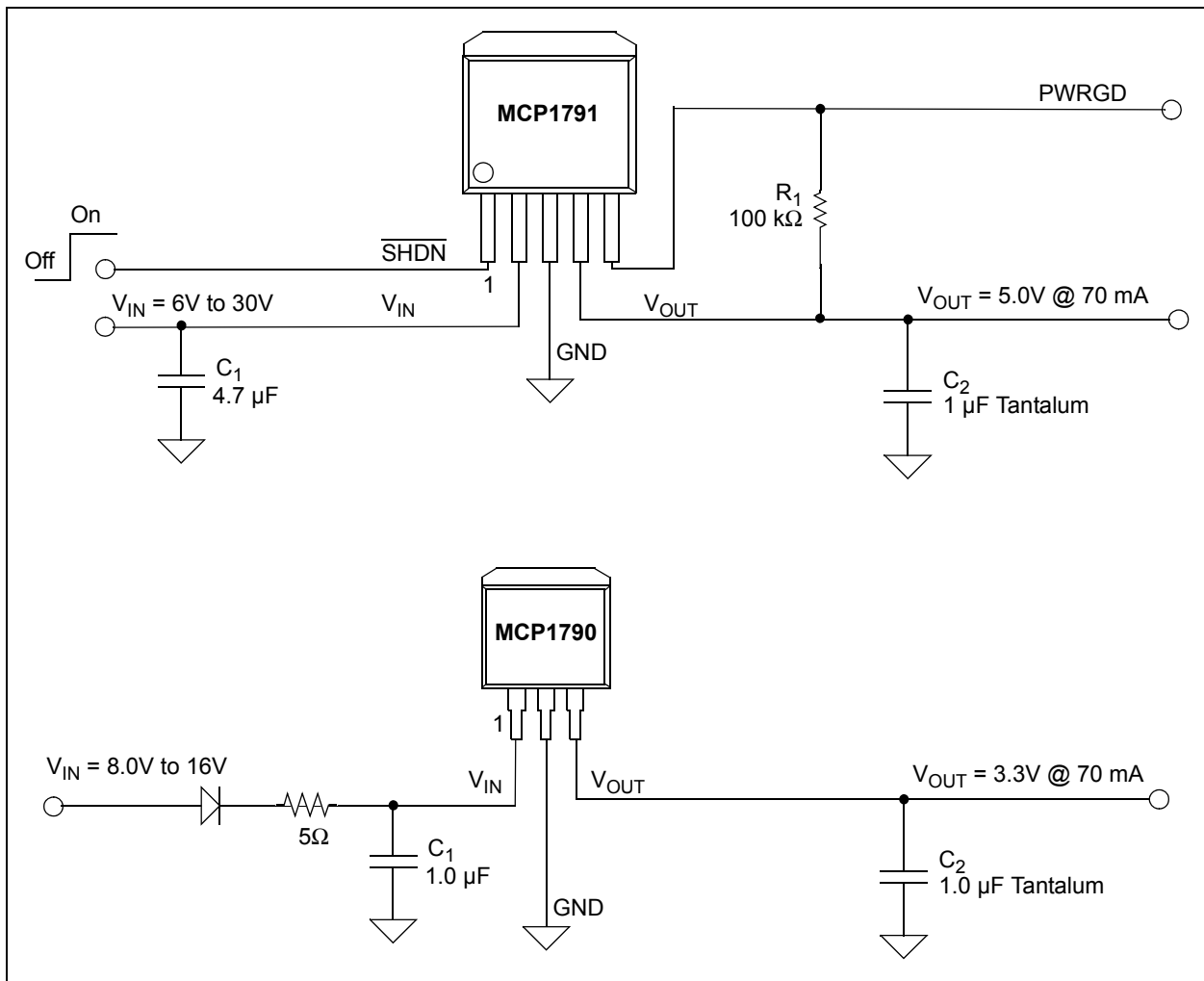


SOT-223-5



Pin	
1	SHDN
2	V_{IN}
3	GND (TAB)
4	V_{OUT}
5	PWRGD
6	GND (TAB)

TYPICAL APPLICATION



MCP1790/MCP1791

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage, V_{IN} +48.0V
 V_{IN} , PWRGD, SHDN (GND-0.3V) to (V_{IN} +0.3V)
 V_{OUT} (GND-0.3V) to (+5.5V)
Internal Power Dissipation Internally-Limited (**Note 4**)
Output Short Circuit Current Continuous
Storage temperature -55°C to +150°C
Maximum Junction Temperature 165°C (**Note 7**)
Operating Junction Temperature -40°C to +125°C
ESD protection on all pins ≥ 6 kV HBM and ≥ 400 V MM

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$, (Note 1), $I_{OUT} = 1$ mA, $C_{OUT} = 4.7$ μ F (X7R Ceramic), $C_{IN} = 4.7$ μ F (X7R Ceramic), $T_A = +25^\circ\text{C}$, SHDN > 2.4V. Boldface type applies for junction temperatures, T_J (Note 5) of -40°C to +125°C.						
Parameters	Symbol	Min	Typ	Max	Units	Conditions
Input Operating Voltage	V_{IN}	6.0	—	30.0	V	+48V _{DC} Load Dump Peak < 500 ms
Input Quiescent Current	I_q	—	70	130	μ A	$I_L = 0$ mA
Input Quiescent Current for SHDN Mode	I_{SHDN}	—	10	25	μ A	SHDN = GND
Ground Current	I_{GND}	—	110	210	μ A	$I_L = 70$ mA
Maximum Output Current	I_{OUT}	70	—	—	mA	
Line Regulation	$\frac{\Delta V_{OUT}}{(V_{OUT} \times \Delta V_{IN})}$	—	± 0.0002	± 0.05	%/V	6.0V < V_{IN} < 30V
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	-0.45	± 0.2	0.45	%	$I_{OUT} = 1$ mA to 70 mA (Note 3)
Output Peak Short Circuit Current	I_{OUT_SC}	—	$V_R/10$	—	A	$R_{LOAD} < 0.1\Omega$ Peak Current
Output Voltage Regulation	V_{OUT}	$V_R - 2.5\%$	V_R	$V_R + 2.5\%$	V	—
V_{OUT} Temperature Coefficient	TCV_{OUT}	—	65	—	ppm/°C	Note 9
Input Voltage to Turn On Output	V_{ON}	—	5.5	6.0	V	Rising V_{IN}

- Note 1:** The minimum V_{IN} , $V_{IN(MIN)}$ must meet two conditions: $V_{IN} \geq 6.0$ V and $V_{IN} \geq V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.
- 2:** V_R is the nominal regulator output voltage.
- 3:** Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.
- 4:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A , T_J , θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 165°C rating. Sustained junction temperatures above 165°C can impact the device reliability.
- 5:** The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the ambient temperature is not significant.
- 6:** Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_R + V_{DROPOUT(MAX)}$.
- 7:** Sustained junction temperatures above 165°C can impact the device reliability.
- 8:** The Short Circuit Recovery Time test is done by placing the device into a short circuit condition and then removing the short circuit condition before the device die temperature reaches 125 °C. If the device goes into thermal shutdown, then the Short Circuit Recovery Time will depend upon the thermal dissipation properties of the package and circuit board.
- 9:** $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) * 10^6 / (V_R * \Delta\text{Temperature})$, $V_{OUT-HIGH}$ = highest voltage measured over the temperature range. $V_{OUT-LOW}$ = lowest voltage measured over the temperature range.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$, (**Note 1**), $I_{OUT} = 1 \text{ mA}$, $C_{OUT} = 4.7 \mu\text{F}$ (X7R Ceramic), $C_{IN} = 4.7 \mu\text{F}$ (X7R Ceramic), $T_A = +25^\circ\text{C}$, $SHDN > 2.4\text{V}$. **Boldface** type applies for junction temperatures, T_J (**Note 5**) of -40°C to $+125^\circ\text{C}$.

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Short Circuit Foldback Voltage Corner	V _{FOLDBACK}	—	4.2	—	V	V _R = 5.0V Falling V _{OUT} , R _{LOAD} < 0.1Ω
		—	3.0	—	V	V _R = 3.3V Falling V _{OUT} , R _{LOAD} < 0.1Ω
		—	2.7	—	V	V _R = 3.0V Falling V _{OUT} , R _{LOAD} < 0.1Ω
Short Circuit Foldback Current		—	105	—	mA	V _{OUT} ~ 0V, R _{LOAD} < 0.1Ω V _R = 5.0V (Note 2)
		—	99	—	mA	V _R = 3.3V (Note 2)
		—	99	—	mA	V _R = 3.0V (Note 2)
Startup Voltage Overshoot	V _{OVER}	—	0.10	—	% V _{OUT}	V _{IN} = 0V to 6.0V
Dropout Voltage	V _{DROPOUT}	—	700	1300	mV	I _{OUT} = 70 mA, (Note 6)
Dropout Current I _{OUT} = 0 mA	I _{DO}	—	130	—	μA	V _R = 5.0V, V _{IN} = 4.500V
		—	75	—	μA	V _R = 3.3V, V _{IN} = 4.500V
		—	75	—	μA	V _R = 3.0V, V _{IN} = 4.500V
Shutdown Input						
Logic High Input	V _{SHDN-HIGH}	2.4	—	V _{IN(MAX)}	V	—
Logic Low Input	V _{SHDN-LOW}	0	—	0.8	V	—
Shutdown Input Leakage Current	SHDN _{ILK}	— —	0.100 3.0	0.500 5.0	μA	SHDN = GND SHDN = 6V
Power Good Characteristics						
PWRGD Input Voltage Operating Range	V _{PWRGD_VIN}	2.8	—	—	V	—
PWRGD Threshold Voltage (Referenced to V _{OUT})	V _{PWRGD_TH}	88	90	92	%V _{OUT}	Falling Edge of V _{OUT}
PWRGD Threshold Hysteresis	V _{PWRGD_HYS}	1.0	2.0	3.0	%V _{OUT}	Rising Edge of V _{OUT}
PWRGD Output Voltage LOW	V _{PWRGD_L}	—	0.2	0.4	V	I _{PWRGD SINK} = 5.0 mA, V _{OUT} = 0V
PWRGD Output Sink Current	I _{PWRGD_L}	5.0	—	—	mA	V _{PWRGD} <= 0.4V
PWRGD Leakage	I _{PWRGD_LK}	—	1.0	—	nA	V _{PWRGD} = V _{IN} = 6.0V
PWRGD Time Delay	T _{PG}	—	30	—	μs	Rising Edge

- Note 1:** The minimum V_{IN} , $V_{IN(MIN)}$ must meet two conditions: $V_{IN} \geq 6.0\text{V}$ and $V_{IN} \geq V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.
- 2:** V_R is the nominal regulator output voltage.
- 3:** Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.
- 4:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A , T_J , θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 165°C rating. Sustained junction temperatures above 165°C can impact the device reliability.
- 5:** The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the ambient temperature is not significant.
- 6:** Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_R + V_{DROPOUT(MAX)}$.
- 7:** Sustained junction temperatures above 165°C can impact the device reliability.
- 8:** The Short Circuit Recovery Time test is done by placing the device into a short circuit condition and then removing the short circuit condition before the device die temperature reaches 125°C . If the device goes into thermal shutdown, then the Short Circuit Recovery Time will depend upon the thermal dissipation properties of the package and circuit board.
- 9:** $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) * 10^6 / (V_R * \Delta\text{Temperature})$, $V_{OUT-HIGH}$ = highest voltage measured over the temperature range. $V_{OUT-LOW}$ = lowest voltage measured over the temperature range.

MCP1790/MCP1791

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$, (Note 1), $I_{OUT} = 1 \text{ mA}$, $C_{OUT} = 4.7 \mu\text{F}$ (X7R Ceramic), $C_{IN} = 4.7 \mu\text{F}$ (X7R Ceramic), $T_A = +25^\circ\text{C}$, $\text{SHDN} > 2.4\text{V}$. Boldface type applies for junction temperatures, T_J (Note 5) of -40°C to $+125^\circ\text{C}$.						
Parameters	Symbol	Min	Typ	Max	Units	Conditions
Detect Threshold to PWRGD Active Time Delay	$T_{V_{DET-PWRGD}}$	—	235	—	μs	$V_{OUT} = V_{PWRGD_TH} + 100 \text{ mV}$ to $V_{PWRGD_TH} - 100 \text{ mV}$
AC Performance						
Output Delay from SHDN	T_{OR}	—	200	—	μs	$\text{SHDN} = \text{GND}$ to V_{IN} , $V_{OUT} = \text{GND}$ to $95\% V_R$, $C_{OUT} = 1.0 \mu\text{F}$
PWRGD Delay from SHDN	T_{SHDN_PG}	—	400	—	ns	$\text{SHDN} = V_{IN}$ to GND , $C_{OUT} = 1.0 \mu\text{F}$
Output Noise	e_N	—	1.2	—	$(\mu\text{V}/\sqrt{\text{Hz}})$	$I_{OUT} = 50 \text{ mA}$, $f = 1 \text{ kHz}$
Power Supply Ripple Rejection Ratio	PSRR	—	90	—	dB	$V_{IN} = 7.0\text{V}$, $C_{IN} = 0 \mu\text{F}$, $I_{OUT} = 10 \text{ mA}$, $V_{INAC} = 400 \text{ mVpp}$, $f = 100 \text{ Hz}$
		—	75	—		$f = 1 \text{ kHz}$, $V_R = 5.0\text{V}$
		—	80	—		$f = 1 \text{ kHz}$, $V_R = < 5.0\text{V}$
		—	—	—		
Thermal Shutdown Temperature	T_{SD}	—	157	—	$^\circ\text{C}$	Rising Temperature
Thermal Shutdown Hysteresis	ΔT_{SD}	—	20	—	$^\circ\text{C}$	Falling Temperature
Short Circuit Recovery Time	t_{THERM}	—	0	—	ms	(Note 8)

- Note 1:** The minimum V_{IN} , $V_{IN(MIN)}$ must meet two conditions: $V_{IN} \geq 6.0\text{V}$ and $V_{IN} \geq V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.
- 2:** V_R is the nominal regulator output voltage.
- 3:** Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.
- 4:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A , T_J , θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 165°C rating. Sustained junction temperatures above 165°C can impact the device reliability.
- 5:** The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the ambient temperature is not significant.
- 6:** Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_R + V_{DROPOUT(MAX)}$.
- 7:** Sustained junction temperatures above 165°C can impact the device reliability.
- 8:** The Short Circuit Recovery Time test is done by placing the device into a short circuit condition and then removing the short circuit condition before the device die temperature reaches 125°C . If the device goes into thermal shutdown, then the Short Circuit Recovery Time will depend upon the thermal dissipation properties of the package and circuit board.
- 9:** $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) \cdot 10^6 / (V_R \cdot \Delta\text{Temperature})$, $V_{OUT-HIGH}$ = highest voltage measured over the temperature range. $V_{OUT-LOW}$ = lowest voltage measured over the temperature range.

TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_J	-40	—	+125	°C	—
Operating Temperature Range	T_J	-40	—	+125	°C	—
Storage Temperature Range	T_A	-55	—	+150	°C	—
Package Thermal Resistances						
Thermal Resistance, 3LD DPAK	θ_{JA} θ_{JC}	—	31.4 3	—	°C/W	EIA/JEDEC JESD51-751-7 4 Layer Board
Thermal Resistance, 3LD SOT-223	θ_{JA} θ_{JC}	—	62 15	—	°C/W	EIA/JEDEC JESD51-751-7 4 Layer Board
Thermal Resistance, 5LD DPAK	θ_{JA} θ_{JC}	—	31.4 3	—	°C/W	EIA/JEDEC JESD51-751-7 4 Layer Board
Thermal Resistance, 5LD SOT-223	θ_{JA} θ_{JC}	—	62 15	—	°C/W	EIA/JEDEC JESD51-751-7 4 Layer Board

MCP1790/MCP1791

2.0 TYPICAL PERFORMANCE CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $C_{OUT} = 4.7 \mu\text{F}$ Ceramic (X7R), $C_{IN} = 10.0 \mu\text{F}$ Ceramic (X7R), $I_{OUT} = 1 \text{ mA}$, Temperature = $+25^\circ\text{C}$, $V_{IN} = 6.0\text{V}$, $R_{PWRGD_PULLUP} = 10 \text{ k}\Omega$ To V_{OUT} , $\overline{V_{SHDN}} = V_{IN}$, and device is MCP1790.

Note: Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction Temperature over the Ambient temperature is not significant.

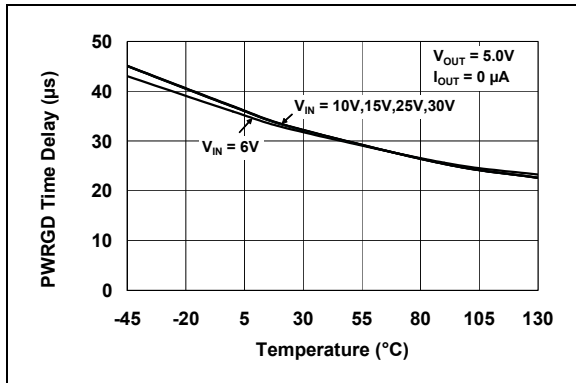


FIGURE 2-1: Power Good Time Delay vs. Temperature (MCP1791).

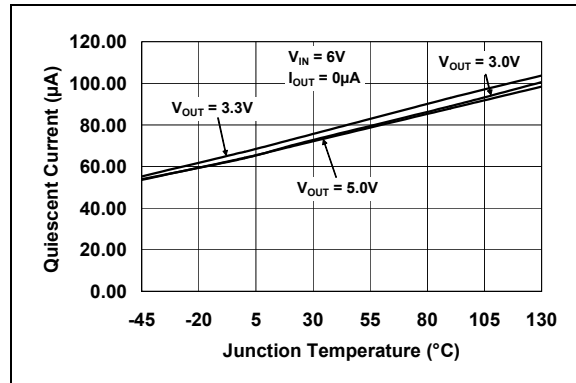


FIGURE 2-4: Quiescent Current vs. Junction Temperature.

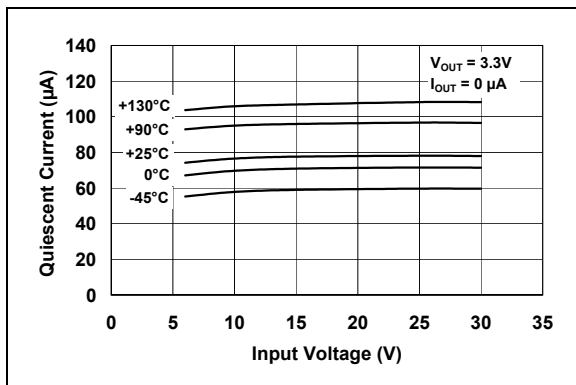


FIGURE 2-2: Quiescent Current vs. Input Voltage.

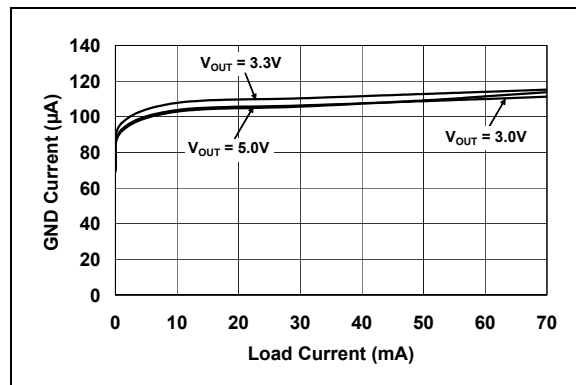


FIGURE 2-5: Ground Current vs. Load Current.

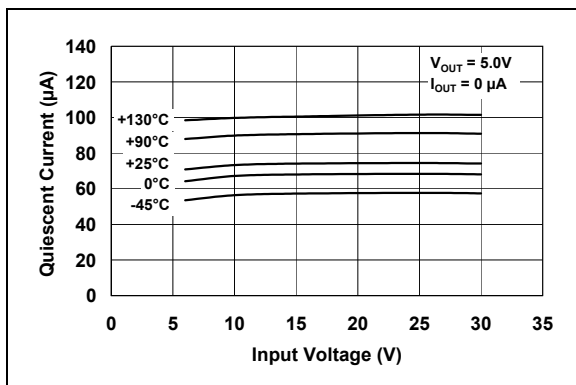


FIGURE 2-3: Quiescent Current vs. Input Voltage.

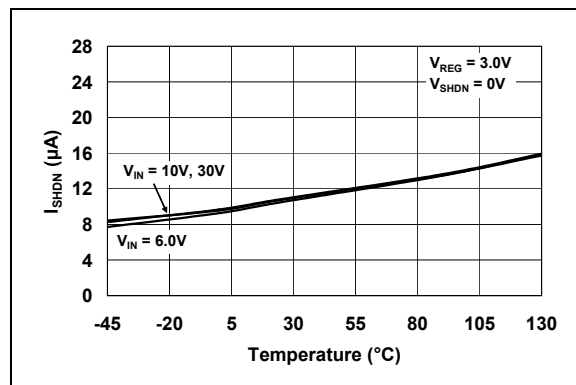


FIGURE 2-6: I_{SHDN} vs Temperature.

MCP1790/MCP1791

Note: Unless otherwise indicated, $C_{OUT} = 4.7 \mu\text{F}$ Ceramic (X7R), $C_{IN} = 10.0 \mu\text{F}$ Ceramic (X7R), $I_{OUT} = 1 \text{ mA}$, Temperature = $+25^\circ\text{C}$, $V_{IN} = 6.0\text{V}$, $R_{PWRGD_PULLUP} = 10 \text{ k}\Omega$ To V_{OUT} , $\overline{V}_{SHDN} = V_{IN}$, and device is MCP1790.

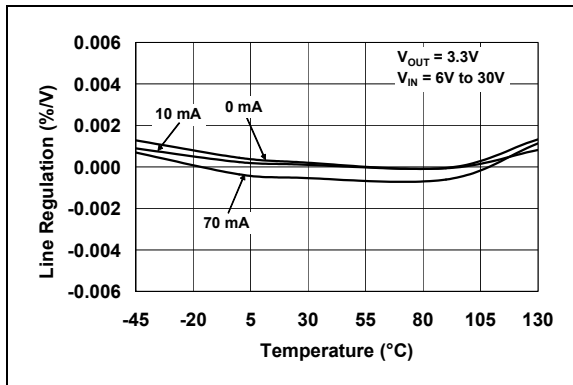


FIGURE 2-7: Line Regulation vs. Temperature.

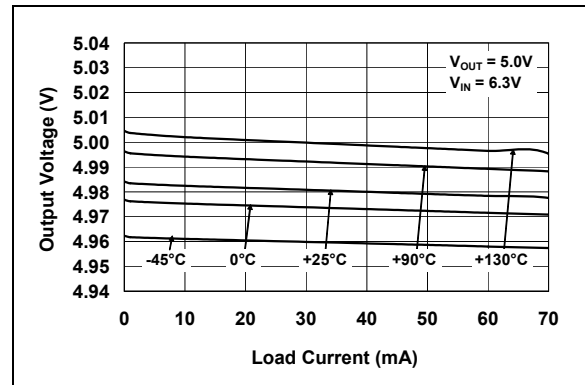


FIGURE 2-10: Output Voltage vs. Load Current.

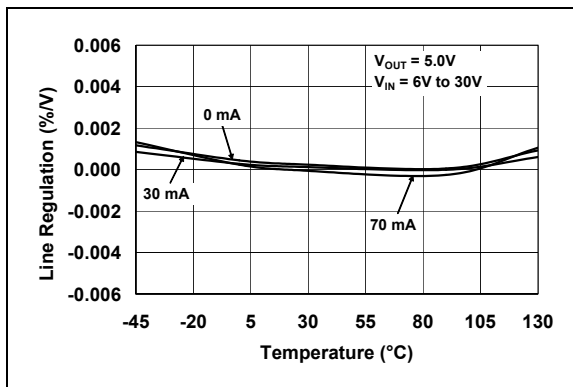


FIGURE 2-8: Line Regulation vs. Temperature.

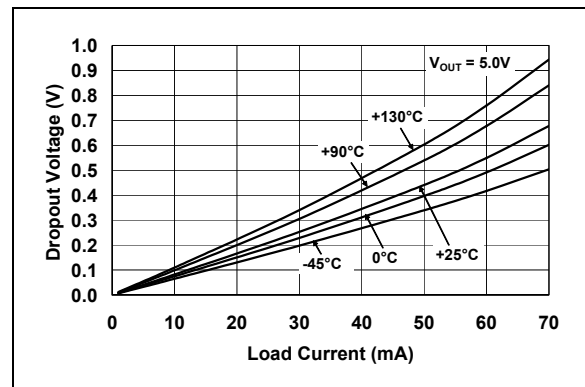


FIGURE 2-11: Dropout Voltage vs. Load Current.

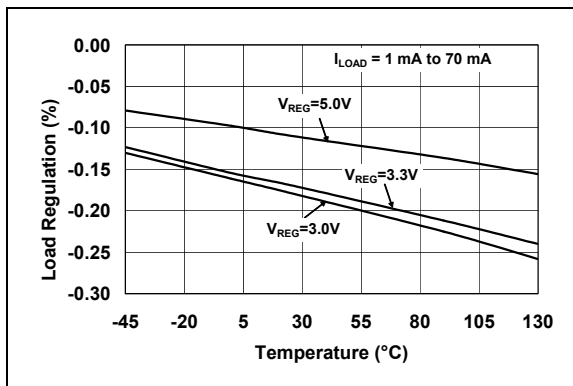


FIGURE 2-9: Load Regulation vs. Temperature.

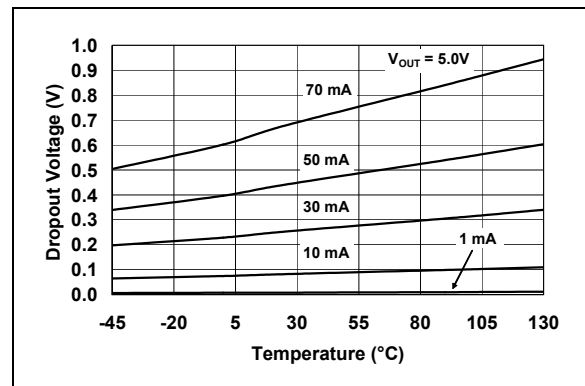


FIGURE 2-12: Dropout Voltage vs. Temperature.

MCP1790/MCP1791

Note: Unless otherwise indicated, $C_{OUT} = 4.7 \mu\text{F}$ Ceramic (X7R), $C_{IN} = 10.0 \mu\text{F}$ Ceramic (X7R), $I_{OUT} = 1 \text{ mA}$, Temperature = $+25^\circ\text{C}$, $V_{IN} = 6.0\text{V}$, $R_{PWRGD_PULLUP} = 10 \text{ k}\Omega$ To V_{OUT} , $\overline{V}_{SHDN} = V_{IN}$, and device is MCP1790.

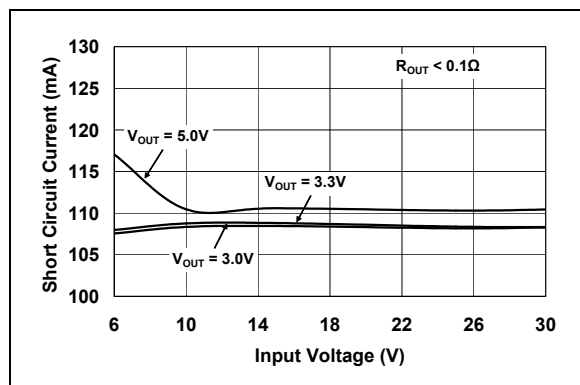


FIGURE 2-13: Short Circuit Current vs Input Voltage.

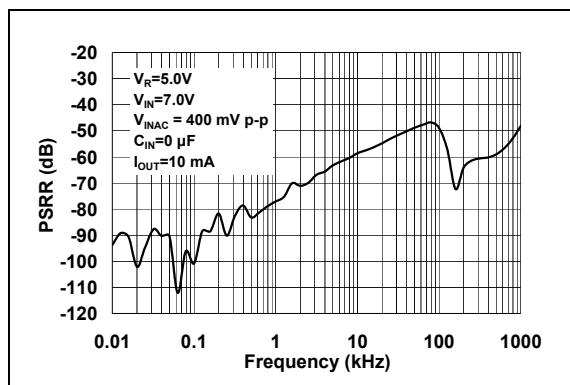


FIGURE 2-16: Power Supply Ripple Rejection vs. Frequency.

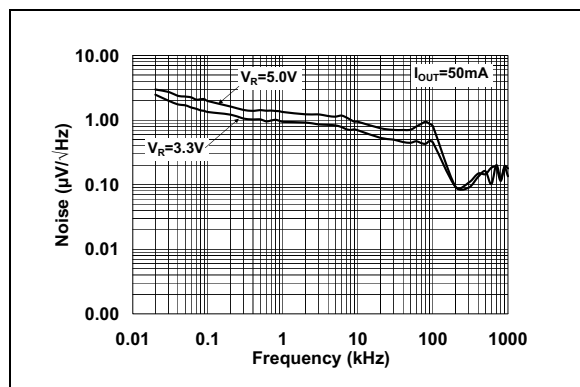


FIGURE 2-14: Output Noise Voltage Density vs. Frequency.

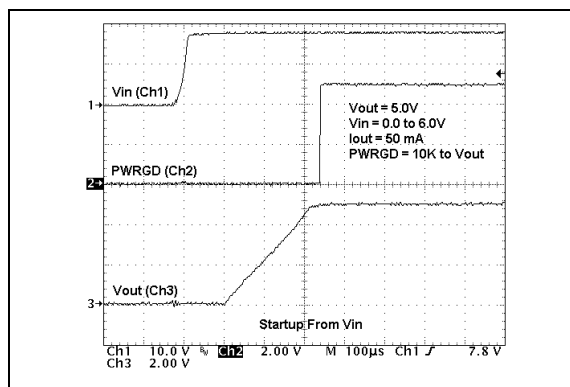


FIGURE 2-17: Startup from V_{IN} (MCP1791).

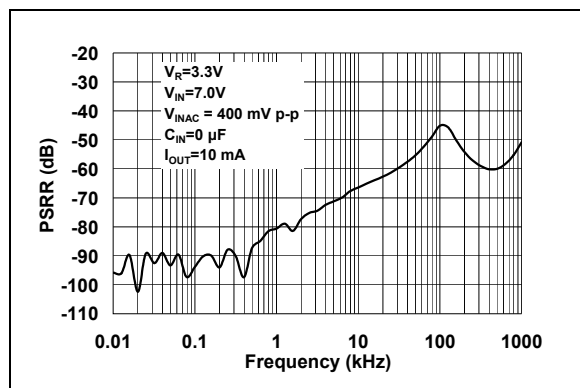


FIGURE 2-15: Power Supply Ripple Rejection vs. Frequency.

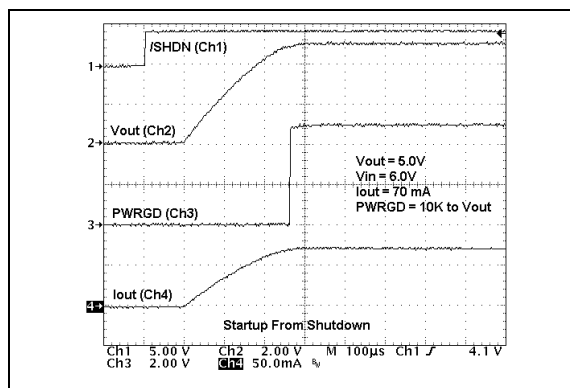


FIGURE 2-18: Startup from Shutdown (MCP1791).

MCP1790/MCP1791

Note: Unless otherwise indicated, $C_{OUT} = 4.7 \mu\text{F}$ Ceramic (X7R), $C_{IN} = 10.0 \mu\text{F}$ Ceramic (X7R), $I_{OUT} = 1 \text{ mA}$, Temperature = $+25^\circ\text{C}$, $V_{IN} = 6.0\text{V}$, $R_{PWRGD_PULLUP} = 10 \text{ k}\Omega$ To V_{OUT} , $\overline{V}_{SHDN} = V_{IN}$, and device is MCP1790.

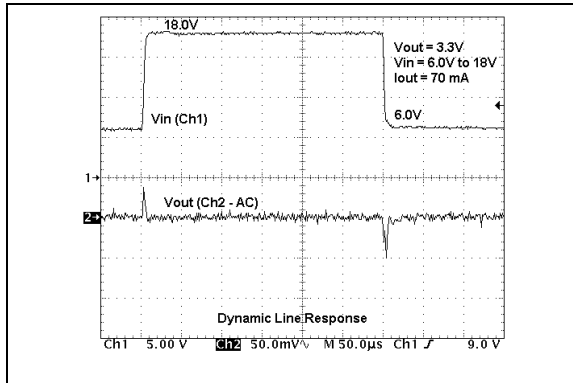


FIGURE 2-19: Dynamic Line Response.

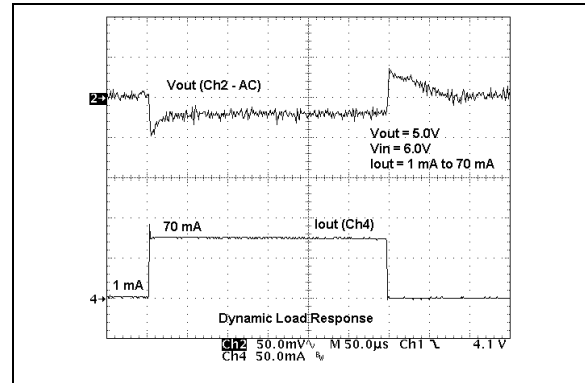


FIGURE 2-22: Dynamic Load Response.

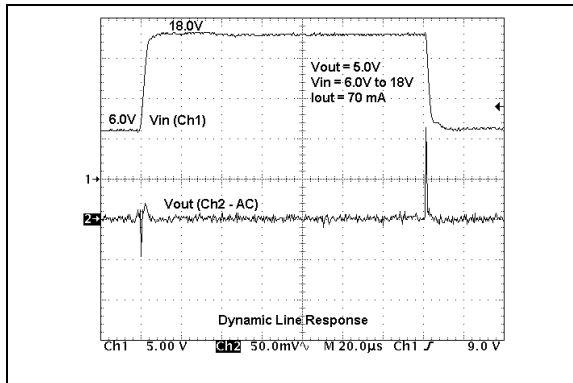


FIGURE 2-20: Dynamic Line Response.

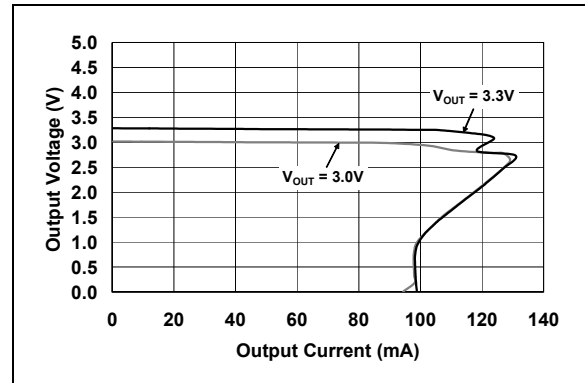


FIGURE 2-23: Short Circuit Response.

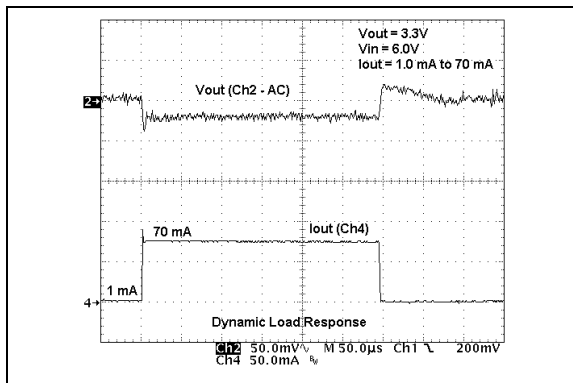


FIGURE 2-21: Dynamic Load Response.

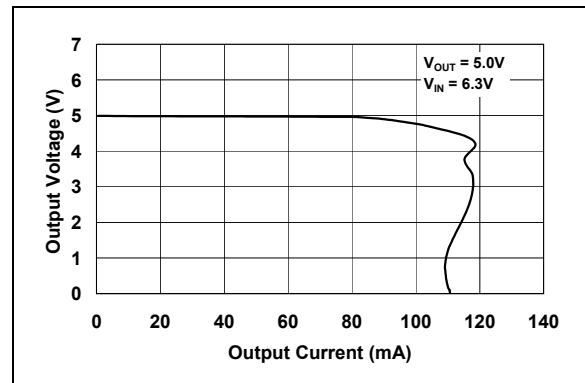


FIGURE 2-24: Short Circuit Response.

MCP1790/MCP1791

Note: Unless otherwise indicated, $C_{OUT} = 4.7 \mu\text{F}$ Ceramic (X7R), $C_{IN} = 10.0 \mu\text{F}$ Ceramic (X7R), $I_{OUT} = 1 \text{ mA}$, Temperature = $+25^\circ\text{C}$, $V_{IN} = 6.0\text{V}$, $R_{PWRGD_PULLUP} = 10 \text{ k}\Omega$ To V_{OUT} , $\overline{V}_{SHDN} = V_{IN}$, and device is MCP1790.

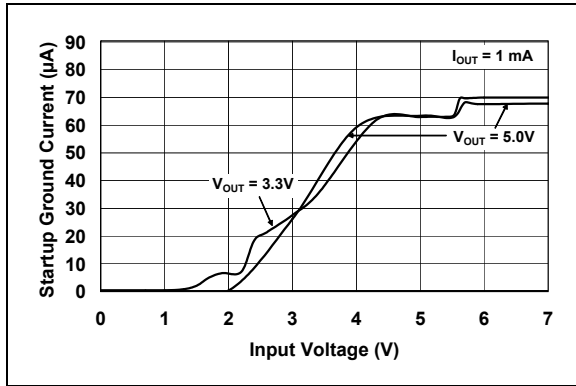


FIGURE 2-25: Startup Ground Current.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#) and [Table 3-2](#).

TABLE 3-1: MCP1790 PIN FUNCTION TABLE

Pin No. SOT-223-3	Pin No. DDPAK-3	Symbol	Function
1	1	V_{IN}	Unregulated Supply Voltage
2, Tab	2, Tab	GND	Ground Terminal
3	3	V_{OUT}	Regulated Output Voltage

TABLE 3-2: MCP1791 PIN FUNCTION TABLE

Pin No. SOT-223-5	Pin No. DDPAK-5	Symbol	Function
1	1	$\overline{\text{SHDN}}$	Shutdown Input
2	2	V_{IN}	Unregulated Supply Voltage
3	3	GND	Ground Terminal
4	4	V_{OUT}	Regulated Output Voltage
5	5	PWRGD	Power Good Open-Drain Output
Tab	Tab	—	Connected to Ground
—	—	N/C	No connection

3.1 Input Voltage Supply (V_{IN})

Connect the unregulated or regulated input voltage source to V_{IN} . If the input voltage source is located several inches away from the regulator or the input source is a battery, it is recommended that an input capacitor is used. A typical input capacitance value of 1 μF to 10 μF should be sufficient for most applications. The type of capacitor used can be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic will yield better noise and PSRR performance at high-frequency.

3.2 Ground (GND)

Tie GND to the negative side of the output and the negative side of the input capacitor. Only the regulator bias current flows out of this pin; there is no high current. The regulator output regulation is referenced to this pin. Minimize voltage drops between this pin and the negative side of the load.

3.3 Regulated Output Voltage (V_{OUT})

The V_{IN} pin is the regulated output voltage of the regulator. A minimum output capacitance of 1.0 μF tantalum, 1.0 μF electrolytic, or 4.7 μF ceramic is required for stability. The MCP1790 is stable with ceramic, tantalum, and electrolytic capacitors. See **Section 4.7 “Output Capacitor”** for output capacitor selection guidance.

3.4 Shutdown ($\overline{\text{SHDN}}$)

The $\overline{\text{SHDN}}$ pin is an active-low input signal that turns the regulator output voltage on and off. When the $\overline{\text{SHDN}}$ input is at a logic-high level, the regulator output voltage is enabled. When the $\overline{\text{SHDN}}$ input is pulled to a logic-low level, the regulator output voltage is disabled. When the $\overline{\text{SHDN}}$ input is pulled low, the PWRGD output signal also goes low and the regulator enters a low quiescent current shutdown state where the typical quiescent current is 10 μA . The $\overline{\text{SHDN}}$ pin is bonded to V_{IN} in the 3-pin versions of the regulator. See [Table 4-1](#).

3.5 Power Good Output (PWRGD)

The PWRGD pin is an open-drain output signal that is used to indicate when the regulator output voltage is within 90% (typically) of its nominal regulation value. The PWRGD threshold has a typical hysteresis value of 2%. The typical PWRGD delay time due to V_{OUT} rising above 90% +3% (maximum hysteresis) is 30 μs . The typical PWRGD delay time due to V_{OUT} falling below 90% is 235 μs . These delay times are internally fixed.

3.6 Exposed Pad (EP)

The DDPAK package has an exposed tab on the package. A heat sink may be mounted to the tab to aid in the removal of heat from the package during operation.

The exposed tab or pad of all of the available packages is at the ground potential of the regulator.

4.5 Shutdown ($\overline{\text{SHDN}}$)

The MCP1791 has a Shutdown ($\overline{\text{SHDN}}$) input signal that enables or disables the regulator output voltage. When the $\overline{\text{SHDN}}$ input signal is greater than 2.40V, the regulator output voltage is enabled. Note that the regulator output may still be disabled by the undervoltage lockout incorporated within the V_{IN} circuitry.

The value of the $\overline{\text{SHDN}}$ signal to put the regulator into Shutdown mode is $\leq 0.8\text{V}$. The SHDN pin is pulled low by an internal resistor. If the SHDN pin is left floating, the internal pull-down resistor will put the regulator into shutdown mode.

When the $\overline{\text{SHDN}}$ input signal is pulled to a logic-low, the PWRGD output signal will also go low and the regulator will enter a low quiescent current state where the typical quiescent current is 10 μA . There is a short time delay (approximately 400 ns) when the $\overline{\text{SHDN}}$ input signal transitions from high-to-low to prevent signal noise from disabling the regulator. The SHDN pin will ignore low-going pulses that are up to 400 ns in pulse width. If the SHDN input is pulled low for more than 400 ns, the regulator will enter Shutdown mode. This small bit of filtering helps to reject any system noise spikes on the $\overline{\text{SHDN}}$ input signal.

On the rising edge of the $\overline{\text{SHDN}}$ input, the shutdown circuitry will have a 100 μs delay before allowing the regulator output to turn on. This delay helps to reject any false turn-on signals or noise on the $\overline{\text{SHDN}}$ input signal. After the 100 μs delay, the regulator will start charging the output capacitor as the regulator output voltage rises from 0V to its final regulated value. The charging current will be limited by the short circuit current value of the device. If the $\overline{\text{SHDN}}$ input signal is pulled low during the 100 μs delay period, the timer will be reset and the delay time will start over again on the next rising edge of the $\overline{\text{SHDN}}$ input. The total time from the SHDN input going high (turn-on) to the regulator output being in regulation shall typically be 200 μs (100 μs + 100 μs) for a $C_{\text{LOAD}} = 1.0 \mu\text{F}$.

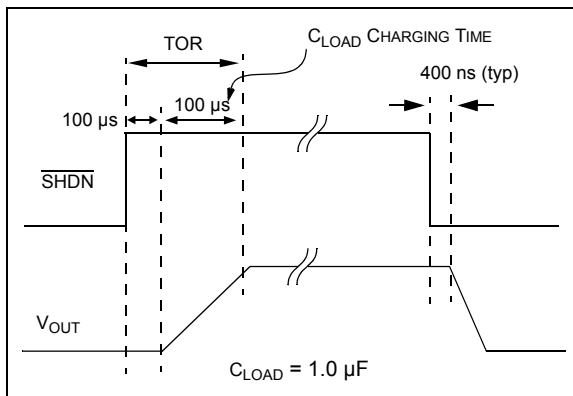


FIGURE 4-2: Shutdown Input Timing Diagram.

4.6 Low Voltage Shutdown

The MCP1790/MCP1791 incorporates a Low Voltage Shutdown circuit that turns off the output of the regulator whenever the input voltage, V_{IN} , is below the specified turn off voltage, V_{OFF} . When the input voltage (V_{B}) drops below the differential needed to provide stable regulation, the output voltage (V_{REG}) shall track the input down to approximately +4.00V. The regulator will turn off the output at this point.

The output will turn on when V_{IN} rises above the V_{ON} value specified in the data sheet. This feature is independent of the Shutdown input signal ($\overline{\text{SHDN}}$) that is provided for external regulator control. If the SHDN input signal is active (LOW), then the output of the regulator shall be disabled regardless of input voltage.

TABLE 4-1: SHUTDOWN LOGIC

V_{IN}	$\overline{\text{SHDN}}$	V_{OUT}
$< V_{\text{OFF}}$	L	OFF
$< V_{\text{OFF}}$	H	OFF
$> V_{\text{ON}}$	L	OFF
$> V_{\text{ON}}$	H	ON

4.7 Output Capacitor

The MCP1790/MCP1791 requires a minimum output capacitance of 1 μF tantalum or electrolytic capacitance. The minimum value for ceramic capacitors is 4.7 μF . The regulator is stable for all three types of capacitors from 4.7 μF to 1000 μF (see Figure 4-3). The MCP1790/MCP1791 regulator may be used with a 1 μF ceramic output capacitor if a 0.300 Ω resistor is placed in series with the capacitor. The low ESR and corresponding pole of the ceramic capacitor causes the instability below 4.7 μF .

The Equivalent Series Resistance (ESR) of the output capacitor must be no greater than 3 ohms. The output capacitor should be located as close to the regulator output as is practical. Ceramic materials X7R and X5R have low temperature coefficients and are recommended because of their size, cost and environmental robustness qualities.

MCP1790/MCP1791

4.8 Output Current and Current Limiting

The MCP1790/MCP1791 devices are tested and ensured to supply a minimum of 70 mA of output current.

The MCP1790/MCP1791 also incorporate an output current limit foldback. When the regulator is in an overcurrent condition, V_{OUT} will decrease with increasing load. When V_{OUT} falls below 30% (typical) of V_R , the output current will start to fold back. The output current will fold back to less than 100 mA (typical) when V_{OUT} is near 0 volts.

The 5.0V regulator has an overload current limiting of approximately 120 mA. If V_{REG} is lower than 3.5V, I_{OUT} will start to fold back and decrease along with V_{REG} until I_{OUT} is less than 105 mA and V_{REG} is near 0 volts.

The 3.3V regulator has an overload current limiting of approximately 130 mA. If V_{REG} is lower than 2.5V, I_{OUT} will start to fold back and decrease along with V_{REG} until I_{OUT} is less than 99 mA and V_{REG} is near 0 volts.

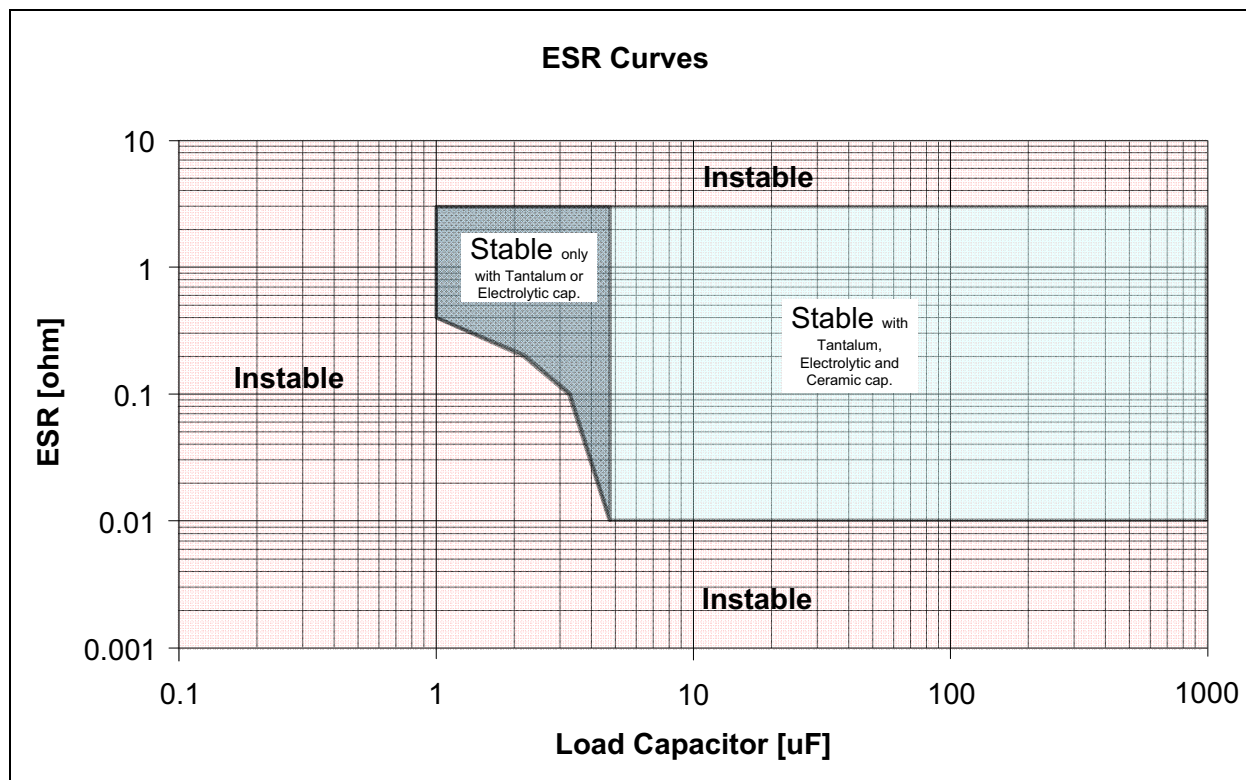


FIGURE 4-3: ESR Curves for Load Capacitor Selection.

4.9 Power Good Output (PWRGD)

The MCP1791 has an open-drain Power Good (PWRGD) output signal capable of sinking a minimum of 5.0 mA of current while maintaining a PWRGD output voltage of 0.4V or less.

As the output voltage of the LDO rises, the PWRGD output will be held low until the output voltage has exceeded the power good threshold (V_{PWRGD_TH}) level by an amount equal to the power good hysteresis value (V_{PWRGD_HYS}), typically 2% of V_R . Once this threshold has been exceeded, the power good output signal will be pulled high by an external pull-up resistor, indicating that the output voltage is stable and within regulation limits.

If the output voltage of the LDO falls below the power good threshold (V_{PWRGD_TH}) level, the power good output will transition low. The power good circuitry has a 235 μs delay when detecting a falling output voltage, which helps to increase noise immunity of the power good output and avoid false triggering of the power good output during fast output transients. See Figure 4-4 for power good timing characteristics.

When the LDO is put into Shutdown mode using the SHDN input, the power good output is pulled low within 400 ns typical, indicating that the output voltage will be out of regulation. The timing diagram for the power good output when using the shutdown input is shown in Figure 4-5.

The PWRGD output may be pulled up to either V_{IN} or V_{OUT} . When pulled to V_{OUT} , the PWRGD output will sink very little current during shutdown. When PWRGD is pulled up to V_{IN} , the PWRGD output will sink current during shutdown. That is because V_{OUT} is 0 during shutdown while V_{IN} is still active. When the PWRGD output is pulled to V_{IN} , the PWRGD output signal will track V_{IN} at startup until the threshold of the PWRGD circuitry has been reached and the PWRGD circuitry pulls the signal back low. Therefore, when pulling PWRGD to V_{IN} instead of V_{OUT} , the designer must be aware of the PWRGD signal going high while the input voltage is rising at startup. Pulling PWRGD to V_{OUT} removes the startup pulse.

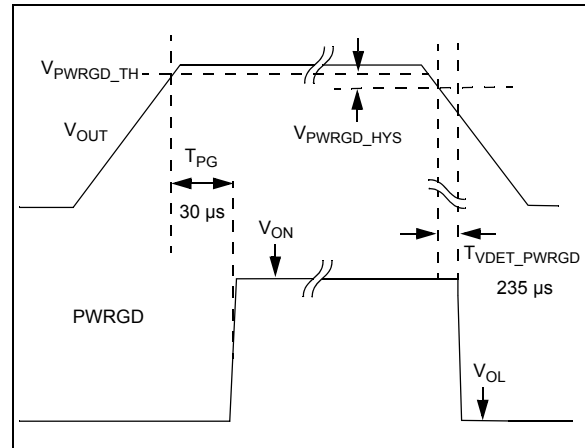


FIGURE 4-4: Power Good Timing.

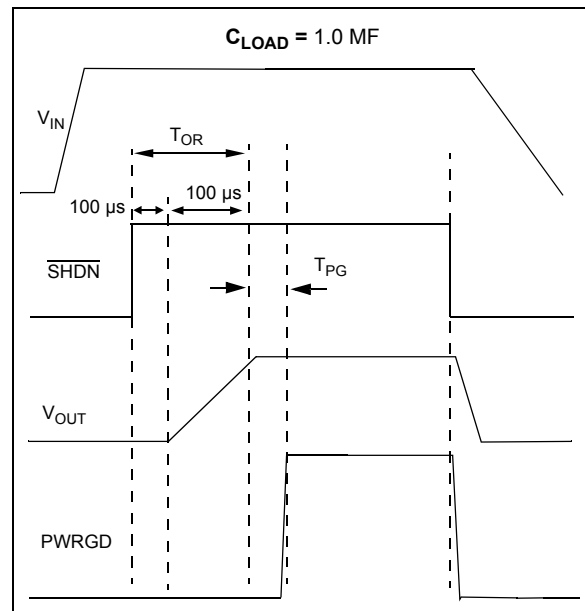


FIGURE 4-5: Power Good Timing from Shutdown.

MCP1790/MCP1791

5.0 APPLICATION CIRCUITS/ISSUES

5.1 Typical Application

The MCP1790/MCP1791 is most commonly used as a voltage regulator. It is a high voltage input capability and thermal protection make it ideal for automotive and 24V industrial applications.

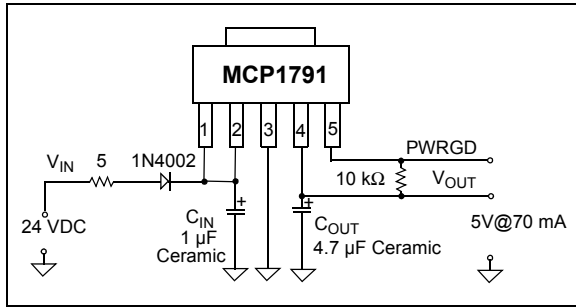


FIGURE 5-1: Typical Application.

5.1.1 APPLICATION INPUT CONDITIONS

Package Type = SOT-223-5
 Input Voltage Range = 8V to 24V
 V_{IN} maximum = 24V
 V_{OUT} typical = 5.0V
 I_{OUT} = 70 mA maximum

5.2 Power Calculations

5.2.1 POWER DISSIPATION

The internal power dissipation of the MCP1790/MCP1791 is a function of input voltage, output voltage and output current. The power dissipation, as a result of the quiescent current draw, is so low, it is insignificant ($70.0 \mu A \times V_{IN}$). The following equation can be used to calculate the internal power dissipation of the LDO.

EQUATION 5-1:

$$P_{LDO} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$$

P_{LDO} = LDO Pass device internal power dissipation
 $V_{IN(MAX)}$ = Maximum input voltage
 $V_{OUT(MIN)}$ = LDO minimum output voltage

The maximum continuous operating junction temperature specified for the MCP1790/MCP1791 is +125°C. To estimate the internal junction temperature of the MCP1790/MCP1791, the total internal power dissipation is multiplied by the thermal resistance from junction to ambient ($R\theta_{JA}$). The thermal resistance from junction to ambient for the SOT-223-5 package is estimated at 62°C/W.

EQUATION 5-2:

$$T_{J(MAX)} = P_{TOTAL} \times R\theta_{JA} + T_{AMAX}$$

$T_{J(MAX)}$ = Maximum continuous junction temperature
 P_{TOTAL} = Total device power dissipation
 $R\theta_{JA}$ = Thermal resistance from junction to ambient
 T_{AMAX} = Maximum ambient temperature

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. The following equation can be used to determine the package maximum internal power dissipation.

EQUATION 5-3:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{R\theta_{JA}}$$

$P_{D(MAX)}$ = Maximum device power dissipation
 $T_{J(MAX)}$ = Maximum continuous junction temperature
 $T_{A(MAX)}$ = Maximum ambient temperature
 $R\theta_{JA}$ = Thermal resistance from junction to ambient

EQUATION 5-4:

$$T_{J(RISE)} = P_{TOTAL} \times R\theta_{JA}$$

$T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature
 P_{TOTAL} = Total device power dissipation
 $R\theta_{JA}$ = Thermal resistance from junction-to-ambient

EQUATION 5-5:

$$T_J = T_{J(RISE)} + T_A$$

T_J = Junction Temperature
 $T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature
 T_A = Ambient temperature

5.3 Power Dissipation Example

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation, as a result of ground current, is small enough to be neglected.

5.3.1 POWER DISSIPATION EXAMPLE

Package:

Package Type = SOT-223-5

Input Voltage:

$V_{IN} = 8V \text{ to } 24V$

LDO Output Voltages and Currents:

$V_{OUT} = 5.0V$

$I_{OUT} = 50 \text{ mA}$

Maximum Ambient Temperature:

$T_{A(MAX)} = +40^{\circ}C$

Internal Power Dissipation:

Internal Power dissipation is the product of the LDO output current times the voltage across the LDO (V_{IN} to V_{OUT}).

$$P_{LDO(MAX)} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$$

$$P_{LDO} = (24V - (0.98 \times 5.0V)) \times 50 \text{ mA}$$

$$P_{LDO} = 955 \text{ milli-Watts}$$

5.3.1.1 Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction to ambient for the application. The thermal resistance from junction to ambient ($R_{\theta JA}$) is derived from an EIA/JEDEC standard for measuring thermal resistance for small surface mount packages. The EIA/JEDEC specification is JESD51-7, "High Effective Thermal Conductivity Test Board for Leadless Surface Mount Packages". The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors, such as copper area and thickness. Refer to AN792, "A Method to Determine How Much Power a SOT23 Can Dissipate in an Application", (DS00792), for more information regarding this subject.

$$T_{J(RISE)} = P_{TOTAL} \times R_{\theta JA}$$

$$T_{JRISE} = 955 \text{ milli-Watts} \times 62^{\circ}C/Watt$$

$$T_{JRISE} = 59.2^{\circ}C$$

5.3.1.2 Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below.

$$T_J = T_{JRISE} + T_{A(MAX)}$$

$$T_J = 99.2^{\circ}C$$

5.3.1.3 Maximum Package Power Dissipation at +40°C Ambient Temperature

SOT-223-5 ($62^{\circ}C/Watt = R_{\theta JA}$)

$$P_{D(MAX)} = (125^{\circ}C - 40^{\circ}C) / 62^{\circ}C/W$$

$$P_{D(MAX)} = 1.371 \text{ Watts}$$

DDPAK-5 ($32^{\circ}C/Watt = R_{\theta JA}$)

$$P_{D(MAX)} = (125^{\circ}C - 40^{\circ}C) / 32^{\circ}C/W$$

$$P_{D(MAX)} = 2.656 \text{ Watts}$$

5.4 Pulsed Load Applications

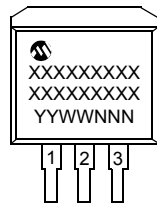
For some applications, there are pulsed load current events that may exceed the specified 70 mA maximum specification of the MCP1790/MCP1791. The internal current foldback feature of the MCP1790/MCP1791 will prevent high peak load demands from causing non-recoverable damage. The Current Foldback feature of the device will limit the output voltage and output current during pulsed applications. As the current rises above the foldback current threshold, the output voltage will decrease.

MCP1790/MCP1791

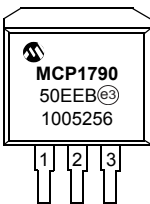
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

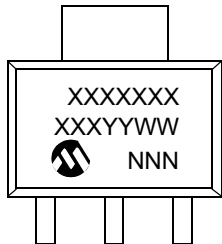
3-Lead DDPAK (MCP1790)



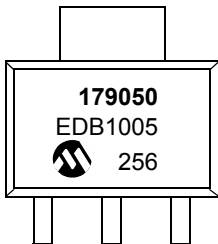
Example:



3-Lead SOT-223 (MCP1790)



Example:

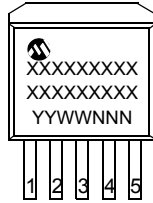


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

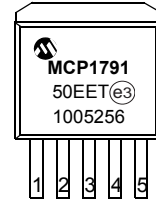
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

6.1 Package Marking Information (Continued)

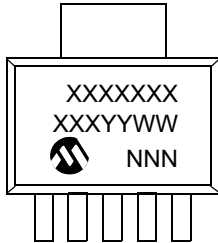
5-Lead DDPAK (Fixed) (MCP1791)



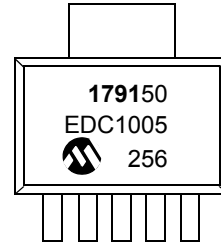
Example:



5-Lead SOT-223 (MCP1791)



Example:



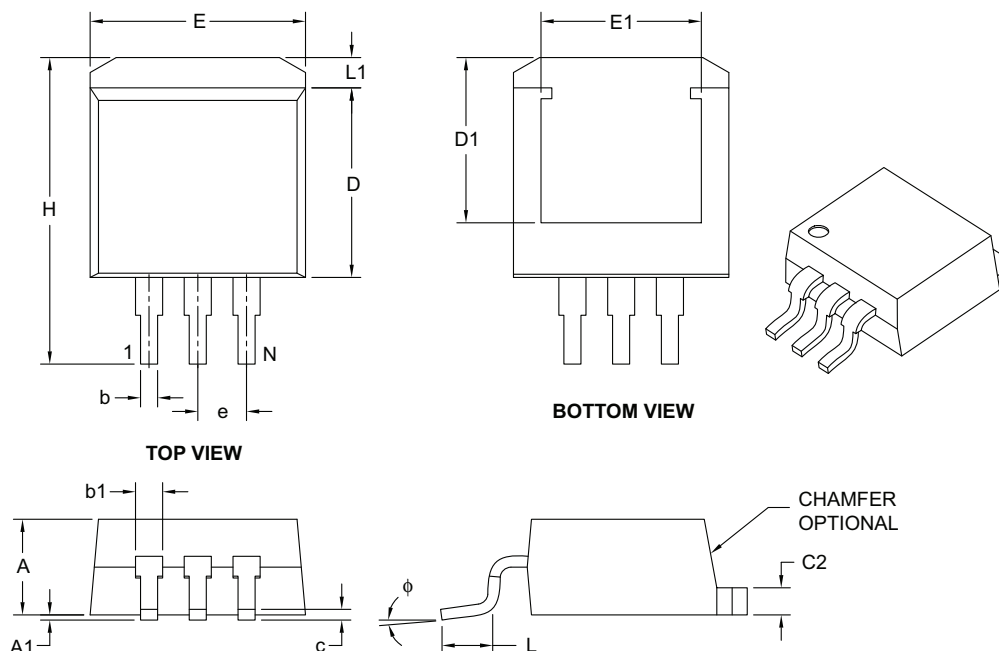
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

MCP1790/MCP1791

3-Lead Plastic (EB) [DDPAK]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	3		
Pitch	e	.100 BSC		
Overall Height	A	.160	—	.190
Standoff §	A1	.000	—	.010
Overall Width	E	.380	—	.420
Exposed Pad Width	E1	.245	—	—
Molded Package Length	D	.330	—	.380
Overall Length	H	.549	—	.625
Exposed Pad Length	D1	.270	—	—
Lead Thickness	c	.014	—	.029
Pad Thickness	C2	.045	—	.065
Lower Lead Width	b	.020	—	.039
Upper Lead Width	b1	.045	—	.070
Foot Length	L	.068	—	.110
Pad Length	L1	—	—	.067
Foot Angle	φ	0°	—	8°

Notes:

- § Significant Characteristic.
- Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

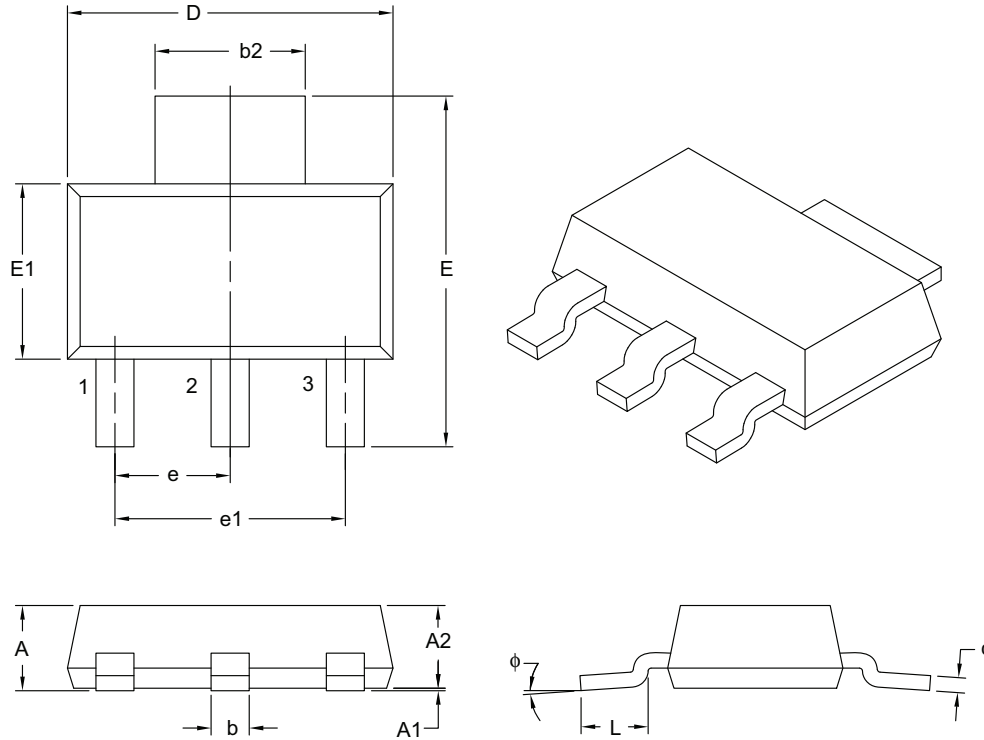
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-011B

MCP1790/MCP1791

3-Lead Plastic Small Outline Transistor (DB) [SOT-223]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Leads	N		3		
Lead Pitch	e		2.30 BSC		
Outside Lead Pitch	e1		4.60 BSC		
Overall Height	A		—	—	1.80
Standoff	A1		0.02	—	0.10
Molded Package Height	A2		1.50	1.60	1.70
Overall Width	E		6.70	7.00	7.30
Molded Package Width	E1		3.30	3.50	3.70
Overall Length	D		6.30	6.50	6.70
Lead Thickness	c		0.23	0.30	0.35
Lead Width	b		0.60	0.76	0.84
Tab Lead Width	b2		2.90	3.00	3.10
Foot Length	L		0.75	—	—
Lead Angle	φ		0°	—	10°

Notes:

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

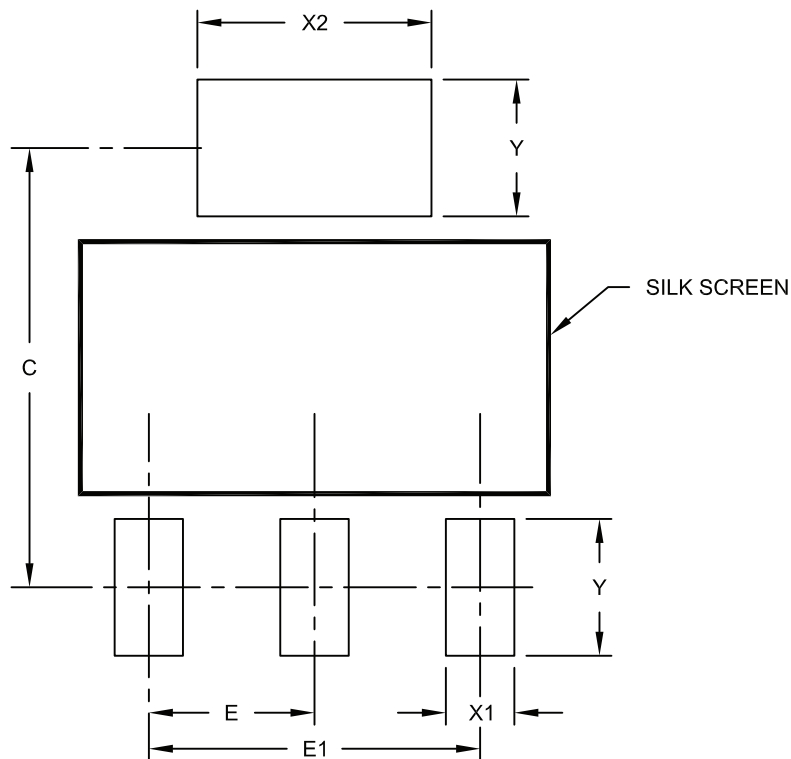
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-032B

MCP1790/MCP1791

3-Lead Plastic Small Outline Transistor (DB) [SOT-223]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	2.30 BSC		
Overall Pitch	E1	4.60 BSC		
Contact Pad Spacing	C		6.10	
Contact Pad Width	X1			0.95
Contact Pad Width	X2			3.25
Contact Pad Length	Y			1.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

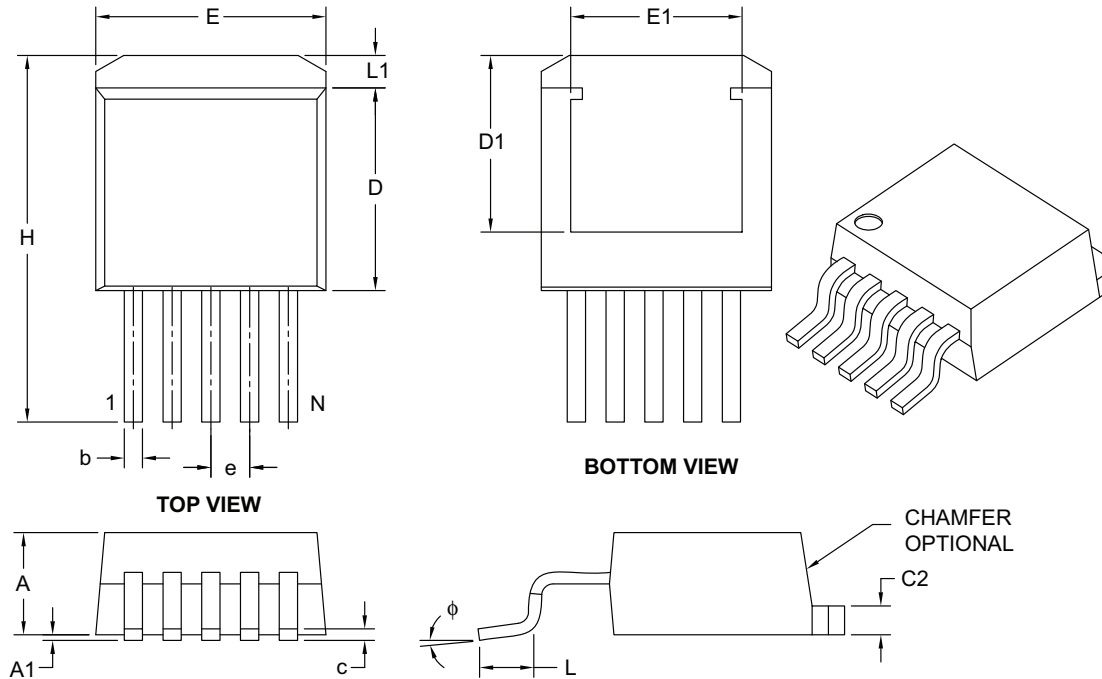
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2032A

MCP1790/MCP1791

5-Lead Plastic (ET) [DDPAK]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	5		
Pitch	e	.067 BSC		
Overall Height	A	.160	—	.190
Standoff §	A1	.000	—	.010
Overall Width	E	.380	—	.420
Exposed Pad Width	E1	.245	—	—
Molded Package Length	D	.330	—	.380
Overall Length	H	.549	—	.625
Exposed Pad Length	D1	.270	—	—
Lead Thickness	c	.014	—	.029
Pad Thickness	C2	.045	—	.065
Lead Width	b	.020	—	.039
Foot Length	L	.068	—	.110
Pad Length	L1	—	—	.067
Foot Angle	φ	0°	—	8°

Notes:

- § Significant Characteristic.
- Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

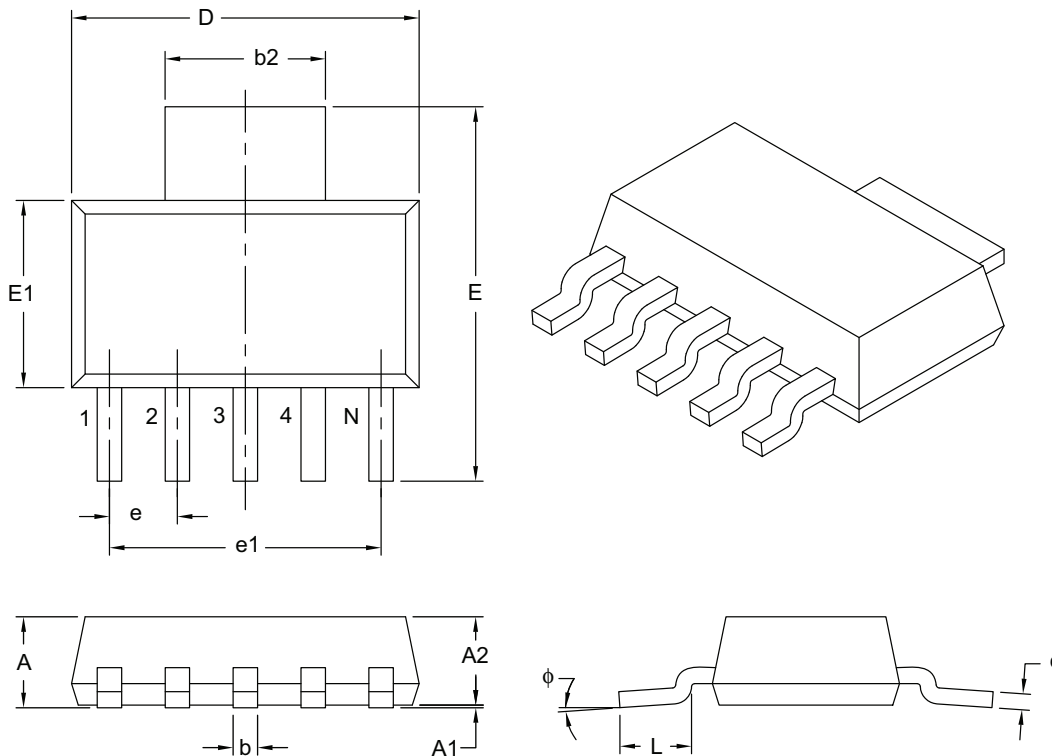
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-012B

MCP1790/MCP1791

5-Lead Plastic Small Outline Transistor (DC) [SOT-223]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Leads	N		5		
Lead Pitch	e		1.27 BSC		
Outside Lead Pitch	e1		5.08 BSC		
Overall Height	A		—	—	1.80
Standoff	A1		0.02	0.06	0.10
Molded Package Height	A2		1.55	1.60	1.65
Overall Width	E		6.86	7.00	7.26
Molded Package Width	E1		3.45	3.50	3.55
Overall Length	D		6.45	6.50	6.55
Lead Thickness	c		0.24	0.28	0.32
Lead Width	b		0.41	0.457	0.51
Tab Lead Width	b2		2.95	3.00	3.05
Foot Length	L		0.91	—	1.14
Lead Angle	φ		0°	4°	8°

Notes:

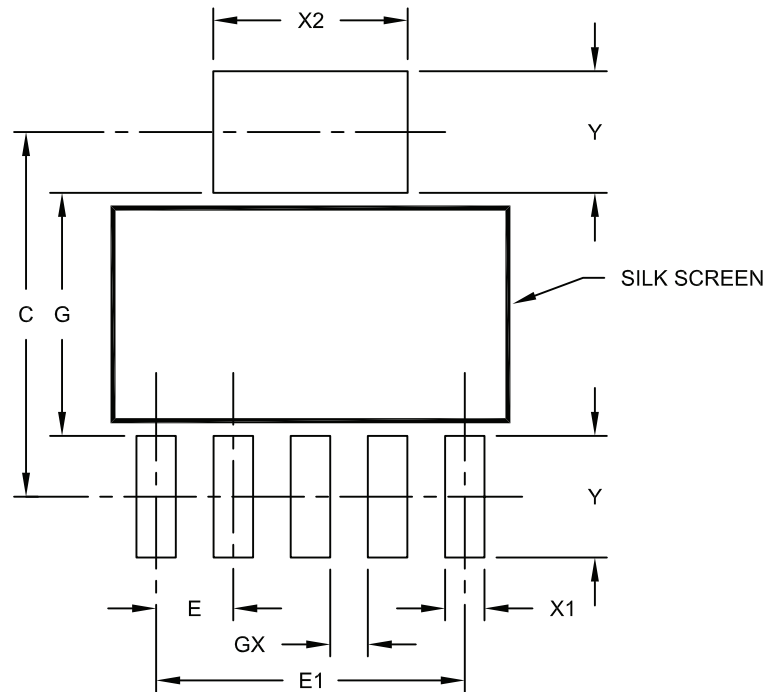
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-137B

5-Lead Plastic Small Outline Transistor (DC) [SOT-223]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packages>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Pad Pitch	E	1.27 BSC		
Overall Pad Pitch	E1	5.08 BSC		
Pad Spacing	C		6.00	
Pad Width	X1			0.65
Pad Width	X2			3.20
Pad Length	Y			2.00
Distance Between Pads	G	4.00		
Distance Between Pads	GX	0.62		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2137A

MCP1790/MCP1791

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (September 2010)

The following is the list of modifications:

- Updated the Features section.
- Removed conditions for the Output Voltage Regulation parameter in the AC/DC Characteristics table.
- Updated the symbol used for the Storage Temperature Range parameter in the TEMPERATURE SPECIFICATIONS table.

Revision A (March 2008)

- Original Release of this Document.

MCP1790/MCP1791

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	X	X	X/	XX
Device	Output Voltage	Feature Code	Tolerance	Temp.	Package
Device: MCP1790: 70 mA High Voltage Regulator MCP1790T: 70 mA High Voltage Regulator Tape and Reel MCP1791: 70 mA High Voltage Regulator MCP1791T: 70 mA High Voltage Regulator Tape and Reel Output Voltage *: 30 = 3.0V "Standard" 33 = 3.3V "Standard" 50 = 5.0V "Standard" *Contact factory for other output voltage options Extra Feature Code: 0 = Fixed Tolerance: 2 = 2.5% (Standard) Temperature: E = -40° C to +125° C Package Type: EB = Plastic, DDPak, 3-lead ET = Plastic, DDPak, 5-lead DB = Plastic Transistor Outline, SOT-223, 3-lead DC = Plastic Transistor Outline, SOT-223, 5-lead					
Examples: a) MCP1790-3002E/EB: 3.0V LDO Regulator, 3LD DDPak b) MCP1790-3302E/EB: 3.3V LDO Regulator, 3LD DDPak c) MCP1790-5002E/EB: 5.0V LDO Regulator, 3LD DDPak d) MCP1790-3002E/DB: 3.0V LDO Regulator, 3LD SOT-223 e) MCP1790-3302E/DB: 3.3V LDO Regulator, 3LD SOT-223 f) MCP1790-5002E/DB: 5.0V LDO Regulator, 3LD SOT-223 a) MCP1791-3002E/ET: 3.0V LDO Regulator 5LD DDPak b) MCP1791-3302E/ET 3.3V LDO Regulator 5LD DDPak c) MCP1791-5002E/ET: 5.0V LDO Regulator 5LD DDPak d) MCP1791-3002E/DC 3.0V LDO Regulator 5LD SOT-223 e) MCP1791-3302E/DC 3.3V LDO Regulator 5LD SOT-223 f) MCP1791-5002E/DC 5.0V LDO Regulator 5LD SOT-223					

MCP1790/MCP1791

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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