MC74AC157, MC74ACT157

Quad 2-Input Multiplexer

The MC74AC157/74ACT157 is a high−speed quad 2−input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (non−inverted) form.

The MC74AC157/74ACT157 can also be used as a function generator.

Features

- Outputs Source/Sink 24 mA
- ′ACT157 Has TTL Compatible Inputs
- These are Pb−Free Devices

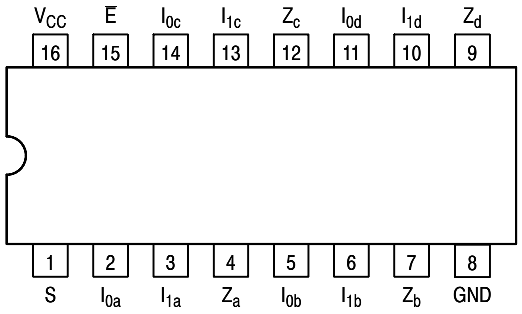

Figure 1. Pinout: 16−Lead Packages Conductors

(Top View)

TRUTH TABLE

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

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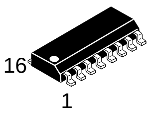
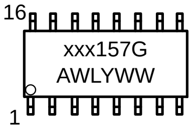
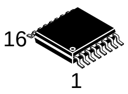
MARKING DIAGRAMS

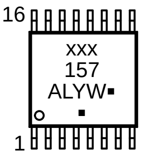


SOIC−16
D SUFFIX
CASE 751B





TSSOP−16
DT SUFFIX
CASE 948F



xxx = AC or ACT
A = Assembly Location
WL or L = Wafer Lot
Y = Year
WW or W = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN NAMES

PIN	FUNCTION
I_{0a}–I_{0d}	Source 0 Data Inputs
I_{1a}–I_{1d}	Source 0 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
Z_a–Z_d	Outputs

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

January, 2015 − Rev. 8

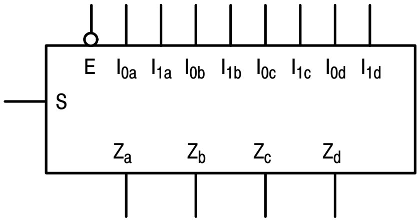


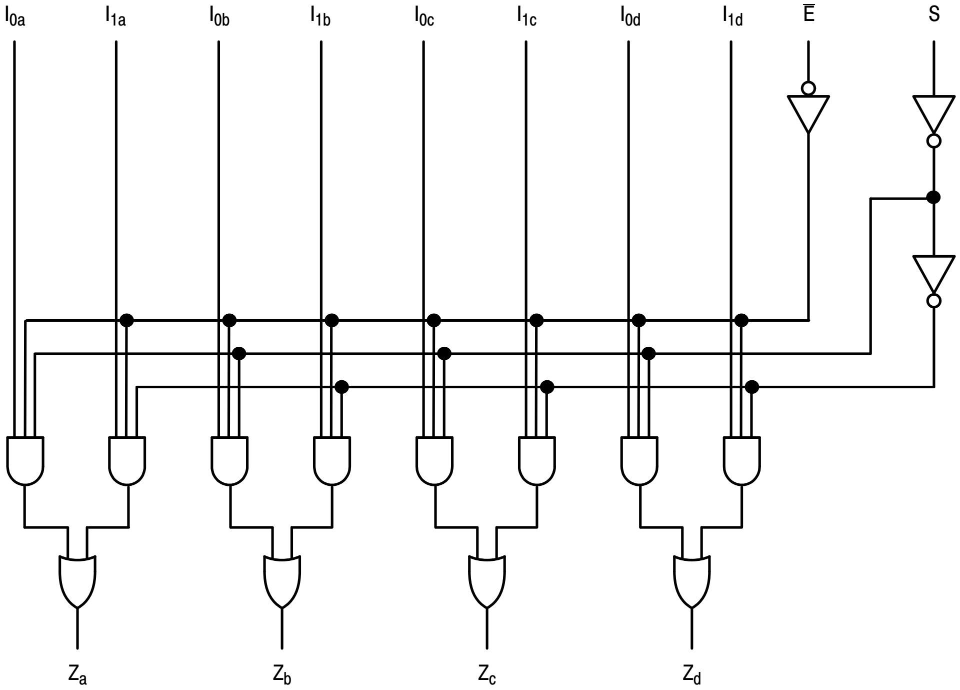
Figure 2. Logic Symbol

FUNCTIONAL DESCRIPTION

The MC74AC157/74ACT157 is a quad 2−input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active−LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The MC74AC157/74ACT157 is the logic implementation of a 4−pole, 2−position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$Z_a = \overline{E}•(I_{1a}•S+I_{0a}•\overline{S})$
$Z_b = \overline{E}•(I_{1b}•S+I_{0b}•\overline{S})$
$Z_c = \overline{E}•(I_{1c}•S+I_{0c}•\overline{S})$
$Z_d = \overline{E}•(I_{1d}•S+I_{0d}•\overline{S})$

A common use of the MC74AC157/74ACT157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The MC74AC157/74ACT157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to $+7.0$	V
V_I	DC Input Voltage	$-0.5 \le V_I \le V_{CC} + 0.5$	V
V_O	DC Output Voltage (Note 1)	$-0.5 \le V_O \le V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	±20	mA
I_{OK}	DC Output Diode Current	±50	mA
I_O	DC Output Sink/Source Current	±50	mA
I_{CC}	DC Supply Current per Output Pin	±50	mA
I_{GND}	DC Ground Current per Output Pin	±50	mA
T_{STG}	Storage Temperature Range	-65 to $+150$	°C
T_L	Lead temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction temperature under Bias	$+150$	°C
θ_{JA}	Thermal Resistance (Note 2) SOIC TSSOP	69.1 103.8	°C/W
P_D	Power Dissipation in Still Air at 65°C (Note 3) SOIC TSSOP	500 500	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 30% − 35%	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 4) Machine Model (Note 5) Charged Device Model (Note 6)	> 2000 > 200 > 1000	V
$I_{Latch-Up}$	Latch−Up Performance Above V_{CC} and Below GND at 85°C (Note 7)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD51−7.
3. 500 mW at 65°C; derate to 300 mW by 10 mW/ from 65°C to 85°C.
4. Tested to EIA/JESD22−A114−A.
5. Tested to EIA/JESD22−A115−A.
6. Tested to JESD22−C101−A.
7. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	′AC	2.0	5.0	6.0	V
		′ACT	4.5	5.0	5.5	
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)		0	−	V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) ′AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V	−	150	−	ns/V
		V_{CC} @ 4.5 V	−	40	−	
		V_{CC} @ 5.5 V	−	25	−	
t_r, t_f	Input Rise and Fall Time (Note 2) ′ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V	−	10	−	ns/V
		V_{CC} @ 5.5 V	−	8.0	−	
T_J	Junction Temperature (PDIP)		−	−	140	°C
T_A	Operating Ambient Temperature Range		−40	25	85	°C
I_{OH}	Output Current − High		−	−	−24	mA
I_{OL}	Output Current − Low		−	−	24	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74AC		74AC	Unit	Conditions
			T_A = +25°C		T_A = −40°C to +85°C		
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 µA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0	−	2.56	2.46	V	*V_{IN} = V_{IL} or V_{IH} −12 mA
		4.5	−	3.86	3.76		I_{OH} −24 mA
		5.5	−	4.86	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 µA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0	−	0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5	−	0.36	0.44		I_{OL} 24 mA
		5.5	−	0.36	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5	−	±0.1	±1.0	µA	V_I = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5	−	−	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	−	−	−75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	−	8.0	80	µA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

AC CHARACTERISTICS (For Figures and Waveforms − See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74AC			74AC		Unit	Fig. No.
			T_A = +25°C C_L = 50 pF			T_A = −40°C to +85°C C_L = 50 pF			
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S to Z_n	3.3	1.5	7.0	11.5	1.5	13.0	ns	3−6
		5.0	1.5	5.5	9.0	1.5	10.0		
t_{PHL}	Propagation Delay S to Z_n	3.3	1.5	6.5	11.0	1.5	12.0	ns	3−6
		5.0	1.5	5.0	8.5	1.0	9.5		
t_{PLH}	Propagation Delay $\overline{E}$ to Z_n	3.3	1.5	7.0	11.5	1.5	13.0	ns	3−6
		5.0	1.5	5.5	9.0	1.5	10.0		
t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n	3.3	1.5	6.5	11.0	1.5	12	ns	3−6
		5.0	1.5	5.5	9.0	1.0	9.5		
t_{PLH}	Propagation Delay I_n to Z_n	3.3	1.5	5.0	8.5	1.0	9.0	ns	3−5
		5.0	1.5	4.0	6.5	1.0	7.0		
t_{PHL}	Propagation Delay I_n to Z_n	3.3	1.5	5.0	8.0	1.0	9.0	ns	3−5
		5.0	1.5	4.0	6.5	1.0	7.0		

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74ACT		74ACT	Unit	Conditions
			T_A = +25°C		T_A = −40°C to +85°C		
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5	− −	3.86 4.86	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5	− −	0.36 0.36	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	−	±0.1	±1.0	μA	V_I = V_{CC}, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6	−	1.5	mA	V_I = V_{CC} − 2.1 V
I_{OLD}	†Minimum Dynamic Output Current	5.5	−	−	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	−	−	−75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	−	8.0	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms − See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74ACT			74ACT		Unit	Fig. No.
			T_A = +25°C C_L = 50 pF			T_A = −40°C to +85°C C_L = 50 pF			
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S to Z_n	5.0	2.0	−	9.0	1.5	10.0	ns	3−6
t_{PHL}	Propagation Delay S to Z_n	5.0	2.0	−	9.5	2.0	10.5	ns	3−6
t_{PLH}	Propagation Delay $\overline{E}_n$ to Z_n	5.0	1.5	−	10	1.5	11.5	ns	3−6
t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n	5.0	1.5	−	8.5	1.0	9.0	ns	3−6
t_{PLH}	Propagation Delay I_n to Z_n	5.0	1.5	−	7.0	1.0	8.5	ns	3−5
t_{PHL}	Propagation Delay I_n to Z_n	5.0	1.5	−	7.5	1.0	8.5	ns	3−5

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value − Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	50	pF	V_{CC} = 5.0 V

ORDERING INFORMATION

Device Order Number	Package	Shipping†
MC74AC157DG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74AC157DR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel
MC74AC157DTR2G	TSSOP−16 (Pb−Free)	2500 Tape & Reel
MC74ACT157DG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74ACT157DR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel
MC74ACT157DTR2G	TSSOP−16 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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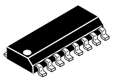

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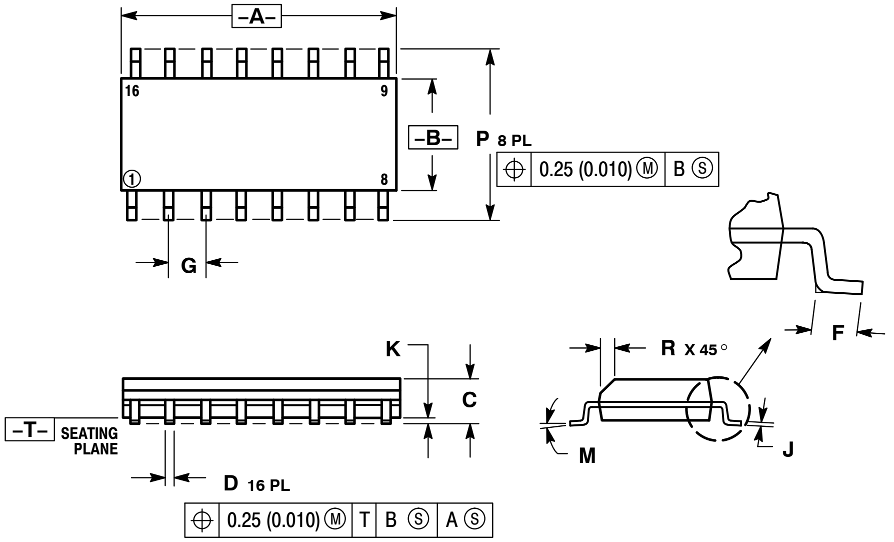
SOIC−16
CASE 751B−05
ISSUE K

DATE 29 DEC 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

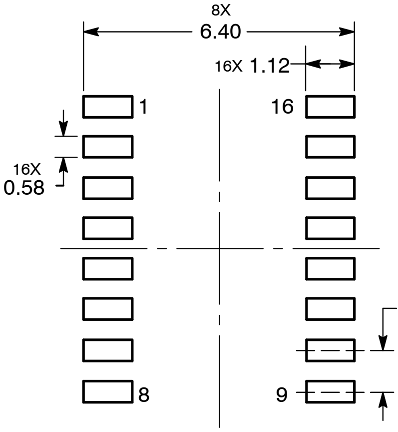
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

DOCUMENT NUMBER:	**98ASB42566B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−16**		**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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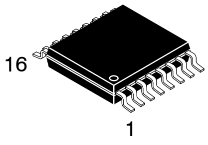
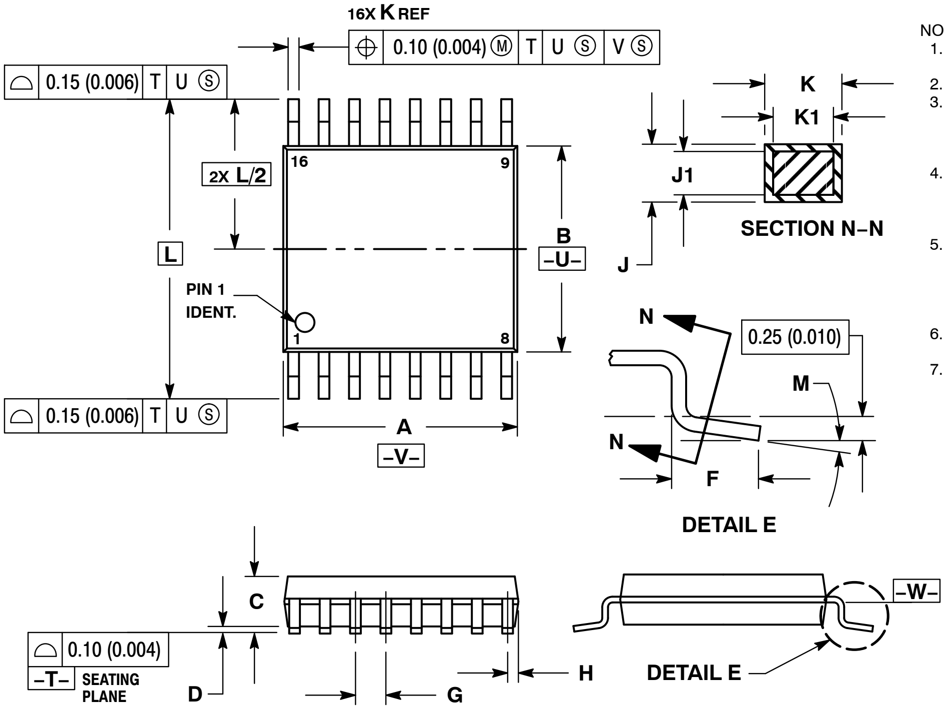


SCALE 2:1

TSSOP−16
CASE 948F−01
ISSUE B

DATE 19 OCT 2006

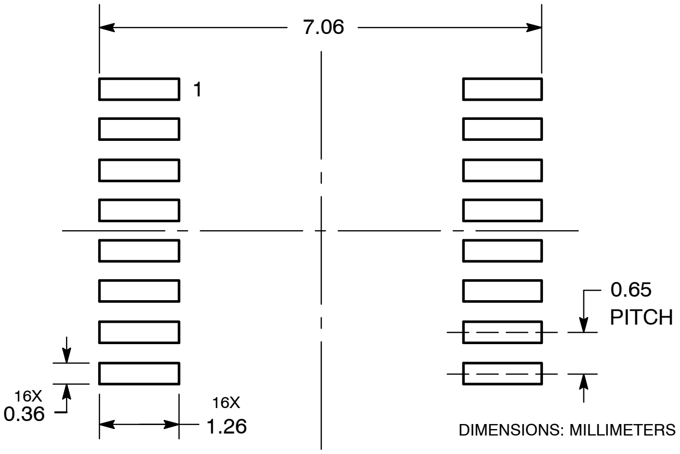


NOTES:

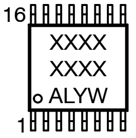
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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