ABSOLUTE MAXIMUM RATINGS

V _{DD} to GND	-0.3V to +6V
C1P to GND	
C1N to GND	(V _{SS} - 0.3V) to +0.3V
V _{SS} to GND	-6V to +0.3V
OUTR, OUTL to GND	±3V
SHDN to GND	-0.3V to +6V
INR, INL to GND	-0.3V to (V _{DD} + 0.3V)
OUTR, OUTL Short Circuit to GND, VD	DContinuous
Short Circuit Between OUTL and OUTF	RContinuous
Continuous Input Current (Into All Othe	er Pins)±20mA
Continuous Power Dissipation ($T_A = +T_A$	70°C)
10-Pin TDFN Single-Layer PCB (dera	ate 18.5mW/°C
above +70°C)	1481.5mW
Junction-to-Case Thermal Resistance	(θ _{JC}) (Note 1)
10-Pin TDFN	8.5°C/W

Junction-to-Ambient Thermal Resistance (θJA) (Note 1) 10-Pin TDFN41.0°C/W	/
Continuous Power Dissipation ($T_A = +70^{\circ}C$)	
10-Pin TDFN Multilayer PCB (derate 24.4mW/°C	
above +70°C)1951mW	[
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1)	
10-Pin TDFN	[
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)	
10-Pin TDFN	1
Dperating Temperature Range40°C to +85°C	;
Storage Temperature Range65°C to +150°C	;
Junction Temperature+150°C	;
_ead Temperature (soldering, 10s)+300°C	,

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a fourlayer board. For detailed information on package thermal considerations, refer to <u>www.maxim-ic.com/thermal-tutorial</u>.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

 $(V_{DD} = V_{SHDN} = 5V, V_{GND} = 0V, R_{IN} = R_{FB} = 40.2k\Omega$ (gain = -1V/V), C1 = C2 = 1µF, C3 = 10µF, R_{LOAD} = ∞, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	ТҮР	МАХ	UNITS
GENERAL							
Supply Voltage Range	V _{DD}	Guaranteed by PSRR test		2.7		5.5	V
Undervoltage Lockout	UVLO			2.2			V
		$V_{DD} = 3.3V$			3.0	4.6	m۸
	UDI	$V_{DD} = 5V$			4.0	6.0	ΠA
Shutdown Current	ISHDN	$V_{\overline{SHDN}} = 0V, T_A = +25^{\circ}C$			< 0.1	1	μΑ
Output Signal Attenuation in Shutdown		$V_{SHDN} = 0V, V_{IN} = 1V_{RMS}, R_{LOAD}$	= 10kΩ		-110		dBV
Output Impedance in Shutdown		V _{SHDN} = 0V			0.6		kΩ
Turn-On Time	ton				0.56		ms
Output Offset Voltage	Vos	$T_A = +25^{\circ}C$ (Note 3)			±0.1	±0.5	mV
		$Z_{LOAD} = 32\Omega + 1\mu$ H, peak	Into shutdown		-79		
Click-and-Pop Level	Кср	per second (Notes 3, 4)	Out of shutdown		-77		dBV
	NCF	$Z_{LOAD} = 10k\Omega$, peak voltage,	Into shutdown		-62		ub v
		A-weighted, 32 samples per second (Notes 3, 4)	Out of shutdown		-58		

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{DD} = V_{SHDN} = 5V, V_{GND} = 0V, R_{IN} = R_{FB} = 40.2k\Omega$ (gain = -1V/V), C1 = C2 = 1µF, C3 = 10µF, R_{LOAD} = ∞, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	COND	ITIONS		MIN	ТҮР	МАХ	UNITS
		V_{DD} = 2.7V to 5.5V, T_A =	+25°C (No	te 3)	75	90		
Power-Supply Rejection Ratio	PSRR	f = 1 kHz, 200mV _{P-P} (Note	e 3)			73		dB
		f = 20kHz, 200mV _{P-P} (No	te 3)			55		
		$Z_{LOAD} = 32\Omega + 1\mu H, f = 1$	1kHz,	$V_{DD} = 3.6V$		45		
Output Dowor	Davia	THD+N = 1%		$V_{DD} = 5.0V$		95		
Output Power	POUT	Z_{LOAD} = 16 Ω + 1 μ H, f = 1	1kHz,	$V_{DD} = 3.6V$		32		TTIVV
		THD+N = 1%		$V_{DD} = 5.0V$		75]
		$Z_{LOAD} = 16\Omega + 1\mu H$, f =	1kHz, P _{OU} -	T = 20mW		0.014		
I otal Harmonic Distortion	THD+N	$Z_{LOAD} = 32\Omega + 1\mu H$, f =	1kHz, Pou ⁻	T = 20mW		0.005		%
		$Z_{LOAD} = 10k\Omega$, f = 1kHz,	$V_{OUT} = 1V$	'RMS		0.001		
Signal-to-Noise Ratio	SNR	$Z_{LOAD} = 32\Omega + 1\mu H, P_{OI}$	_{JT} = 25mW	, A-weighted		105		dB
Output Noise	V _{NOISE}	A-weighted (Note 3)				9		μV
Ore estalle		L to R, R to L,	Z _{LOAD} FS = 0. V _{OUT} =	$Z_{LOAD} = 32\Omega + 1\mu H$ FS = 0.300V _{RMS} , V _{OUT} = 30mV _{RMS}		73		
Crosstaik		BW = 20Hz to 15kHz	Z _{LOAD} FS = 0. V _{OUT} =	= 10kΩ .707V _{RMS} , = 70.7mV _{RMS}		73		uв
Capacitive Load Drive	CL	No sustained oscillations				200		рF
Oscillator Frequency	fosc	$T_A = +25^{\circ}C$			300	500	800	kHz
Thermal Shutdown						145		°C
Thermal Shutdown Hysteresis						15		°C
DIGITAL INPUT (SHDN)								
Input Voltage High	VINH				1.2			V
Input Voltage Low	VINL						0.3	V
Input Leakage Current	ILEAKAGE	$T_A = +25^{\circ}C$					±1	μA

Note 2: All specifications are 100% tested at $T_A = +25$ °C; temperature limits are guaranteed by design.

Note 3: The amplifier inputs are AC-coupled to GND.

Note 4: Mode transitions are controlled by SHDN.

Typical Operating Characteristics

 $(V_{DD} = V_{SHDN} = 5V, V_{GND} = 0V, R_{IN} = R_{FB} = 40.2k\Omega$ (gain = -1V/V), C1 = C2 = 1µF, C3 = 10µF, R_{LOAD} = ∞. Typical values are at T_A = +25°C, unless otherwise noted.)



THD+N vs. OUTPUT POWER







THD+N vs. OUTPUT POWER



THD+N vs. OUTPUT POWER 10 $V_{DD} = 3.6V$ $R_{LOAD} = 32\Omega$ $L_{LOAD}=1\mu H$ 1 THD+N (%) f = 100Hz f = 6 kHz0.1 0.01 f = 1kHz = 0.001 0.01 0.02 0.03 0.04 0.05 0.06 0.07 0.08 0 OUTPUT POWER (W)

THD+N vs. FREQUENCY



Δ

_Typical Operating Characteristics

 $(V_{DD} = V_{SHDN} = 5V, V_{GND} = 0V, R_{IN} = R_{FB} = 40.2k\Omega$ (gain = -1V/V), C1 = C2 = 1µF, C3 = 10µF, R_{LOAD} = ∞. Typical values are at T_A = +25°C, unless otherwise noted.)



VISTA THD+N vs. FREQUENCY







M/IXI/M



VISTA THD+N vs. FREQUENCY



OUTPUT POWER vs. SUPPLY VOLTAGE



Typical Operating Characteristics (continued)

 $(V_{DD} = V_{SHDN} = 5V, V_{GND} = 0V, R_{IN} = R_{FB} = 40.2 k\Omega$ (gain = -1V/V), C1 = C2 = 1µF, C3 = 10µF, R_{LOAD} = ∞. Typical values are at T_A = +25°C, unless otherwise noted.)















POWER-SUPPLY REJECTION RATIO vs. Supply Voltage



6



 $(V_{DD} = V_{\overline{SHDN}} = 5V, V_{GND} = 0V, R_{IN} = R_{FB} = 40.2k\Omega$ (gain = -1V/V), C1 = C2 = 1µF, C3 = 10µF, R_{LOAD} = ∞. Typical values are at T_A = +25°C, unless otherwise noted.)



MAX9820

PIN	NAME	FUNCTION
1	C1P	Flying Capacitor Positive Terminal. Connect a 1µF ceramic capacitor from C1P to C1N.
2	C1N	Flying Capacitor Negative Terminal. Connect a 1µF ceramic capacitor from C1N to C1P.
3	VSS	Charge-Pump Output. Bypass with a 1µF capacitor to GND.
4	OUTL	Left-Channel Output
5	OUTR	Right-Channel Output
6	INR	Right-Channel Input
7	INL	Left-Channel Input
8	V _{DD}	Positive Power-Supply Input. Bypass with a 10µF capacitor to GND.
9	SHDN	Active-Low Shutdown Input
10	GND	Signal Ground
_	EP	Exposed Pad. Internally connected to GND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

Detailed Description

The MAX9820 95mW stereo headphone amplifier features Maxim's DirectDrive architecture, eliminating the large output-coupling capacitors required by conventional single-supply headphone amplifiers. The device features low RF susceptibility, extensive click-and-pop suppression, undervoltage lockout (UVLO) and shutdown control. The MAX9820 also features thermal-overload and short-circuit protection.

The MAX9820 is Windows Vista Premium Mobile compliant (Table 1).

DirectDrive

MIXIM

Conventional single-supply headphone amplifiers have their outputs biased about a nominal DC voltage (typically half the supply) for maximum dynamic range. Large-coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both headphone and headphone amplifier.

Maxim's DirectDrive architecture uses a charge pump to create an internal negative supply voltage, allowing the MAX9820 outputs to be biased at

DEVICE TYPE	REQUIREMENT	WINDOWS VISTA PREMIUM MOBILE SPECIFICATIONS	MAX9820 TYPICAL PERFORMANCE
	THD+N	≤ -65dB FS (100Hz, 20kHz)	-83dBFS (100Hz, 20kHz)
Analog Line Output Jack ($R_L = 10k\Omega$, ES = 0.707VBMS)	Dynamic range with signal present	≤ -80dBV, A-weighted (20Hz, 20kHz)	-101dB A-weighted (20Hz, 20kHz)
	Line output crosstalk	≤ -50dB (20Hz, 15kHz)	-73dB (20Hz, 15kHz)
	THD+N	≤ -45dB FS (100Hz, 20kHz)	-85dBFS (100Hz, 20kHz)
Analog Headphone Out Jack ($R_L = 32\Omega$, ES = 0.300/PMS)	Dynamic range with signal present	≤ -60dBV, A-weighted (20Hz, 20kHz)	-94dB A-weighted (20Hz, 20kHz)
	Headphone output crosstalk	≤ -50dB (20Hz, 15kHz)	-73dB (20Hz, 15kHz)

Table 1. Windows Vista Premium Mobile Specifications vs. MAX9820 Specifications

Note: THD+N, dynamic range, and crosstalk are measured in accordance with AES-17 audio measurements standards.



Figure 1. Conventional Driver Output Waveform vs. MAX9820 Output Waveform

GND (Figure 1). With no DC component, there is no need for the large DC-blocking capacitors. The MAX9820 charge pump requires two small ceramic capacitors, conserving board space, reducing cost, and improving the frequency response of the headphone amplifier.

Charge Pump

The MAX9820 features a low-noise charge pump. The 500kHz (typ) charge pump switching frequency is well beyond the audio range and does not interfere with audio signals.



Figure 2. MAX9820 RF Susceptibility

Click-and-Pop Suppression

In conventional single-supply audio amplifiers, the output-coupling capacitor contributes significantly to audible clicks and pops. Upon startup, the amplifier charges the coupling capacitor to its bias voltage, typically half the supply. Likewise, on shutdown, the capacitor is discharged. This results in a DC shift across the capacitor, which appears as an audible transient at the speaker. Since DirectDrive biases the outputs at ground, this problem does not arise. Additionally, the MAX9820 features extensive click-and-pop suppression that eliminates any audible transient sources internal to the device.

RF Susceptibility

Modern audio systems are often subject to RF radiation from sources such as wireless and cellular phone networks. Although the RF radiation is out of the audio band, many signals, GSM signals in particular, contain bursts or modulation at audible frequencies. Most analog amplifiers demodulate the low-frequency envelope, adding noise to the audio signal. The MAX9820 architecture addresses the RF susceptibility problem by rejecting RF noise and preventing it from coupling into the audio band.



MAX9820



Shutdown

The MAX9820 features a low-power shutdown mode that reduces quiescent current consumption to less than 1µA, extending battery life for portable applications. Drive SHDN low to disable the amplifiers and the charge pump. In shutdown mode, the amplifier output impedance is set to 600Ω II R_{FB}. The amplifiers and charge pump are enabled once SHDN is driven high.

Applications Information

Power Dissipation

Under normal operating conditions, linear power amplifiers can dissipate a significant amount of power. The maximum power dissipation for each package is given in the *Absolute Maximum Ratings* section or can be calculated by the following equation:

$$P_{\text{DISSPKG}(\text{MAX})} = \frac{T_{\text{J}(\text{MAX})} - T_{\text{A}}}{\theta_{\text{JA}}}$$

where $T_{J(MAX)}$ is +150°C, T_A is the ambient temperature, and θ_{JA} is the reciprocal of the derating factor in °C/W as specified in the *Absolute Maximum Ratings* section.

The MAX9820 has two power dissipation sources: a charge pump and the two output amplifiers. If power dissipation for a given application exceeds the maximum allowed package power dissipation, reduce V_{DD}, increase load impedance, decrease the ambient temperature, or add heatsinking to the device. Large output, supply, and ground traces decrease θ_{JA} , allowing more heat to be transferred from the package to the surrounding air.

Thermal-overload protection limits total power dissipation in the MAX9820. When the junction temperature exceeds 145°C (typ), the thermal protection circuitry disables the amplifier output stage. The amplifiers are enabled once the junction temperature cools by approximately 15°C.

Undervoltage Lockout (UVLO)

The MAX9820 features a UVLO function that prevents the device from operating if the supply voltage falls below 2.2V (min). This feature ensures proper operation during brownout conditions and prevents deep battery discharge. Once the supply voltage reaches the minimum supply voltage range, the MAX9820 charge pump is turned on and the amplifiers are powered, provided that <u>SHDN</u> is high.

Component Selection

Input-Coupling Capacitor

The input capacitor (C_{IN}), in conjunction with the input resistor (R_{IN}), forms a highpass filter that removes the DC bias from an incoming signal (see the *Functional Diagram/Typical Operating Circuit*). The AC-coupling capacitor allows the device to bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN}C_{IN}}$$

Choose the C_{IN} such that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the device's low-frequency response. Use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, can result in increased distortion at low frequencies.

Charge-Pump Capacitor Selection

/V//XI/VI

Use ceramic capacitors with a low ESR for optimum performance. For optimal performance over the extended temperature range, select capacitors with an X7R or X5R dielectric. Table 2 lists suggested manufacturers.

Table 2. Suggestee	d Capacitor	Vendors
--------------------	-------------	---------

SUPPLIER	PHONE	FAX	WEBSITE
Taiyo Yuden	800-348-2496	847-925-0899	www.t-yuden.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com
Murata	770-436-1300	770-436-3030	www.murata.com

Amplifier Gain

The gain of the MAX9820 is set externally using input and feedback resistors (see the *Functional Diagram/ Typical Operating Circuit*). The gain is:

$$A_{V} = -\frac{R_{FB}}{R_{IN}}(V/V)$$

Choose feedback resistor values in the tens of $\mbox{k}\Omega$ range.

Layout and Grounding

MAX9820

Proper layout and grounding are essential for optimum performance. Connect EP and GND together at a single point on the PCB. Ensure ground return resistance is minimized for optimum crosstalk performance. Place the power-supply bypass capacitor, the charge-pump hold capacitor, and the charge-pump flying capacitor as close as possible to the MAX9820. Route all traces that carry switching transients away from the audio signal path.



_Functional Diagram/Typical Operating Circuit

Chip Information

PROCESS: BICMOS

Package Information



MAX9820

Package Information (continued)

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

	DIMENS	SIONS		PACKAGE VA	RIAT	IONS					
SYMBOL	MIN.	MAX.	1	PKG. CODE	Ν	D2	E2	е	JEDEC SPEC	b	[(N/2)-1] x e
А	0.70	0.80	1	T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229/WEEA	0.40±0.05	1.90 REF
D	2.90	3.10	1	T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
E	2.90	3.10	1	T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
A1	0.00	0.05	1	T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
L	0.20	0.40	1	T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
k	0.25	MIN.	1	T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC		0.20±0.05	2.40 REF
A2	0.20	REF.	1	T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC		0.20±0.05	2.40 REF
NOTES:											
NOTES: 1. ALL I 2. COPL 3. WARF 4. PACK 5. DRAW 6. "N" I 7. NUME 8. MARK	Dimension Anarity Age Lei Ving Co S The Ber Of Ving Is	DNS AR 'SHALL IALL NC NGTH/F NFORM TOTAL I LEADS FOR P/	E IN mm NOT EXC T EXCEEL ACKAGE N TO JEDI NUMBER (SHOWN A ACKAGE 0	. ANGLES IN SEED 0.08 m) 0.10 mm. VIDTH ARE CC G M0229, E SF LEADS. IRE FOR REFI RIENTATION R	DEGF m. DNSID XCEP EREN EFER	REES. DERED AS S T DIMENSIO CE ONLY. ENCE ONLY	PECIAL CHA NS "D2" AM	RACTERISTI ID "E2", AN	C(S). ND T1433-1 & T	1433–2.	

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