# Micropower, Ultra-Small, Single/Dual/Quad, Single-Supply Comparators

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD}$ to $V_{SS}$) ....................................-0.3V to +6V
Voltage Inputs (IN+, IN- to $V_{SS}$). ................-0.3V to ($V_{DD}$ + 0.3V)
Differential Input Voltage (IN+ to IN-)...................................6.6V
Current into Input Pins .....................................................±20mA
Output Short-Circuit Duration ..................2s to Either $V_{DD}$ or $V_{SS}$
Current into Any Pin ...........................................................20mA
Continuous Power Dissipation ($T_A$ = +70°C)
5-Pin SC70 (derate 3.1mW/°C above +70°C)...............247mW
5-Pin SOT23 (derate 7.1mW/°C above +70°C)............571mW
8-Pin SOT23 (derate 9.1mW/°C above +70°C)............727mW
8-Pin µMAX (derate 4.5mW/°C above +70°C) .............362mW
8-Pin SO (derate 5.88mW/°C above +70°C)................471mW
14-Pin TSSOP (derate 9.1mW/°C above +70°C) ..........727mW
14-Pin SO (derate 8.3mW/°C above +70......................667mW
Operating Temperature Range
Automotive Application...................................-40°C to +125°C
Junction Temperature .....................................................+150°C
Storage Temperature Range .............................-65°C to +150°C
Lead Temperature (soldering, 10s) ................................+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = 5V, $V_{SS}$ = 0, $V_{CM}$ = 0, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 1)

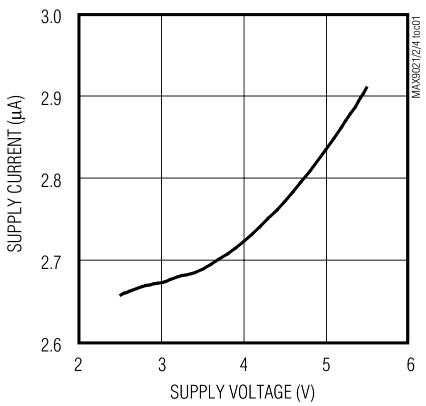
| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Operating Voltage Range | $V_{DD}$ | Guaranteed by PSRR test | | 2.5 | | 5.5 | V |
| Supply Current Per Comparator | $I_{DD}$ | | | | 2.8 | 5 | µA |
| Input Offset Voltage | $V_{OS}$ | (Note 2) | | | ±1 | ±8 | mV |
| Input Offset Voltage Temperature Coefficient | $TCV_{OS}$ | | | | ±1 | | µV/°C |
| Hysteresis | | (Note 3) | | | 4 | | mV |
| Input Bias Current | $I_{BIAS}$ | | | | 3 | 80 | nA |
| Input Offset Current | $I_{OS}$ | | | | ±2 | ±60 | nA |
| Common-Mode Voltage Range | $V_{CM}$ | Guaranteed by CMRR test | | $V_{SS}$ | | $V_{DD}$ - 1.1 | V |
| Common-Mode Rejection Ratio | CMRR | $V_{SS} \le V_{CM} \le (V_{DD} - 1.1V)$, $V_{DD}$ = 5.5V | | 70 | 100 | | dB |
| Power-Supply Rejection Ratio | PSRR | $V_{DD}$ = 2.5V to 5.5V | | 60 | 80 | | dB |
| Output-Voltage Swing | $V_{OL}$, $V_{OH}$ | $V_{OH} = V_{DD} - V_{OUT}$, $(V_{IN+} - V_{IN-}) \ge 20mV$ | $I_{SOURCE}$ = 10µA | | 2 | | mV |
| | | | $I_{SOURCE}$ = 4mA | | 160 | 400 | |
| | | $V_{OL} = V_{OUT} - V_{SS}$, $(V_{IN-} - V_{IN+}) \ge 20mV$ | $I_{SINK}$ = 10µA | | 2 | | |
| | | | $I_{SINK}$ = 4mA | | 180 | 400 | |
| Output Short-Circuit Current | $I_{SC}$ | | | | 50 | | mA |
| Propagation Delay | $t_{pd+}$, $t_{pd-}$ | $R_L$ = 10kΩ, $C_L$ = 15pF (Note 4) | $V_{OD}$ = 10mV | | 8 | | µs |
| | | | $V_{OD}$ = 100mV | | 3 | | |
| Rise and Fall Time | $t_R$, $t_F$ | $R_L$ = 10kΩ, $C_L$ = 15pF (Note 5) | | | 20 | | ns |
| Power-On Time | | $R_L$ = 10kΩ, $C_L$ = 15pF | | | 150 | | ns |
| Maximum Capacitive Load | $C_L$ | No sustained oscillations | | | 150 | | pF |

**Note 1:** All devices are production tested at 25°C. All temperature limits are guaranteed by design.
**Note 2:** Comparator Input Offset is defined as the center of the hysteresis zone.
**Note 3:** Hysteresis is defined as the difference of the trip points required to change comparator output states.
**Note 4:** $V_{OD}$ is the overdrive voltage beyond the offset and hysteresis-determined trip points.
**Note 5:** Rise and fall times are measured between 10% and 90% at OUT.

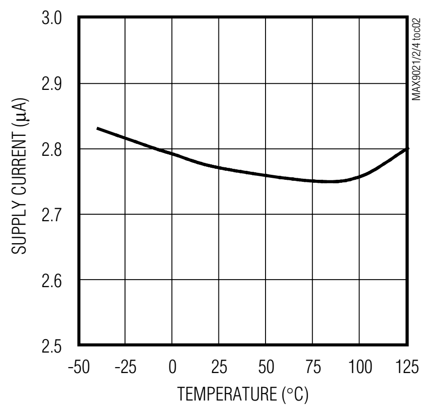
## Typical Operating Characteristics

($V_{DD}$ = 5V, $V_{SS}$ = 0, $V_{CM}$ = 0, $R_L$ = 10kΩ, $C_L$ = 15pF, $V_{OD}$ = 100mV, $T_A$ = +25°C, unless otherwise noted.)

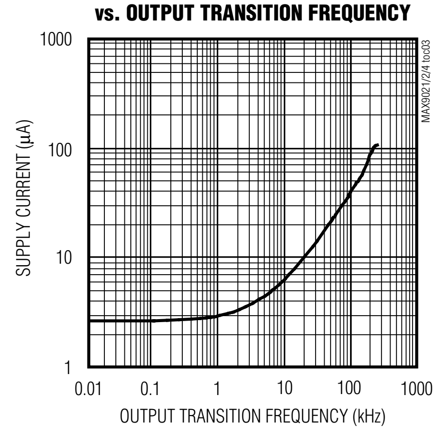
**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



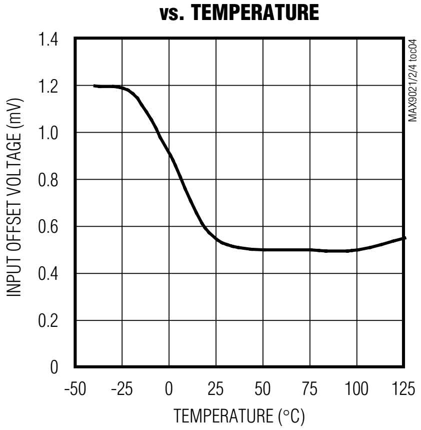

**SUPPLY CURRENT vs. TEMPERATURE**



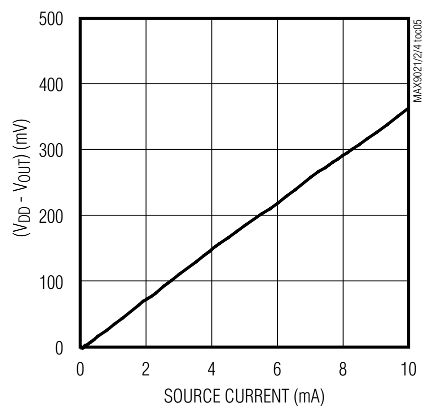

**SUPPLY CURRENT vs. OUTPUT TRANSITION FREQUENCY**



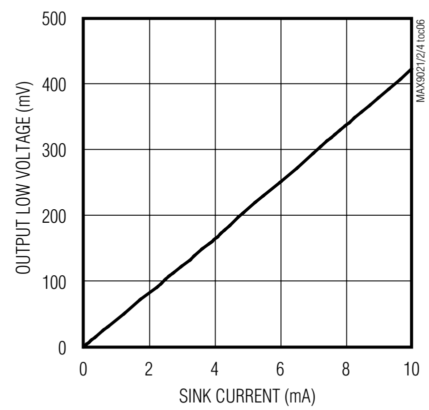

**INPUT OFFSET VOLTAGE vs. TEMPERATURE**



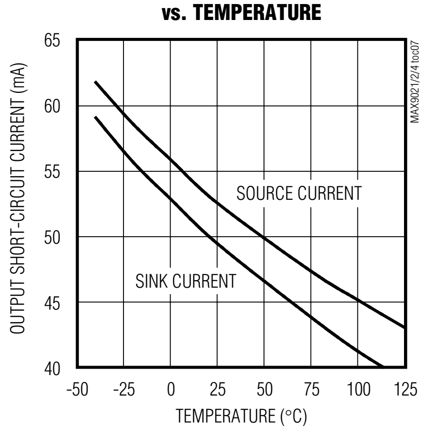

**OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT**



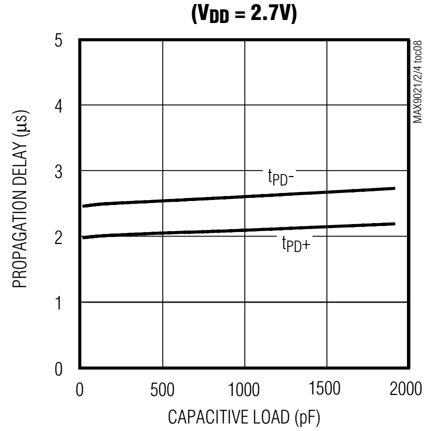

**OUTPUT LOW VOLTAGE vs. SINK CURRENT**



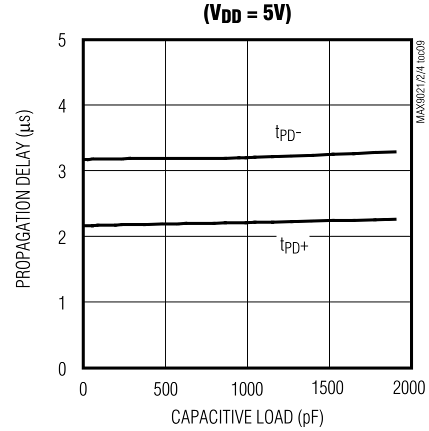

**OUTPUT SHORT-CIRCUIT CURRENT vs. TEMPERATURE**




**PROPAGATION DELAY vs. CAPACITIVE LOAD ($V_{DD}$ = 2.7V)**




**PROPAGATION DELAY vs. CAPACITIVE LOAD ($V_{DD}$ = 5V)**

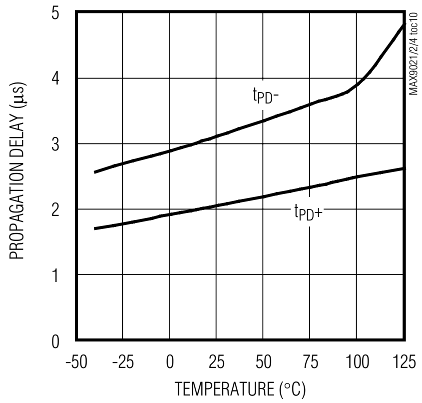


# Micropower, Ultra-Small, Single/Dual/Quad, Single-Supply Comparators

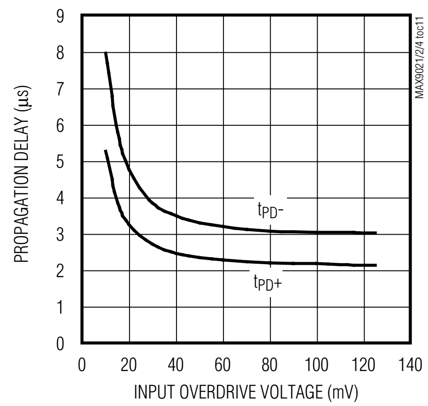
## Typical Operating Characteristics (continued)

($V_{DD}$ = 5V, $V_{SS}$ = 0, $V_{CM}$ = 0, $R_L$ = 10kΩ, $C_L$ = 15pF, $V_{OD}$ = 100mV, $T_A$ = +25°C, unless otherwise noted.)

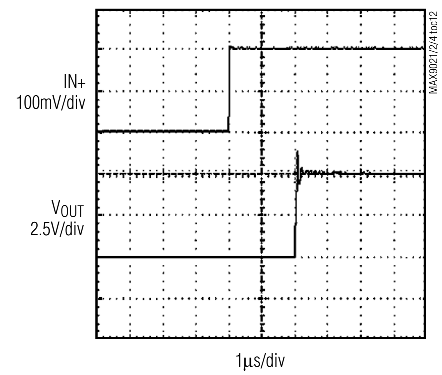
**PROPAGATION DELAY vs. TEMPERATURE**



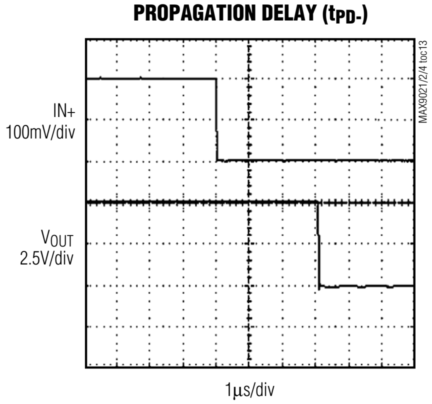

**PROPAGATION DELAY vs. INPUT OVERDRIVE VOLTAGE**



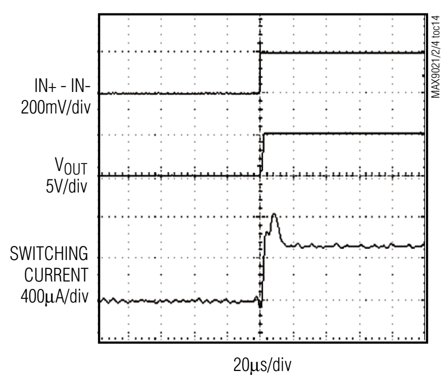

**PROPAGATION DELAY ($t_{PD+}$)**



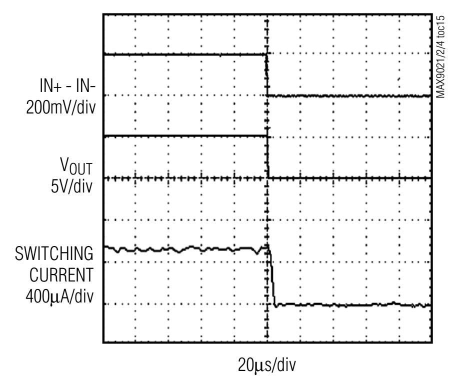

**PROPAGATION DELAY ($t_{PD-}$)**



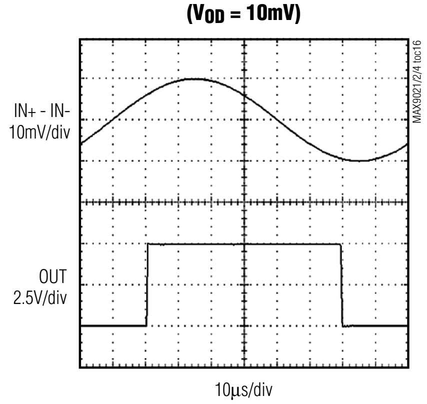

**OUTPUT SWITCHING CURRENT, RISING**



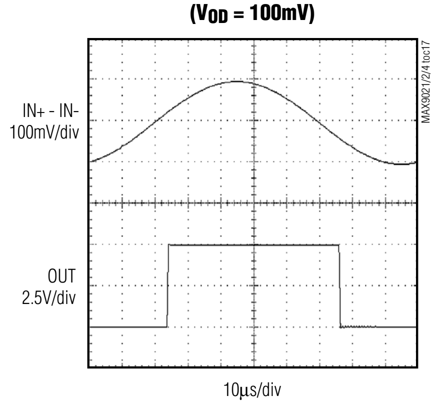

**OUTPUT SWITCHING CURRENT, FALLING**



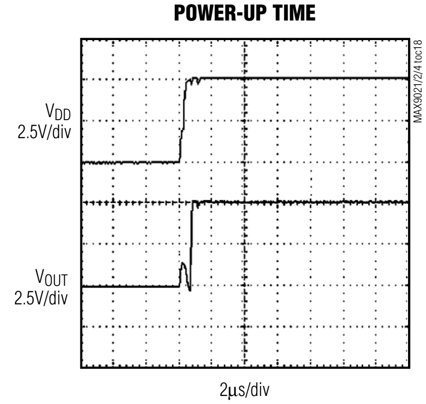

**10kHz RESPONSE ($V_{OD}$ = 10mV)**




**10kHz RESPONSE ($V_{OD}$ = 100mV)**




**POWER-UP TIME**



## Pin Description

| PIN | | | NAME | FUNCTION |
|---|---|---|---|---|
| MAX9021 | MAX9022 | MAX9024 | | |
| 1 | — | — | IN+ | Comparator Noninverting Input |
| 2 | 4 | 11 | $V_{SS}$ | Negative Supply Voltage |
| 3 | — | — | IN- | Comparator Inverting Input |
| 4 | — | — | OUT | Comparator Output |
| 5 | 8 | 4 | $V_{DD}$ | Positive Supply Voltage. Bypass with a 0.1µF capacitor to GND. |
| — | 1 | 1 | OUTA | Comparator A Output |
| — | 2 | 2 | INA- | Comparator A Inverting Input |
| — | 3 | 3 | INA+ | Comparator A Noninverting Input |
| — | 5 | 5 | INB+ | Comparator B Noninverting Input |
| — | 6 | 6 | INB- | Comparator B Inverting Input |
| — | 7 | 7 | OUTB | Comparator B Output |
| — | — | 8 | OUTC | Comparator C Output |
| — | — | 9 | INC- | Comparator C Inverting Input |
| — | — | 10 | INC+ | Comparator C Noninverting Input |
| — | — | 12 | IND+ | Comparator D Noninverting Input |
| — | — | 13 | IND- | Comparator D Inverting Input |
| — | — | 14 | OUTD | Comparator D Output |

## Detailed Description

The MAX9021/MAX9022/MAX9024 are single/dual/quad, low-cost, low-power comparators that consume only 2.8µA and provide a propagation delay, $t_{PD}$, typically 3µs. They have an operating-supply voltage from 2.5V to 5.5V when operating from a single supply and from ±1.25V to ±2.75V when operating from dual power supplies. Their common-mode input voltage range extends from the negative supply to within 1.1V of the positive supply. Internal hysteresis ensures clean output switching, even with slow-moving input signals.

## Applications Information

### Adding Hysteresis

Hysteresis extends the comparator's noise margin by increasing the upper threshold and decreasing the lower threshold. A voltage-divider from the comparator's output sets the trip voltage. Therefore, the trip voltage is related to the output voltage.

These comparators have 4mV internal hysteresis. Additional hysteresis can be generated with two resistors, using positive feedback (Figure 1). Use the following procedure to calculate resistor values:

1) Find the trip points of the comparator using these formulas:

$$V_{TH} = V_{REF} + ((V_{DD} - V_{REF})R2) / (R1 + R2)$$

$$V_{TL} = V_{REF}(1 - (R2 / (R1 + R2))$$

where $V_{TH}$ is the threshold voltage at which the comparator switches its output from high to low as $V_{IN}$ rises above the trip point. $V_{TL}$ is the threshold voltage at which the comparator switches its output from low to high as $V_{IN}$ drops below the trip point.

# Micropower, Ultra-Small, Single/Dual/Quad, Single-Supply Comparators

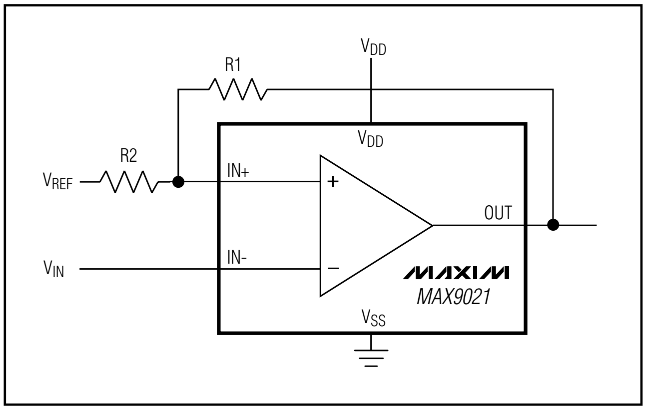



*Figure 1. Additional Hysteresis*

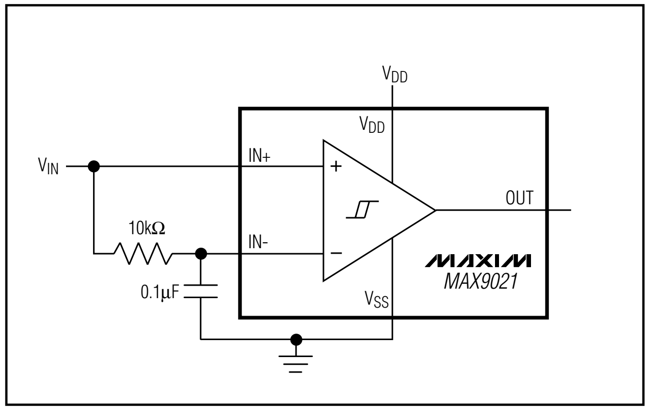



*Figure 2. Time Averaging of the Input Signal for Data Recovery*

2) The hysteresis band will be:

$$V_{HYS} = V_{TH} - V_{TL} = V_{DD}(R2 / (R1 + R2))$$

3) In this example, let $V_{DD}$ = 5V and $V_{REF}$ = 2.5V.

$$V_{TH} = 2.5V + 2.5V(R2 / (R1 + R2))$$

and

$$V_{TL} = 2.5V[(1 - (R2 / (R1 + R2))]$$

4) Select R2. In this example, we will choose 1kΩ.
5) Select $V_{HYS}$. In this example, we will choose 50mV.
6) Solve for R1.

$$V_{HYS} = V_{DD}(R2 / (R1 + R2))$$
$$0.050V = 5(1000\Omega/(R1 + 1000\Omega))\ V$$

where R1 ≈ 100kΩ, $V_{TH}$ = 2.525V, and $V_{TL}$ = 2.475V.

The above-described design procedure assumes rail-to-rail output swing. If the output is significantly loaded, the results should be corrected.

### Board Layout and Bypassing

Use 100nF bypass as a starting point. Minimize signal trace lengths to reduce stray capacitance. Minimize the capacitive coupling between IN- and OUT. For slow-moving input signals (rise time > 1ms), use a 1nF capacitor between IN+ and IN-.

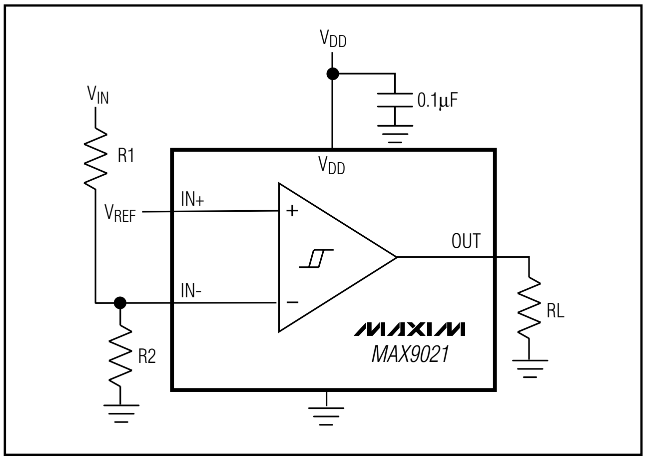
### Biasing for Data Recovery

Digital data is often embedded into a bandwidth and amplitude-limited analog path. Recovering the data can be difficult. Figure 2 compares the input signal to a time-averaged version of itself. This self-biases the threshold to the average input voltage for optimal noise margin. Even severe phase distortion is eliminated from the digital output signal. Be sure to choose R1 and C1 so that:

$$f_{CAR} >> 1 / (2\pi R1C1)$$

where $f_{CAR}$ is the fundamental carrier frequency of the digital data stream.

## Typical Application Circuit

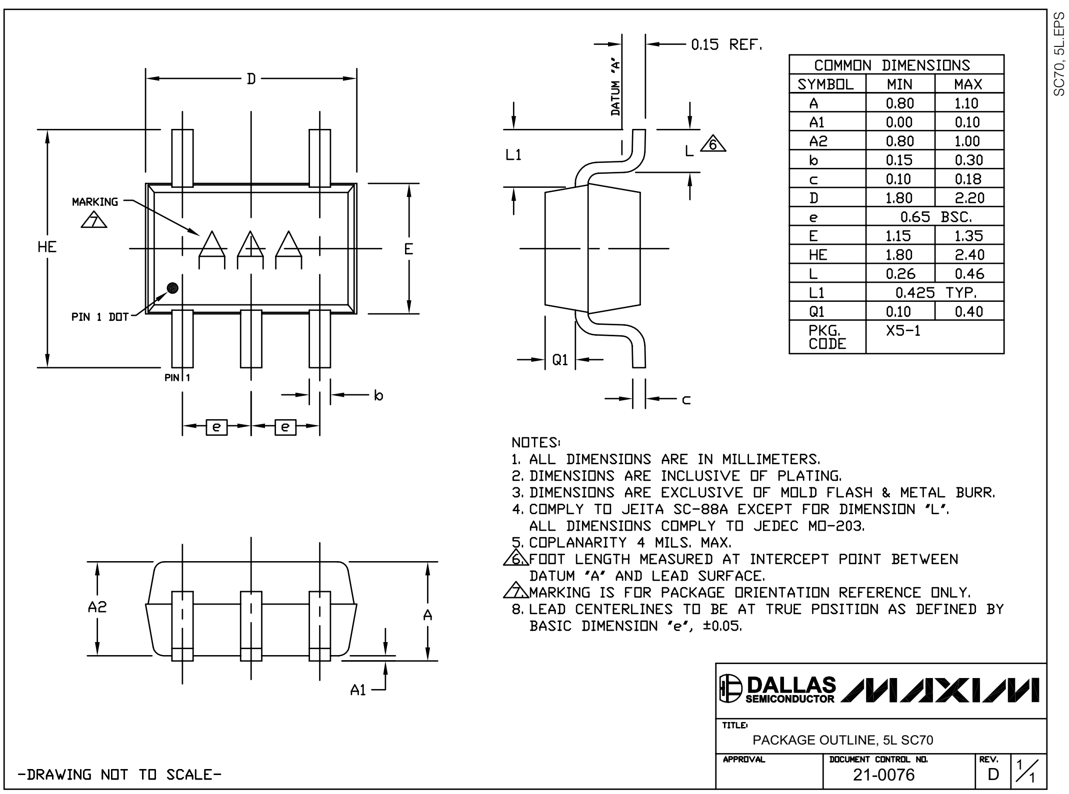



## Chip Information

MAX9021 TRANSISTOR COUNT: 106
MAX9022 TRANSISTOR COUNT: 212
MAX9024 TRANSISTOR COUNT: 424

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



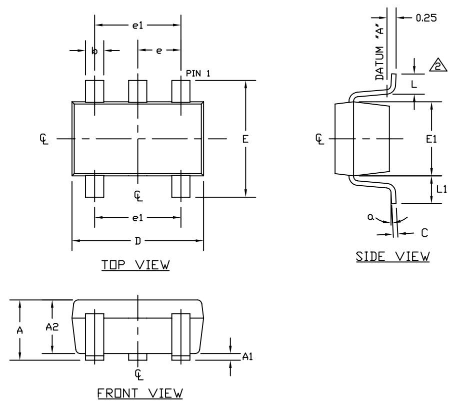

| COMMON DIMENSIONS | | |
|---|---|---|
| SYMBOL | MIN | MAX |
| A | 0.80 | 1.10 |
| A1 | 0.00 | 0.10 |
| A2 | 0.80 | 1.00 |
| b | 0.15 | 0.30 |
| c | 0.10 | 0.18 |
| D | 1.80 | 2.20 |
| e | 0.65 BSC. | |
| E | 1.15 | 1.35 |
| HE | 1.80 | 2.40 |
| L | 0.26 | 0.46 |
| L1 | 0.425 TYP. | |
| Q1 | 0.10 | 0.40 |
| PKG. CODE | X5-1 | |

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COMPLY TO JEITA SC-88A EXCEPT FOR DIMENSION 'L'. ALL DIMENSIONS COMPLY TO JEDEC MO-203.
5. COPLANARITY 4 MILS. MAX.
6. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM 'A' AND LEAD SURFACE.
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
8. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.

# Micropower, Ultra-Small, Single/Dual/Quad, Single-Supply Comparators

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

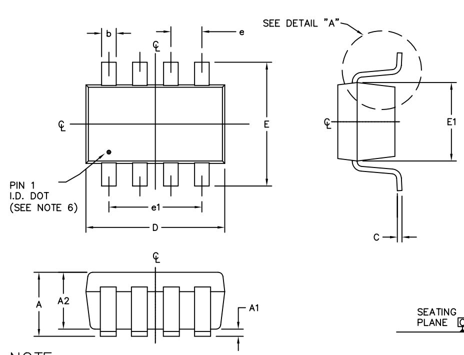



| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.90 | 1.25 | 1.45 |
| A1 | 0.00 | 0.05 | 0.15 |
| A2 | 0.90 | 1.10 | 1.30 |
| b | 0.35 | 0.40 | 0.50 |
| C | 0.08 | 0.15 | 0.20 |
| D | 2.80 | 2.90 | 3.00 |
| E | 2.60 | 2.80 | 3.00 |
| E1 | 1.50 | 1.625 | 1.75 |
| L | 0.35 | 0.45 | 0.60 |
| L1 | 0.60 REF | | |
| e | 0.95 BSC. | | |
| e1 | 1.90 BSC. | | |
| α | 0° | 2.5° | 8° |
| PKG CODES: U5-1, U5-2 | | | |

SOT-23 5L .EPS

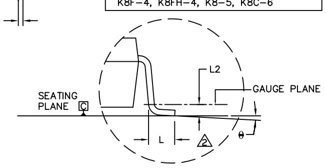
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. MEETS JEDEC MO178, VARIATION AA.
6. LEADS TO BE COPLANAR WITHIN 0.10 mm.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, SOT-23, 5L
APPROVAL | DOCUMENT CONTROL NO. 21-0057 | REV. F | 1/1




| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.90 | 1.25 | 1.45 |
| A1 | 0.00 | 0.06 | 0.15 |
| A2 | 0.90 | 1.10 | 1.30 |
| b | 0.22 | 0.30 | 0.38 |
| C | 0.08 | 0.15 | 0.22 |
| D | 2.80 | 2.90 | 3.00 |
| E | 2.60 | 2.80 | 3.00 |
| E1 | 1.50 | 1.625 | 1.75 |
| L | 0.30 | 0.45 | 0.60 |
| L2 | 0.25 BSC. | | |
| e | 0.65 BSC. | | |
| e1 | 1.95 REF. | | |
| θ | 0° | 3° | 8° |
| PKG CODES: K8-1, K8-2, K8S-3, K8F-4, K8FH-4, K8-5, K8C-6 | | | |

SOT23, 8L .EPS




DETAIL "A"

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178 VARIATION BA.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, SOT-23, 8L BODY
APPROVAL | DOCUMENT CONTROL NO. 21-0078 | REV. F | 1/1

## Revision History

Pages changed at Rev 2: 1, 2, 6, 7, 8

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