Absolute Maximum Ratings

IN to GND (V_{EN} = 0V).....-0.3V to +26V
NDRV, AUXDRV to GND.....-0.3V to (V_{IN} + 0.3V)
RT, DT, FFB, COMP, SS, DCLMP, DITHER/SYNC to GND.....-0.3V to +6V
FB to GND (MAX5974A/MAX5974B only).....-6V to +6V
FB to GND (MAX5974C/MAX5974D only).....-0.3V to +6V
CS, CSSC to GND.....-0.8V to +6V
PGND to GND.....-0.3V to +0.3V

Maximum Input/Output Current (continuous)
EN.....1mA
NDRV, AUXDRV (pulsed for less than 100ns).....±1A
Continuous Power Dissipation (T_A = +70°C)
16-Pin TQFN (derate 20.8mW/°C above +70°C).....1666mW
Operating Temperature Range..... -40°C to +125°C
Maximum Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 16 TQFN	
Package Code	T1633+4
Outline Number	21-0136
Land Pattern Number	90-0031
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	48°C/W
Junction to Case (θ_{JC})	7°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 12V (for MAX5974A/MAX5974C, bring V_{IN} up to 17V for startup), V_{CS} = V_{CSSC} = $V_{DITHER/SYNC}$ = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}, V_{EN} = +2V, NDRV = AUXDRV = SS = COMP = unconnected, R_{RT} = 34.8kΩ, R_{DT} = 25kΩ, C_{IN} = 1µF, T_A = -40°C to +85°C (MAX5974BETE+, MAX5974CETE+, MAX5974DETE+), T_A = -40°C to +105°C (MAX5974AETE+), T_A = -40°C to +125°C (MAX5974AATE+, MAX5974BATE+, MAX5974CATE+, MAX5974DATE+), unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
UNDERVOLTAGE LOCKOUT/STARTUP (IN)								
Bootstrap UVLO Wakeup Level	V_{INUVR}	V_{IN} rising	MAX5974A/C		15.4	16	16.5	V
			MAX5974B/D	-40°C to +85°C	8	8.4	8.85	
				-40°C to +125°C	7.95	8.4	8.85	
Bootstrap UVLO Shutdown Level	V_{INUVF}	V_{IN} falling		-40°C to +85°C	6.65	7	7.35	V
				-40°C to +125°C	6.6	7	7.35	
IN Clamp Voltage	V_{IN_CLAMP}	I_{IN} = 2mA (sinking)			17	18.5	20	V
IN Supply Current in Undervoltage Lockout	I_{START}	V_{IN} = +15V (for MAX5974A/C); V_{IN} = +7.5V (for MAX5974B/D), when in bootstrap UVLO		-40°C to +85°C		100	150	µA
				-40°C to +125°C		100	250	
IN Supply Current After Startup	I_C	V_{IN} = +12V		-40°C to +85°C		1.8	3	mA
				-40°C to +125°C		1.8	4	
ENABLE (EN)								
Enable Threshold	V_{ENR}	V_{EN} rising		-40°C to +85°C	1.17	1.215	1.26	V
				-40°C to +125°C	1.17	1.2155	1.2655	
	V_{ENF}	V_{EN} falling		-40°C to +85°C	1.09	1.14	1.19	
				-40°C to +125°C	1.085	1.14	1.19	
Input Current	I_{EN}	-40°C to +85°C					1	µA
		-40°C to +105°C					1.5	
OSCILLATOR (RT)								
RT Bias Voltage	V_{RT}					1.23		V
NDRV Switching Frequency Range	f_{SW}				100		600	kHz
NDRV Switching Frequency Accuracy		-40°C to +85°C			-8		+8	%
		-40°C to +105°C			-11		+11	
		-40°C to +125°C			-13		+13	
Maximum Duty Cycle	D_{MAX}	f_{SW} = 250kHz		-40°C to +85°C	79	80	82	%
				-40°C to +125°C	79	80	83	
SYNCHRONIZATION (SYNC)								
Synchronization Logic-High Input	$V_{IH-SYNC}$				2.91			V
Synchronization Pulse Width						50		ns
Synchronization Frequency Range	f_{SYNCIN}				1.1 x f_{SW}		2 x f_{SW}	kHz

Electrical Characteristics (continued)

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Duty Cycle During Synchronization					D_{MAX} x f_{SYNC}/ f_{SW}		%
DITHERING RAMP GENERATOR (DITHER)							
Charging Current		V_{DITHER} = 0V	-40°C to +85°C	45	50	55	µA
			-40°C to +125°C	44.5	50	55.5	
Discharging Current		V_{DITHER} = 2.2V	-40°C to +85°C	43	50	57	µA
			-40°C to +125°C	42	50	58	
Ramp's High Trip Point					2		V
Ramp's Low Trip Point					0.4		V
SOFT-START AND RESTART (SS)							
Charging Current	I_{SS-CH}	-40°C to +85°C		9.5	10	10.5	µA
		-40°C to +125°C		9	10	11	
Discharging Current	I_{SS-D}	V_{SS} = 2V, normal shutdown		0.65	1.34	2	mA
	I_{SS-DH}	(V_{EN} < V_{ENF} or V_{IN} < V_{INUVF}), V_{SS} = 2V, hiccup mode discharge for t_{RSTRT} (Note 2)		1.6	2	2.4	µA
Discharge Threshold to Disable Hiccup and Restart	V_{SS-DTH}				0.15		V
Minimum Restart Time During Hiccup Mode	$t_{RSTRT-MIN}$				1024		Clock Cycles
Normal Operating High Voltage	V_{SS-HI}				5		V
Duty-Cycle Control Range	$V_{SS-DMAX}$	D_{MAX} (typ) = ($V_{SS-DMAX}$/2.43V)		0		2	V
DUTY-CYCLE CLAMP (DCLMP)							
DCLMP Input Current	I_{DCLMP}	V_{DCLMP} = 0 to 5V		-100	0	+100	nA
Duty-Cycle Control Range	$V_{DCLMP-R}$		V_{DCLMP} = 0.5V	73	75.4	77.5	%
		D_{MAX} (typ) = 1 - (V_{DCLMP}/2.43V)	V_{DCLMP} = 1V	54	56	58	
			V_{DCLMP} = 2V	14.7	16.5	18.3	
NDRV DRIVER							
Pulldown Impedance	R_{NDRV-N}	I_{NDRV} (sinking) = 100mA	-40°C to +85°C		1.9	3.4	Ω
			-40°C to +125°C		1.9	3.5	
Pullup Impedance	R_{NDRV-P}	I_{NDRV} (sourcing) = 50mA			4.7	8.3	Ω
Peak Sink Current					1		A
Peak Source Current					0.65		A
Fall Time	t_{NDRV-F}	C_{NDRV} = 1nF			14		ns
Rise Time	t_{NDRV-R}	C_{NDRV} = 1nF			27		ns
AUXDRV DRIVER							
Pulldown Impedance	R_{AUX-N}	I_{AUXDRV} (sinking) = 50mA	-40°C to +85°C		4.3	7.7	Ω
			-40°C to +125°C		4.3	7.95	
Pullup Impedance	R_{AUX-P}	I_{AUXDRV} (sourcing) = 25mA			10.6	18.9	Ω

Electrical Characteristics (continued)

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Peak Sink Current					0.5		A
Peak Source Current					0.3		A
Fall Time	t_{AUX-F}	C_{AUXDRV} = 1nF			24		ns
Rise Time	t_{AUX-R}	C_{AUXDRV} = 1nF			45		ns
DEAD-TIME PROGRAMMING (DT)							
DT Bias Voltage	V_{DT}				1.215		V
NDRV to AUXDRV Delay (Dead Time)	t_{DT}	From NDRV falling to AUXDRV falling	R_{DT} = 10kΩ		40		ns
			R_{DT} = 100kΩ	300	350	410	
		From AUXDRV rising to NDRV rising	R_{DT} = 10kΩ		40		ns
			R_{DT} = 100kΩ	310	360	420	
CURRENT-LIMIT COMPARATOR (CS)							
Cycle-by-Cycle Peak Current-Limit Threshold	$V_{CS-PEAK}$			375	393	410	mV
Cycle-by-Cycle Reverse Current-Limit Threshold	V_{CS-REV}	Turns AUXDRV off for the remaining cycle if reverse current limit is exceeded	-40°C to +85°C	-118	-100	-88	mV
			-40°C to +105°C	-124	-100	-88	
Current-Sense Blanking Time for Reverse Current Limit	$t_{CS-BLANK-REV}$	From AUXDRV falling edge			115		ns
Number of Consecutive Peak Current-Limit Events to Hiccup	N_{HICCUP}				8		Events
Current-Sense Leading-Edge Blanking Time	$t_{CS-BLANK}$	From NDRV rising edge			115		ns
Propagation Delay from Comparator Input to NDRV	t_{PDCS}	From CS rising (10mV overdrive) to NDRV falling (excluding leading-edge blanking)			35		ns
Minimum On-Time	t_{ON-MIN}			100	150	200	ns
SLOPE COMPENSATION (CSSC)							
Slope Compensation Current Ramp Height		Current ramp's peak added to CSSC input per switching cycle	-40°C to +85°C	47	52	58	µA
			-40°C to +125°C	46.5	52	59.5	
PWM COMPARATOR							
Comparator Offset Voltage	V_{PWM-OS}	V_{COMP} - V_{CSSC}	-40°C to +85°C	1.35	1.7	2	V
			-40°C to +125°C	1.34	1.7	2	
Current-Sense Gain	A_{CS-PWM}	$\Delta V_{COMP}/\Delta V_{CSSC}$ (Note 3)		3.1	3.33	3.6	V/V
Current-Sense Leading-Edge Blanking Time	$t_{CSSC-BLANK}$	From NDRV rising edge			115		ns

Electrical Characteristics (continued)

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Comparator Propagation Delay	t_{PWM}	Change in V_{CSSC} = 10mV (including internal leading-edge blanking)			150		ns
ERROR AMPLIFIER							
FB Reference Voltage	V_{REF}	V_{FB} when I_{COMP} = 0, V_{COMP} = 2.5V	MAX5974A/B	1.5	1.52	1.54	V
			MAX5974CETE/DETE	1.202	1.215	1.227	
			MAX5974CATE/DATE (Note 4)	1.202	1.215	1.230	
FB Input Bias Current	I_{FB}	V_{FB} = 0 to 1.75V	MAX5974A/B	-250		+250	nA
			MAX5974CETE/DETE	-500		+100	
			MAX5974CATE/DATE (Note 4)	-1000		+100	
Voltage Gain	A_{EAMP}				80		dB
Transconductance	g_M		MAX5974A/B	1.8	2.55	3.2	mS
			MAX5974C/D	1.8	2.66	3.5	
Transconductance Bandwidth	BW	Open loop (typical gain = 1) -3dB frequency	MAX5974A/B		2		MHz
			MAX5974C/D		30		
Source Current		V_{FB} = 1V, V_{COMP} = 2.5V		300	375	455	µA
Sink Current		V_{FB} = 1.75V, V_{COMP} = 1V		300	375	455	µA
FREQUENCY FOLDBACK (FFB)							
V_{CSAVG}-to-FFB Comparator Gain					10		V/V
FFB Bias Current	I_{FFB}	V_{FFB} = 0V, V_{CS} = 0V (not in FFB mode)	-40°C to +85°C	26	30	33	µA
			-40°C to +125°C	26	30	33.5	
NDRV Switching Frequency During Foldback	f_{SW-FB}				f_{SW}/2		kHz
THERMAL SHUTDOWN							
Thermal-Shutdown Threshold	T_{SD}	Temperature rising			165		°C
Thermal-Shutdown Hysteresis		Temperature falling			10		°C

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.
Note 2: See the *Output Short-Circuit Protection with Hiccup Mode* section.
Note 3: The parameter is measured at the trip point of latch with V_{FB} = 0V. Gain is defined as $\Delta V_{COMP}/\Delta V_{CSSC}$ for 0.15V < ΔV_{CSSC} < 0.25V.
Note 4: Operates over the -40°C to +125°C operating temperature range.

Typical Operating Characteristics

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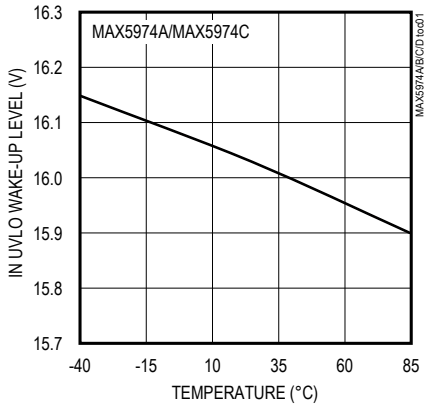
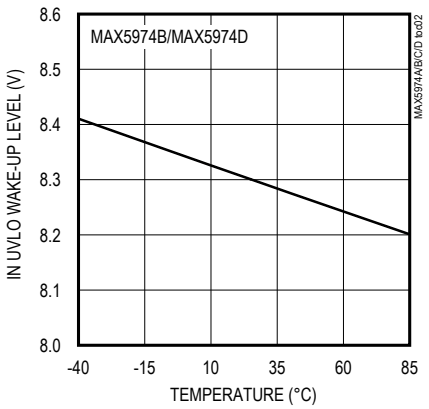
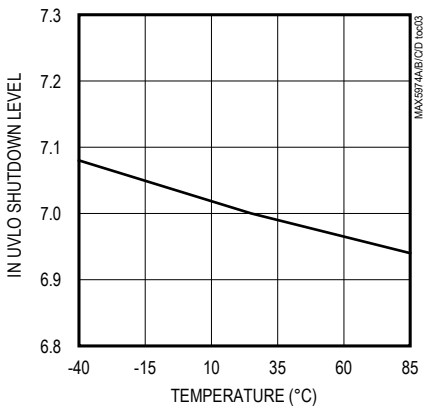
IN UVLO WAKE-UP LEVEL vs. TEMPERATURE



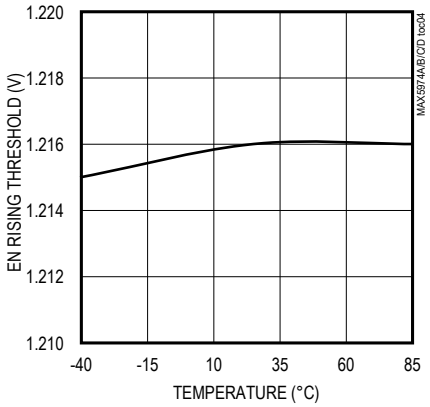
IN UVLO WAKE-UP LEVEL vs. TEMPERATURE



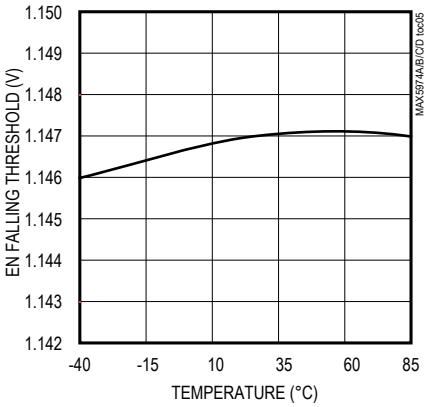
IN UVLO SHUTDOWN LEVEL vs. TEMPERATURE



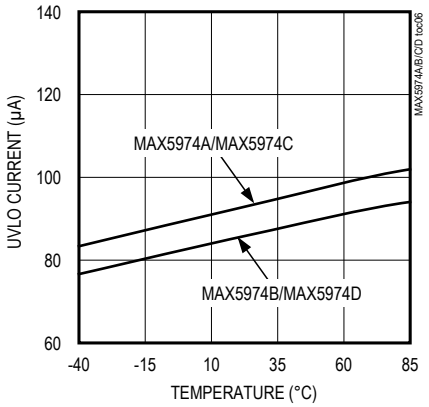
EN RISING THRESHOLD vs. TEMPERATURE



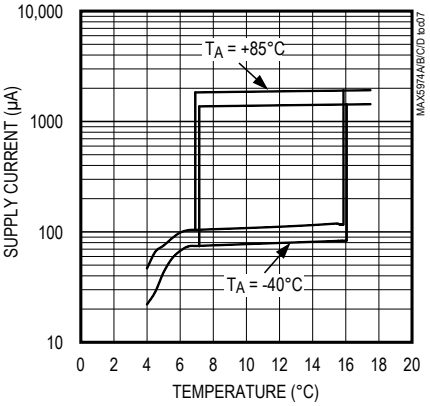
EN FALLING THRESHOLD vs. TEMEPRATURE



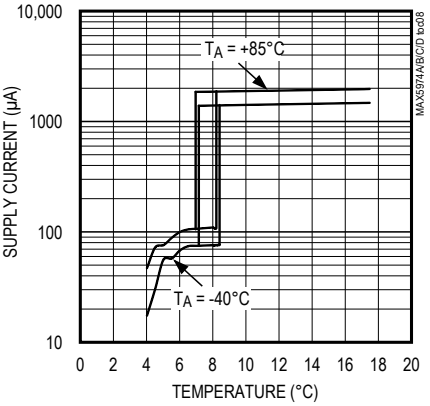
UVLO SHUTDOWN CURRENT vs. TEMPERATURE



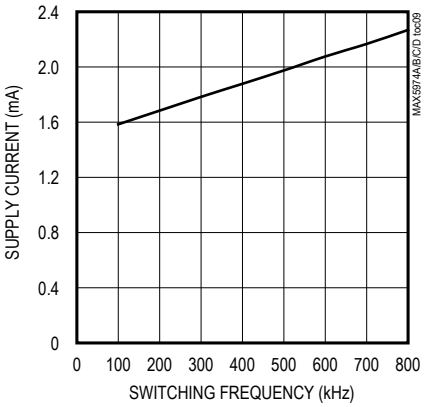
SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX5974A/MAX5974C)



SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX5974B/MAX5974D)



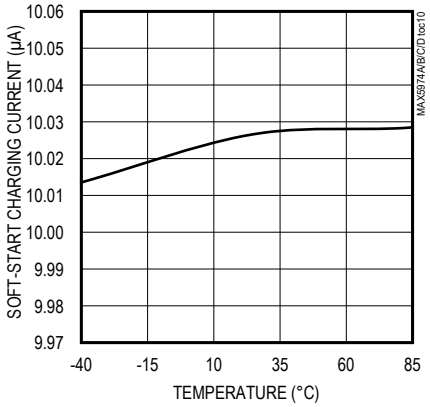
SUPPLY CURRENT vs. SWITCHING FREQUENCY



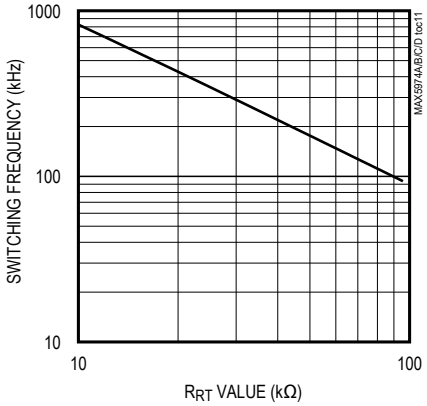
Typical Operating Characteristics (continued)

(V_{IN} = 12V (for MAX5974A/MAX5974C, bring V_{IN} up to 17V for startup), V_{CS} = V_{CSSC} = $V_{DITHER/SYNC}$ = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}, V_{EN} = 2V, NDRV = AUXDRV = SS = COMP = unconnected, R_{RT} = 34.8kΩ, R_{DT} = 25kΩ, unless otherwise noted.)

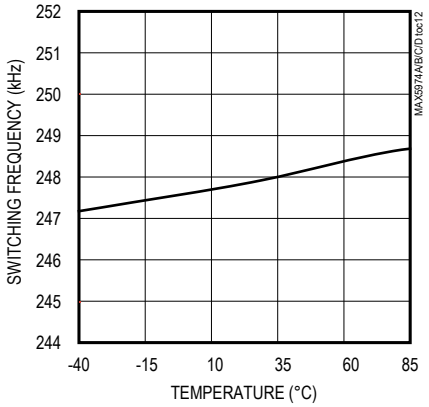
SOFT-START CHARGING CURRENT vs. TEMPERATURE



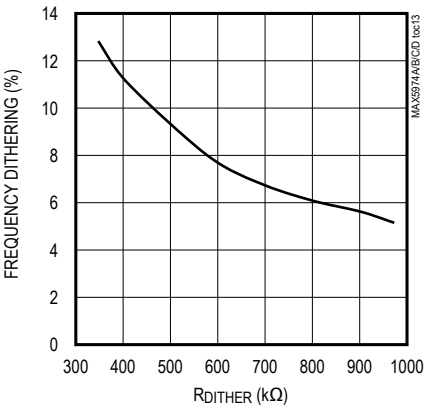
SWITCHING FREQUENCY vs. R_{RT} VALUE



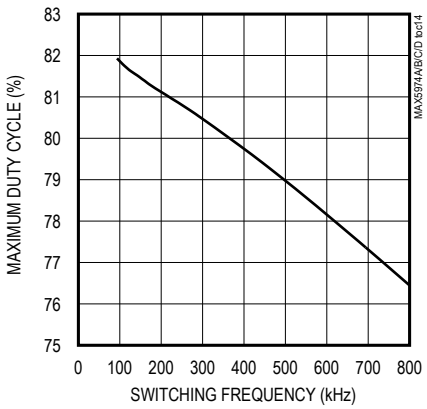
SWITCHING FREQUENCY vs. TEMPERATURE



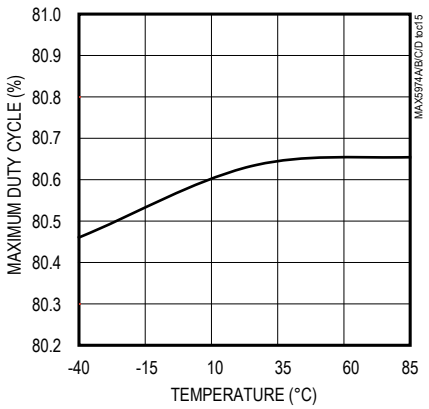
FREQUENCY DITHERING vs. R_{DITHER}



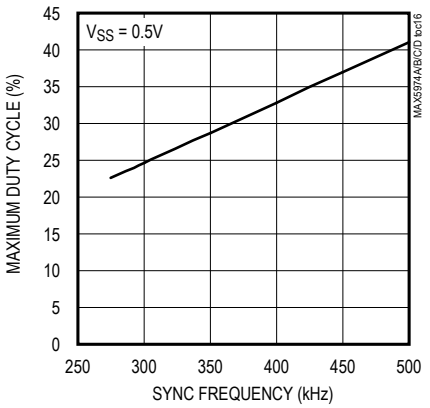
MAXIMUM DUTY CYCLE vs. SWITCHING FREQUENCY



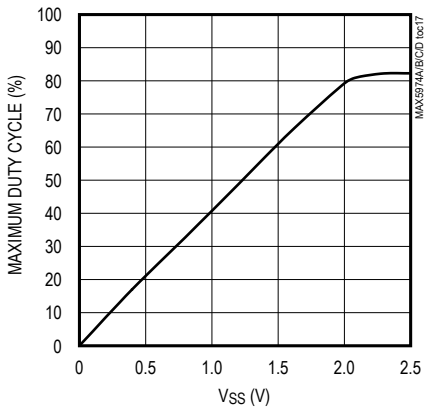
MAXIMUM DUTY CYCLE vs. TEMPERATURE



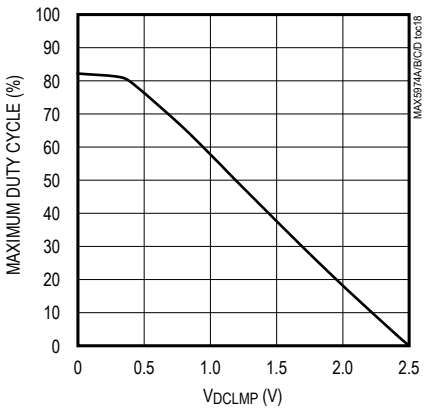
MAXIMUM DUTY CYCLE vs. SYNC FREQUENCY



MAXIMUM DUTY CYCLE vs. V_{SS}



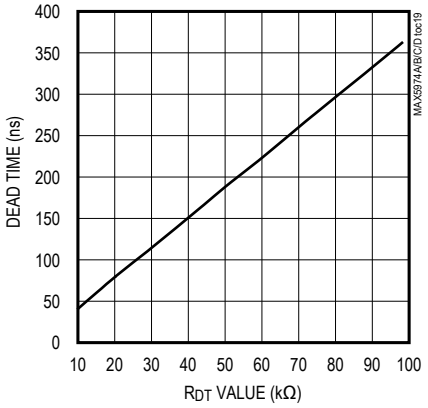
MAXIMUM DUTY CYCLE vs. V_{DCLMP}



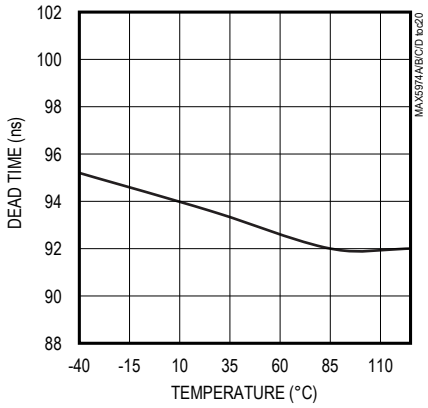
Typical Operating Characteristics (continued)

(V_{IN} = 12V (for MAX5974A/MAX5974C, bring V_{IN} up to 17V for startup), V_{CS} = V_{CSSC} = $V_{DITHER/SYNC}$ = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}, V_{EN} = 2V, NDRV = AUXDRV = SS = COMP = unconnected, R_{RT} = 34.8kΩ, R_{DT} = 25kΩ, unless otherwise noted.)

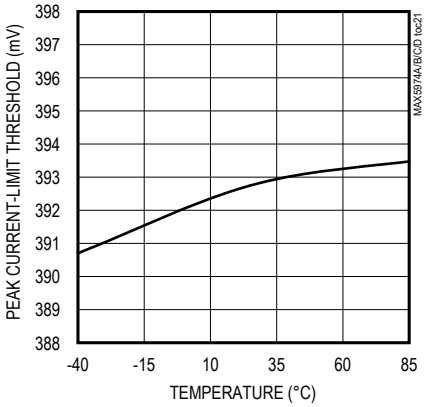
DEAD TIME vs. R_{DT} VALUE



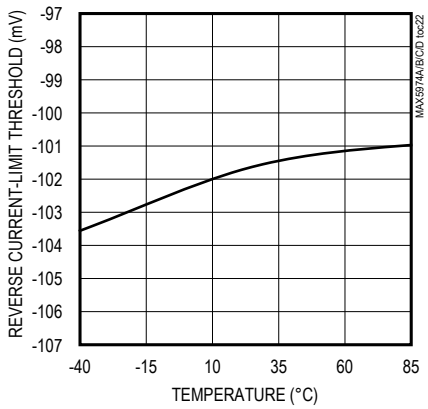
DEAD TIME vs. TEMPERATURE



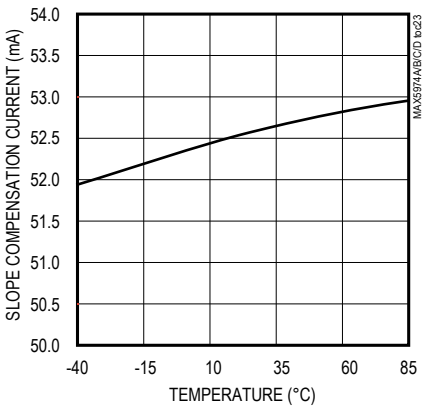
PEAK CURRENT-LIMIT THRESHOLD vs. TEMPERATURE



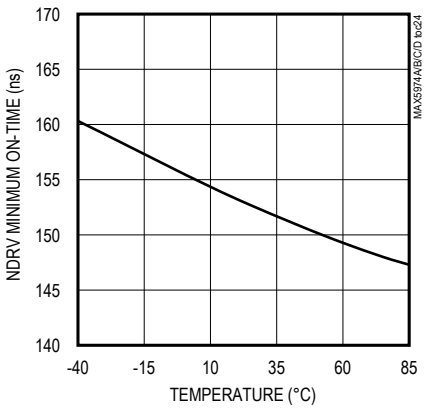
REVERSE CURRENT-LIMIT THRESHOLD vs. TEMPERATURE



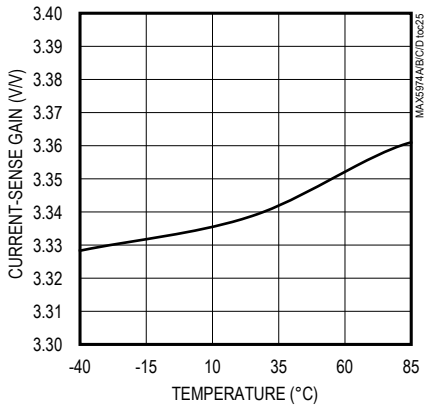
SLOPE COMPENSATION CURRENT vs. TEMPERATURE



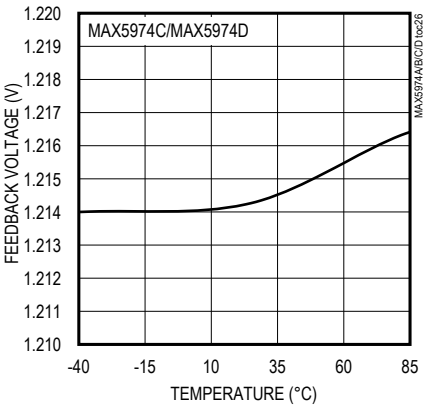
NDRV MINIMUM ON-TIME vs. TEMPERATURE



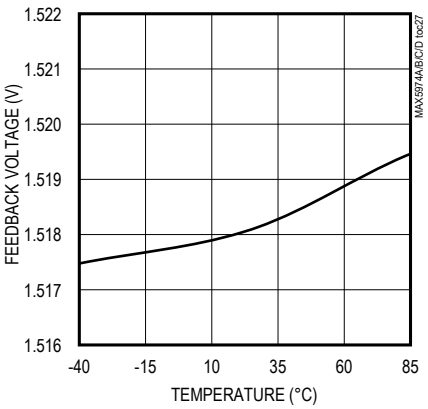
CURRENT-SENSE GAIN vs. TEMPERATURE



FEEDBACK VOLTAGE vs. TEMPERATURE



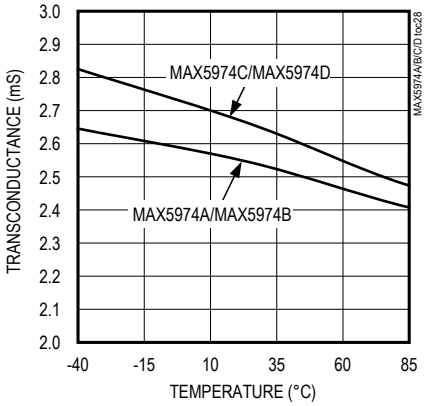
FEEDBACK VOLTAGE vs. TEMPERATURE



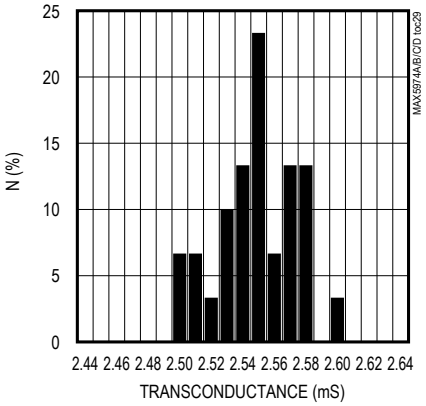
Typical Operating Characteristics (continued)

(V_{IN} = 12V (for MAX5974A/MAX5974C, bring V_{IN} up to 17V for startup), V_{CS} = V_{CSSC} = $V_{DITHER/SYNC}$ = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}, V_{EN} = 2V, NDRV = AUXDRV = SS = COMP = unconnected, R_{RT} = 34.8kΩ, R_{DT} = 25kΩ, unless otherwise noted.)

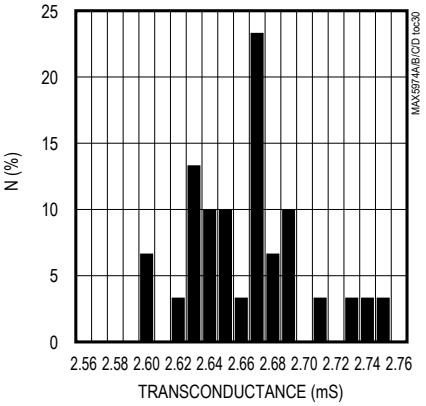
TRANSCONDUCTANCE vs. TEMPERATURE



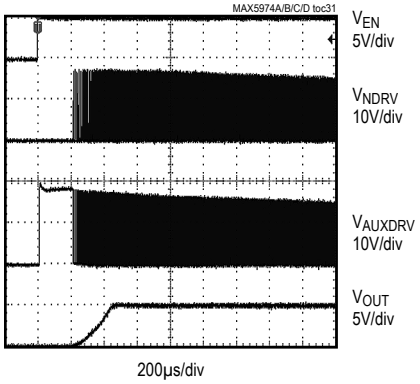
TRANSCONDUCTANCE HISTOGRAM (MAX5974A/MAX5974B)



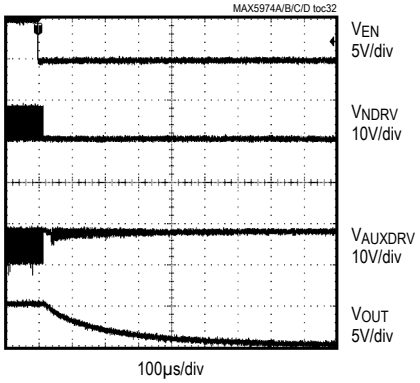
TRANSCONDUCTANCE HISTOGRAM (MAX5974C/MAX5974D)



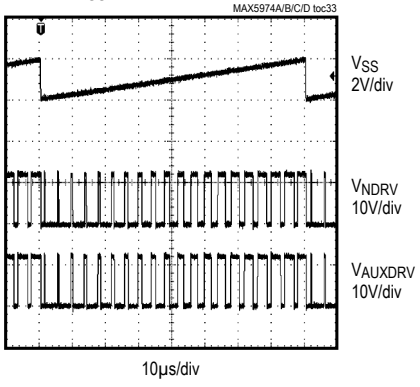
ENABLE RESPONSE



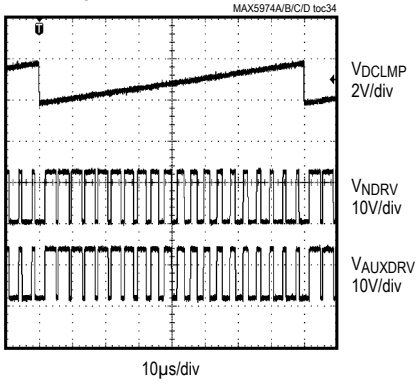
SHUTDOWN RESPONSE



V_{SS} RAMP RESPONSE



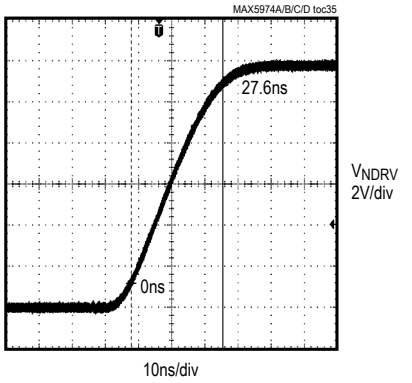
V_{DCLMP} RAMP RESPONSE



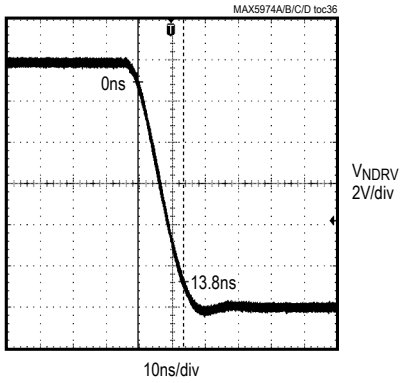
Typical Operating Characteristics (continued)

(V_{IN} = 12V (for MAX5974A/MAX5974C, bring V_{IN} up to 17V for startup), V_{CS} = V_{CSSC} = $V_{DITHER/SYNC}$ = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}, V_{EN} = 2V, NDRV = AUXDRV = SS = COMP = unconnected, R_{RT} = 34.8kΩ, R_{DT} = 25kΩ, unless otherwise noted.)

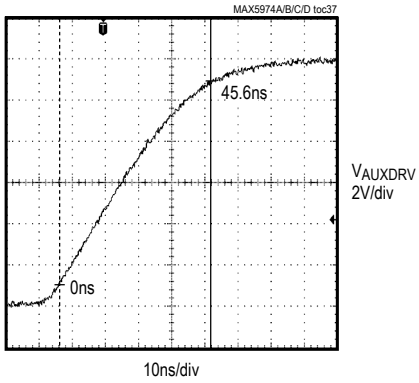
NDRV 10% TO 90% RISE TIME



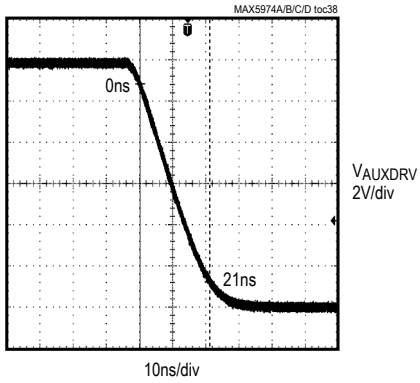
NDRV 90% TO 10% FALL TIME



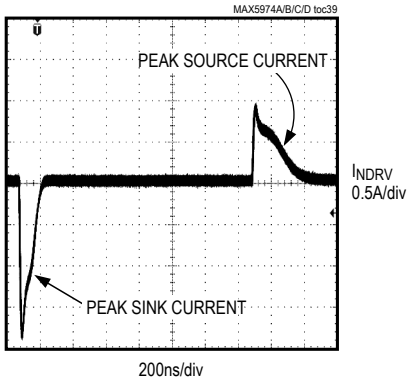
AUXDRV 10% TO 90% RISE TIME



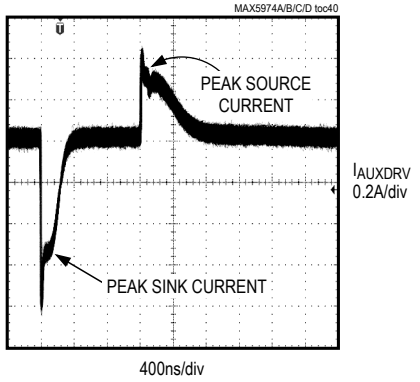
AUXDRV 90% TO 10% FALL TIME



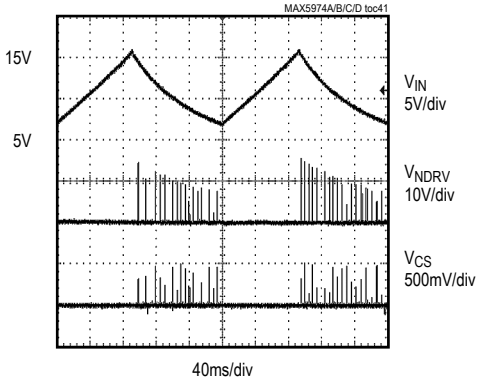
PEAK NDRV CURRENT



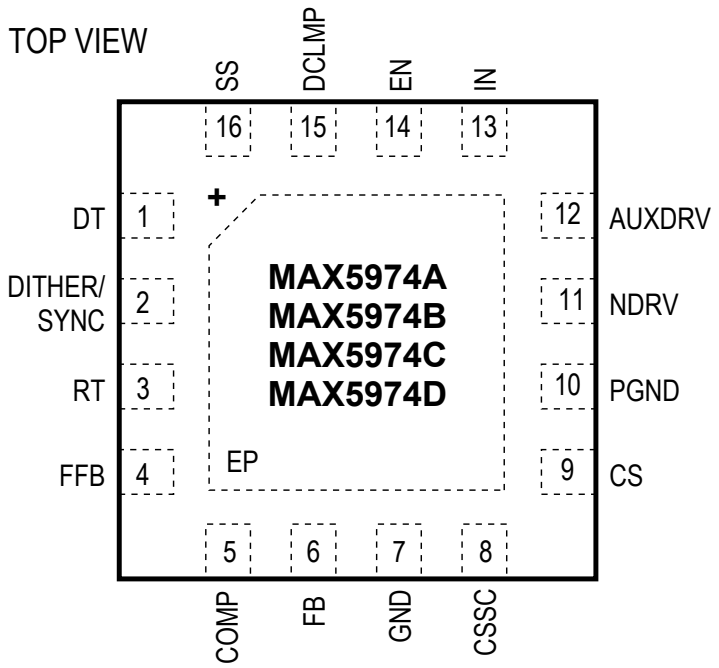
PEAK AUXDRV CURRENT



SHORT-CURRENT BEHAVIOR



Pin Configuration



16 TQFN
(3mm x 3mm)

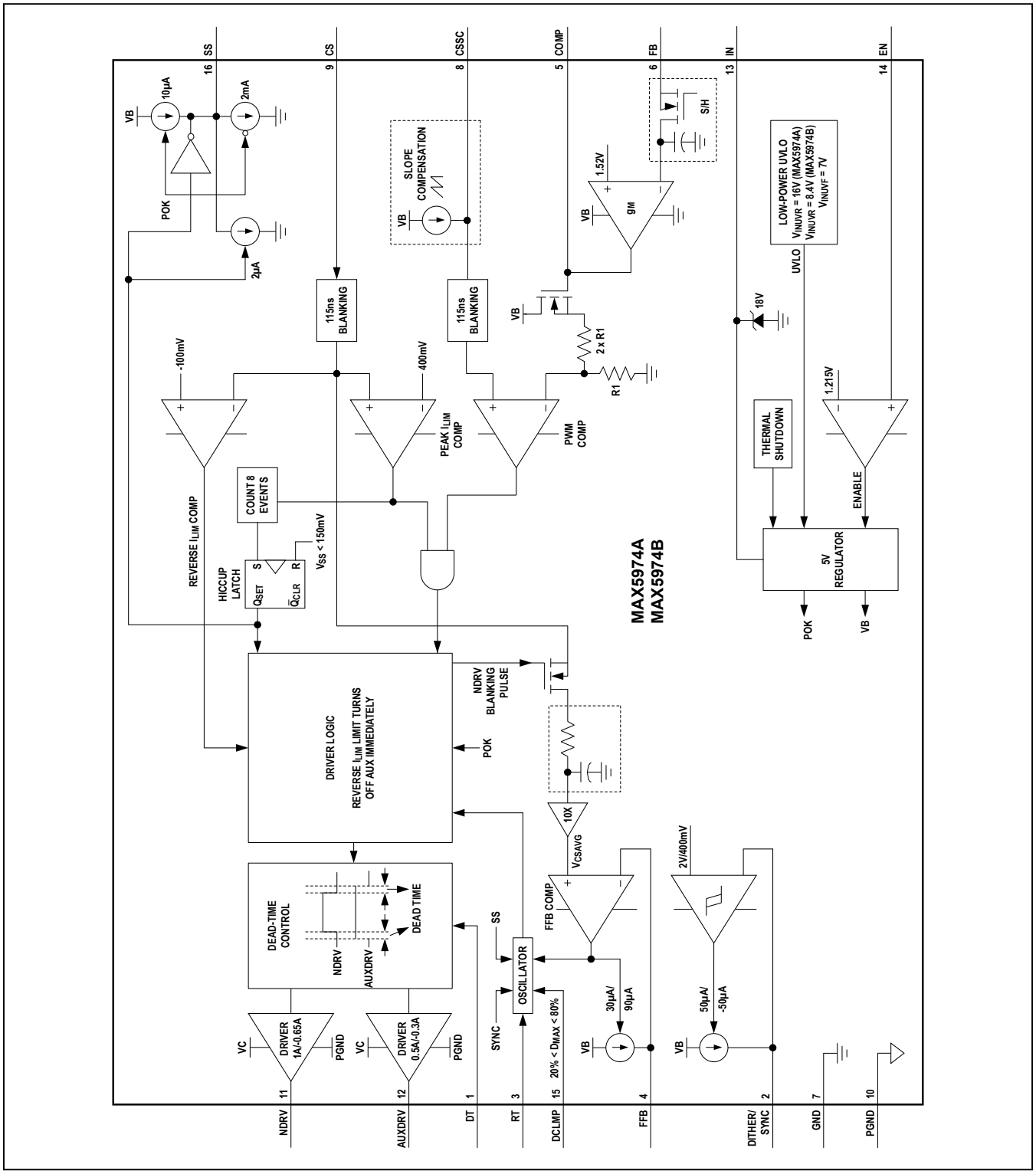
Pin Description

PIN	NAME	FUNCTION
1	DT	Dead-Time Programming Resistor Connection. Connect resistor R_{DT} from DT to GND to set the desired dead time between the NDRV and AUXDRV signals. See the *Dead Time* section to calculate the resistor value for a particular dead time.
2	DITHER/ SYNC	Frequency Dithering Programming or Synchronization Connection. For spread-spectrum frequency operation, connect a capacitor from DITHER to GND and a resistor from DITHER to RT. To synchronize the internal oscillator to the externally applied frequency, connect DITHER/SYNC to the synchronization pulse.
3	RT	Switching Frequency Programming Resistor Connection. Connect resistor R_{RT} from RT to GND to set the PWM switching frequency. See the *Oscillator/Switching Frequency* section to calculate the resistor value for the desired oscillator frequency.
4	FFB	Frequency Foldback Threshold Programming Input. Connect a resistor from FFB to GND to set the output average current threshold below which the converter folds back the switching frequency to 1/2 of its original value. Connect to GND to disable frequency foldback.
5	COMP	Transconductance Amplifier Output and PWM Comparator Input. COMP is level shifted down and connected to the inverting input of the PWM comparator. COMP is actively pulled low by the controller after shutdown.

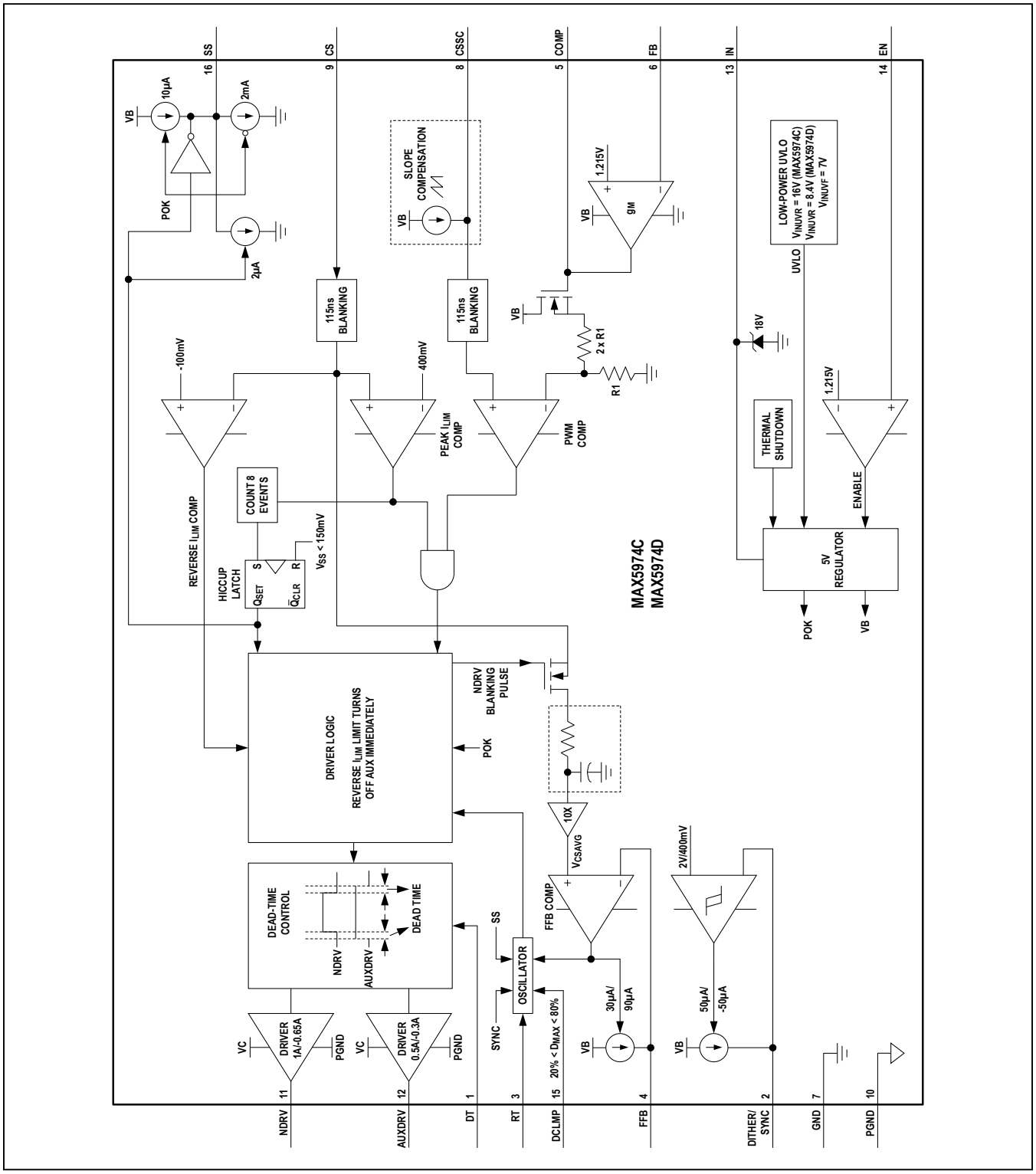
Pin Description (continued)

PIN	NAME	FUNCTION
6	FB	Transconductance Amplifier Inverting Input
7	GND	Signal Ground
8	CSSC	Current Sense with Slope Compensation Input. A resistor connected from CSSC to CS programs the amount of slope compensation. See the *Programmable Slope Compensation* section.
9	CS	Current-Sense Input. Current-sense connection for average current sense and cycle-by-cycle current limit. Peak current-limit trip voltage is 400mV and reverse current-limit trip voltage is -100mV.
10	PGND	Power Ground. PGND is the return path for gate-driver switching currents.
11	NDRV	Main Switch Gate-Driver Output
12	AUXDRV	pMOS Active Clamp Switch Gate-Driver Output. AUXDRV can also be used to drive a pulse transformer for synchronous flyback application.
13	IN	Converter Supply Input. IN has wide UVLO hysteresis, enabling the design of efficient power supplies. See the *Enable Input* section to determine if an external zener diode is required at IN.
14	EN	Enable Input. The gate drivers are disabled and the device is in a low-power UVLO mode when the voltage on EN is below V_{ENF}. When the voltage on EN is above V_{ENR}, the device checks for other enable conditions. See the *Enable Input* section for more information about interfacing to EN.
15	DCLMP	Feed-Forward Maximum Duty-Cycle Clamp Programming Input. Connect a resistive divider between the input supply voltage DCLMP and GND. The voltage at DCLMP sets the maximum duty cycle (D_{MAX}) of the converter inversely proportional to the input supply voltage, so that the MOSFET remains protected during line transients.
16	SS	Soft-Start Programming Capacitor Connection. Connect a capacitor from SS to GND to program the soft-start period. This capacitor also determines hiccup mode current-limit restart time. A resistor from SS to GND can also be used to set the D_{MAX} below 75%.
—	EP	Exposed Pad. Internally connected to GND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

Block Diagrams



Block Diagrams (continued)



Detailed Description

The MAX5974A/MAX5974B/MAX5974C/MAX5974D are optimized for controlling a 25W to 50W active-clamped, self-driven synchronous rectification forward converter in continuous-conduction mode. The main switch gate driver (NDRV) and the active-clamped switch driver (AUXDRV) are sized to optimize efficiency for 25W design. The features-rich devices are ideal for PoE IEEE 802.3af/at-powered devices.

The MAX5974A/MAX5974C offer a 16V bootstrap UVLO wake-up level with a 9V wide hysteresis. The low startup and operating currents allow the use of a smaller storage capacitor at the input without compromising startup and hold times. The MAX5974A/MAX5974C are well-suited for universal input (rectified 85V AC to 265V AC) or telecom (-36V DC to -72V DC) power supplies.

The MAX5974B/MAX5974D have a UVLO rising threshold of 8.4V and can accommodate for low-input voltage (12V DC to 24V DC) power sources such as wall adapters.

Power supplies designed with the MAX5974A/MAX5974C use a high-value startup resistor, R_{IN}, that charges a reservoir capacitor, C_{IN} (see the *Typical Application Circuits*). During this initial period, while the voltage is less than the internal bootstrap UVLO threshold, the device typically consumes only 100µA of quiescent current. This low startup current and the large bootstrap UVLO hysteresis help to minimize the power dissipation across R_{IN} even at the high end of the universal AC input voltage (265V AC).

Feed-forward maximum duty-cycle clamping detects changes in line conditions and adjusts the maximum duty cycle accordingly to eliminate the clamp voltage's (i.e., the main power FET's drain voltage) dependence on the input voltage.

For EMI-sensitive applications, the programmable frequency dithering feature allows up to ±10% variation in the switching frequency. This spread-spectrum modulation technique spreads the energy of switching harmonics over a wider band while reducing their peaks, helping to meet stringent EMI goals.

The devices include a cycle-by-cycle current limit that turns off the main and AUX drivers whenever the internally set threshold of 400mV is exceeded. Eight consecutive occurrences of current-limit events trigger hiccup mode, which protects external components by halting switching for a period of time (t_{RSTRT}) and allowing the overload current to dissipate in the load and body diode of the synchronous rectifier before soft-start is reattempted.

The reverse current-limit feature of the devices turns the AUX driver off for the remaining off period when V_{CS} exceeds the -100mV threshold. This protects the transformer core from saturation due to excess reverse current under some extreme transient conditions.

Current-Mode Control Loop

The advantages of current-mode control over voltage-mode control are twofold. First, there is the feed-forward characteristic brought on by the controller's ability to adjust for variations in the input voltage on a cycle-by-cycle basis. Second, the stability requirements of the current-mode controller are reduced to that of a single-pole system, unlike the double pole in voltage-mode control.

The devices use a current-mode control loop where the scaled output of the error amplifier (COMP) is compared to a slope-compensated current-sense signal at CSSC.

Input Clamp

When the device is enabled, an internal 18V input clamp is active. During an overvoltage condition, the clamp prevents the voltage at the supply input IN from rising above 18.5V (typ).

When the device is disabled, the input clamp circuitry is also disabled.

Enable Input

The enable input is used to enable or disable the device. Driving EN low disables the device. Note that the internal 18V input clamp is also disabled when EN is low. Therefore, an external 18V zener diode is needed for certain operating conditions as described below.

UVLO on Power Source

The enable input has an accurate threshold of 1.26V (max). For applications that require a UVLO on the power source, connect a resistive divider from the power source to EN to GND as shown in Figure 1. A zener diode between IN and GND is required to prevent the NDRV and AUXDRV gate-drive voltages from exceeding 20V, the maximum allowed gate voltage of power FETs.

The external zener diode should clamp in the following range:

$$20V > V_Z > V_{UVLO(MAX)}$$

where V_Z is the zener voltage and $V_{UVLO(MAX)}$ is the maximum wakeup level (16.5V or 8.85V depending on the device version). An 18V zener diode is the best choice.

Design the resistive divider by first selecting the value of R_{EN1} to be on the order of 100kΩ. Then calculate R_{EN2} as follows:

$$V_{EN2} = R_{EN1} \times \frac{V_{EN(MAX)}}{V_{S(UVLO)} - V_{EN(MAX)}}$$

where $V_{EN(MAX)}$ is the maximum enable threshold voltage and is equal to 1.26V and $V_{S(UVLO)}$ is the desired UVLO threshold for the power source, below which the device is disabled.

The digital output connected to EN should be capable of withstanding more than the maximum supply voltage.

MCU Control of Enable Input

When using a microcontroller GPIO to control the enable input, an 18V zener diode is required on IN as shown in Figure 2.

High-Voltage Logic Control of Enable Input

In the case where EN is externally controlled by a high-voltage open-drain/collector output (e.g., PGOOD indicator of a powered device controller), connect IN to EN through a resistor R_{EN} and connect EN to an open-drain or open-collector output as shown in Figure 3. Select R_{EN} such that the voltage at IN, when EN is low, is less than 20V (i.e., the maximum gate voltage of the main and AUX FETs):

$$V_{S(MAX)} \times \frac{R_{EN}}{R_{EN} + R_{IN}} < 20V$$

where $V_{S(MAX)}$ is the maximum supply voltage. Obeying this relationship eliminates the need for an external zener diode.

The digital output connected to EN should be capable of withstanding more than 20V.

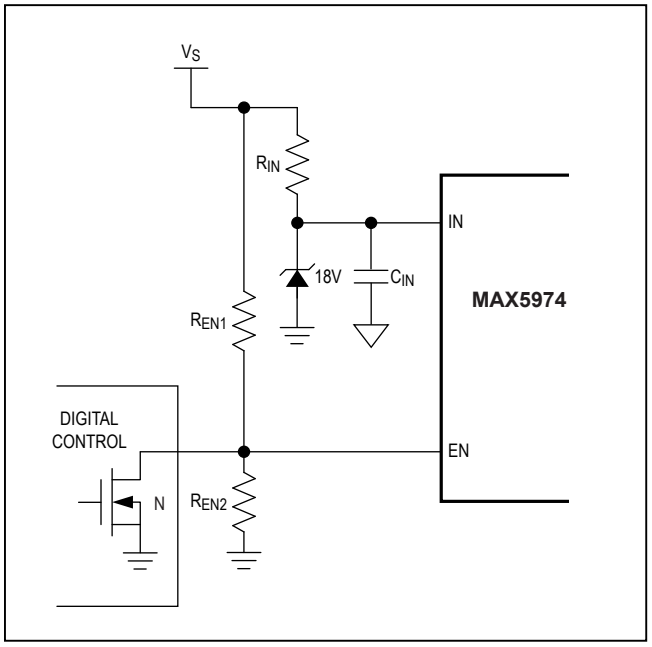


Figure 1. Programmable UVLO for the Power Source

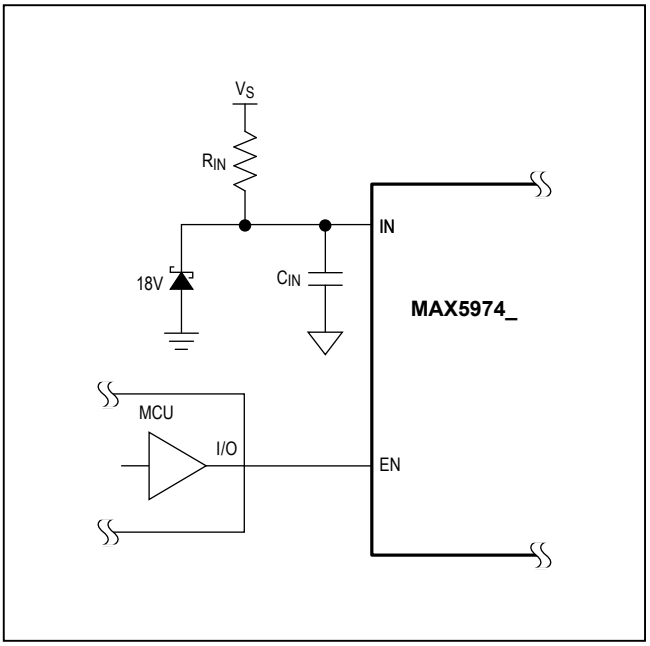


Figure 2. MCU Control of the Enable Input

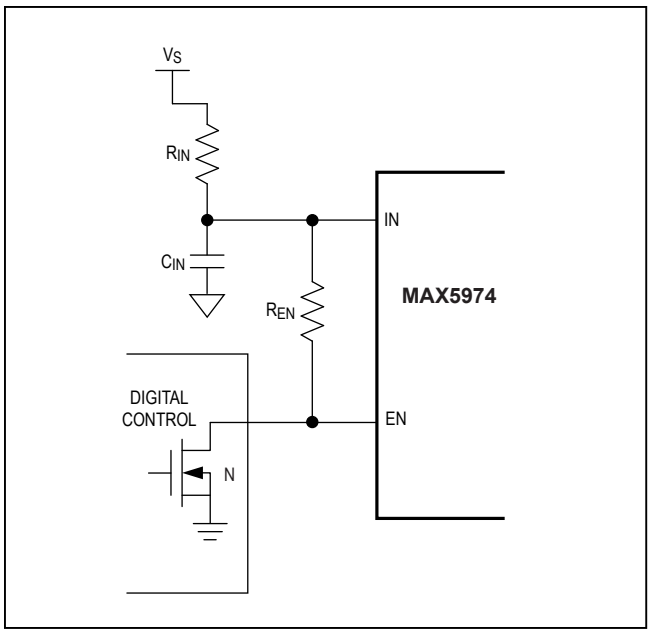


Figure 3. High-Voltage Logic Control of the Enable Input

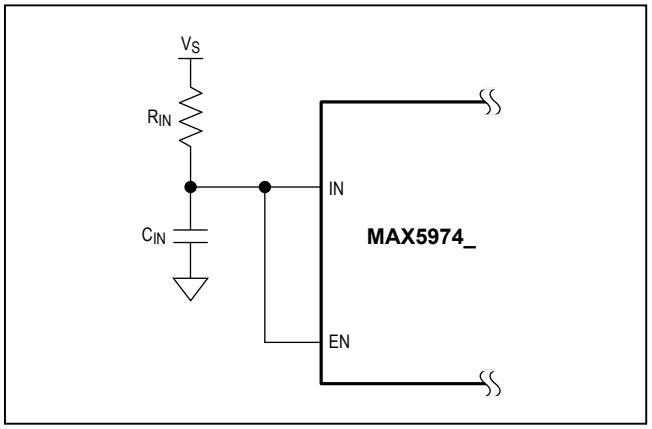


Figure 4. Always-On Operation

Always-On Operation

For always-on operation, connect EN to IN as shown in Figure 4. No external zener diode is needed for this configuration.

Bootstrap Undervoltage Lockout

The devices have an internal bootstrap UVLO that is very useful when designing high-voltage power supplies (see the *Block Diagrams*). This allows the device to bootstrap itself during initial power-up. The MAX5974A/MAX5974C soft-start when V_{IN} exceeds the bootstrap UVLO threshold of V_{INUVR} (16V typ).

Because the MAX5974B/MAX5974D are designed for use with low-voltage power sources such as wall adapters outputting 12V to 24V, they have a lower UVLO wake-up threshold of 8.4V.

Startup Operation

The device starts up when the voltage at IN exceeds 16V (MAX5974A/MAX5974C) or 8.4V (MAX5974B/MAX5974D) and the enable input voltage is greater than 1.26V.

During normal operation, the voltage at IN is normally derived from a tertiary winding of the transformer (MAX5974C/MAX5974D). However, at startup there is no energy being delivered through the transformer; hence, a special bootstrap sequence is required. In the *Typical Application Circuits*, C_{IN} charges through the startup resistor, R_{IN}, to an intermediate voltage. Only 100µA of the current supplied through R_{IN} is used by the ICs, the remaining input current charges C_{IN} until V_{IN} reaches the bootstrap UVLO wake-up level. Once V_{IN} exceeds this level, NDRV begins switching the n-channel MOSFET and transfers energy to the secondary and tertiary outputs. If the voltage on the tertiary output builds to higher than 7V (the bootstrap UVLO shutdown level), then startup has been accomplished and sustained operation commences. If V_{IN} drops below 7V before startup is complete, the device goes back to low-current UVLO. In this case, increase the value of C_{IN} in order to store enough energy to allow for the voltage at the tertiary winding to build up.

While the MAX5974A/MAX5974B derive their input voltage from the coupled inductor output during normal operation, the startup behavior is similar to that of the MAX5974C/MAX5974D.

Soft-Start

A capacitor from SS to GND, C_{SS}, programs the soft-start time. V_{SS} controls the oscillator duty cycle during startup to provide a slow and smooth increase of the duty cycle to its steady-state value. Calculate the value of C_{SS} as follows:

$$C_{SS} = \frac{I_{SS\text{-}CH} \times t_{SS}}{2V}$$

where $I_{SS\text{-}CH}$ (10µA typ) is the current charging C_{SS} during soft-start and t_{SS} is the programmed soft-start time.

A resistor can also be added from the SS pin to GND to clamp V_{SS} < 2V and, hence, program the maximum duty cycle to be less than 80% (see the *Duty-Cycle Clamping* section)

n-Channel MOSFET Gate Driver

The NDRV output drives an external n-channel MOSFET. NDRV can source/sink in excess of 650mA/1000mA peak current; therefore, select a MOSFET that yields acceptable conduction and switching losses. The external MOSFET used must be able to withstand the maximum clamp voltage.

p-Channel MOSFET Gate Driver

The AUXDRV output drives an external p-channel MOSFET with the aid of a level shifter. The level shifter consists of C_{AUX}, R_{AUX}, and D5 as shown in the *Typical Application Circuits*. When AUXDRV is high, C_{AUX} is recharged through D5. When AUXDRV is low, the gate of the p-channel MOSFET is pulled below the source by the voltage stored on C_{AUX}, turning on the pFET.

Add a zener diode between gate to source of the external n-channel and p-channel MOSFETs after the gate resistors to protect V_{GS} from rising above its absolute maximum rating during transient condition (see the *Typical Application Circuits*).

Dead Time

Dead time between the main and AUX output edges allow ZVS to occur, minimizing conduction losses and improving efficiency. The dead time (t_{DT}) is applied to both leading and trailing edges of the main and AUX outputs as shown in Figure 5. Connect a resistor between DT and GND to set t_{DT} to any value between 40ns and 400ns:

$$R_{DT} = \frac{10k\Omega}{40ns} \times t_{DT}$$

Oscillator/Switching Frequency

The ICs' switching frequency is programmable between 100kHz and 600kHz with a resistor R_{RT} connected between RT and GND. Use the following formula to determine the appropriate value of R_{RT} needed to generate the desired output-switching frequency (f_{SW}):

$$R_{RT} = \frac{8.7 \times 10^9}{f_{SW}}$$

where f_{SW} is the desired switching frequency.

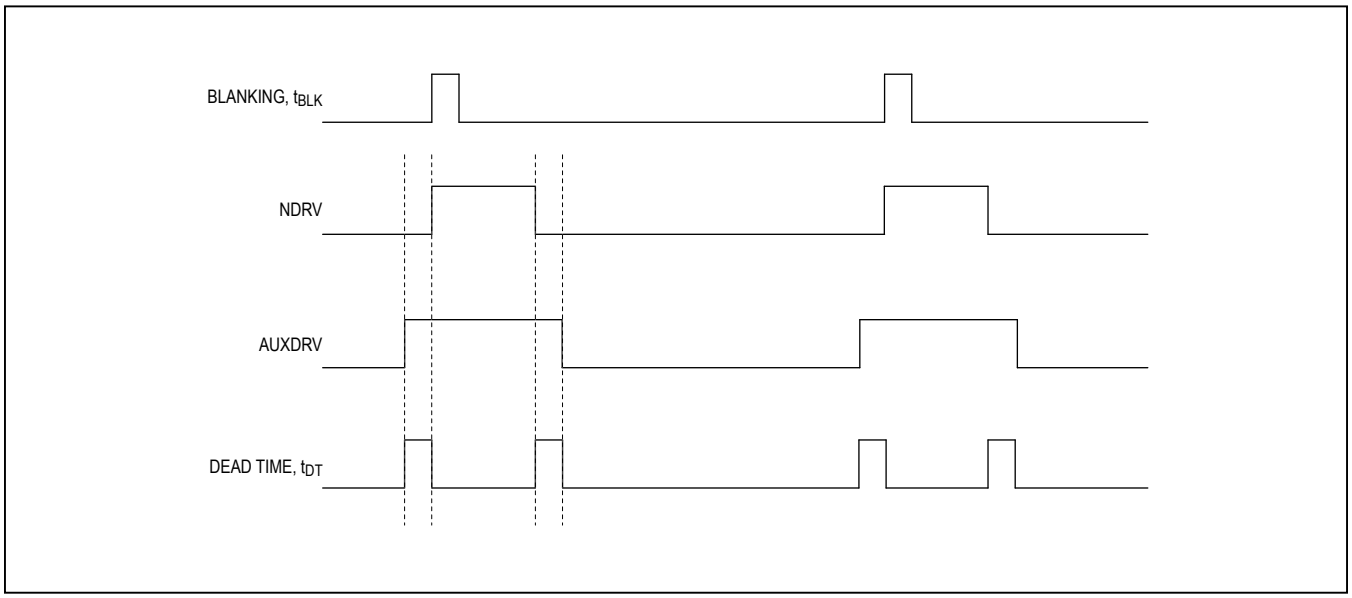


Figure 5. Dead Time Between AUXDRV and NDRV

Peak Current Limit

The current-sense resistor (R_{CS} in the *Typical Application Circuits*), connected between the source of the n-channel MOSFET and PGND, sets the current limit. The current-limit comparator has a voltage trip level ($V_{CS-PEAK}$) of 400mV. Use the following equation to calculate the value of R_{CS}:

$$R_{CS} = \frac{400mV}{I_{PRI}}$$

where I_{PRI} is the peak current in the primary side of the transformer, which also flows through the MOSFET. When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (NDRV) terminates the current on-cycle, within 35ns (typ).

The devices implement 115ns of leading-edge blanking to ignore leading-edge current spikes. These spikes are caused by reflected secondary currents, current-discharging capacitance at the FET's drain, and gate-charging current. Use a small RC network for additional filtering of the leading-edge spike on the sense waveform when needed. Set the corner frequency between 10MHz and 20MHz.

After the leading-edge blanking time, the device monitors V_{CS} for any breaches of the peak current limit of 400mV. The duty cycle is terminated immediately when V_{CS} exceeds 400mV.

Reverse Current Limit

The devices protect the transformer against saturation due to reverse current by monitoring the voltage across R_{CS} while the AUX output is low and the p-channel FET is on.

Output Short-Circuit Protection with Hiccup Mode

When the device detects eight consecutive peak current-limit events, both NDRV and AUXDRV driver outputs are turned off for a restart period, t_{RSTRT}. After t_{RSTRT}, the device undergoes soft-start. The duration of the restart period depends on the value of the capacitor at SS (C_{SS}). During this period, C_{SS} is discharged with a pulldown current of I_{SS-DH} (2µA typ). Once its voltage reaches 0.15V, the restart period ends and the device initiates a soft-start sequence. An internal counter ensures that the minimum restart period ($t_{RSTRT-MIN}$) is 1024 clock cycles when the time required for C_{SS} to discharge to 0.15V is less than 1024 clock cycles. Figure 6 shows the behavior of the device prior and during hiccup mode.

Frequency Foldback for High-Efficiency Light-Load Operation

The frequency foldback threshold can be programmed from 0 to 20% of the full load current using a resistor from FFB to GND.

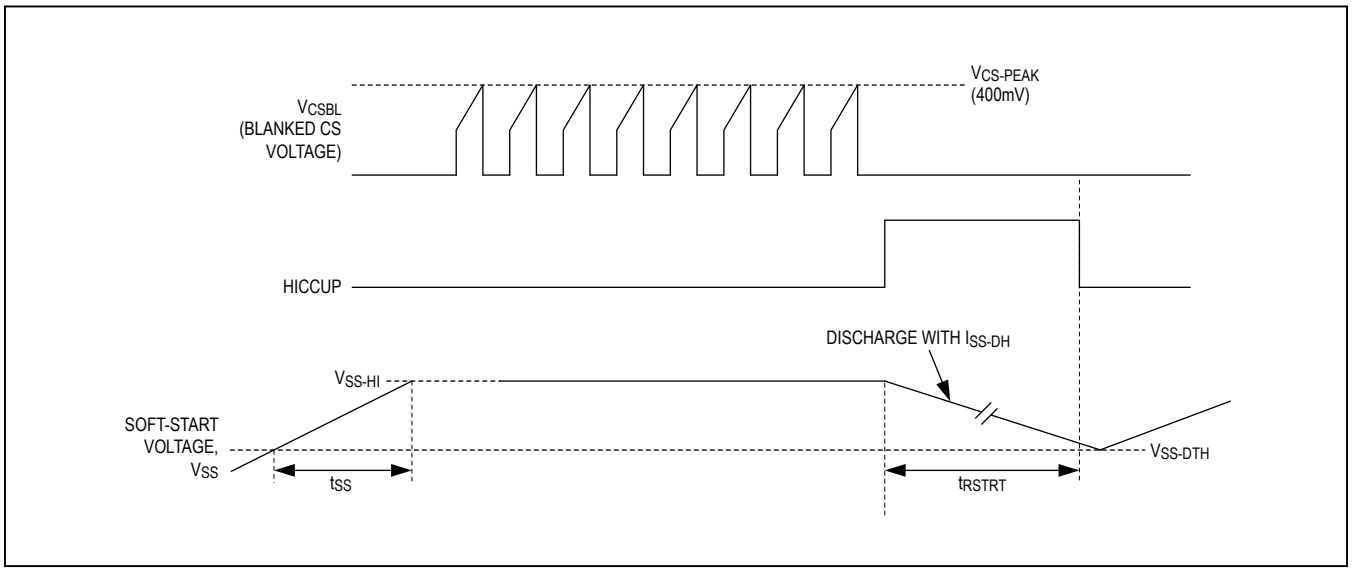


Figure 6. Hiccup Mode Timing Diagram

When V_{CSAVG} falls below V_{FFB}, the device folds back the switching frequency to 1/2 the original value to reduce switching losses and increase the converter efficiency. Calculate the value of R_{FFB} as follows:

$$R_{FFB} = \frac{10 \times I_{LOAD(LIGHT)} \times R_{CS}}{I_{FFB}}$$

where R_{FFB} is the resistor between FFB and GND, $I_{LOAD(LIGHT)}$ is the current at light-load conditions that triggers frequency foldback, R_{CS} is the value of the sense resistor connected between CS and PGND, and I_{FFB} is the current sourced from FFB to R_{FFB} (30µA typ).

Duty-Cycle Clamping

The maximum duty cycle is determined by the lowest of three voltages: 2V, the voltage at SS (V_{SS}), and the voltage (2.43V - V_{DCLMP}). The maximum duty cycle is calculated as:

$$D_{MAX} = \frac{V_{MIN}}{2.43V}$$

where V_{MIN} = minimum (2V, V_{SS}, 2.43V - V_{DCLMP}).

SS

By connecting a resistor between SS and ground, the voltage at SS can be made to be lower than 2V. V_{SS} is calculated as follows:

$$V_{SS} = R_{SS} \times I_{SS-CH}$$

where R_{SS} is the resistor connected between SS and GND, and I_{SS-CH} is the current sourced from SS to R_{SS} (10µA typ).

DCLMP

To set D_{MAX} using supply voltage feed-forward, connect a resistive divider between the supply voltage, DCLMP, and GND as shown in the *Typical Application Circuits*. This feed-forward duty-cycle clamp ensures that the external n-channel MOSFET is not stressed during supply transients. V_{DCLMP} is calculated as follows:

$$V_{DCLMP} = \frac{R_{DCLMP2}}{R_{DCLMP1} + R_{DCLMP2}} \times V_S$$

where R_{DCLMP1} and R_{DCLMP2} are the resistive divider values shown in the *Typical Application Circuits* and V_S is the input supply voltage.

Oscillator Synchronization

The internal oscillator can be synchronized to an external clock by applying the clock to DITHER/SYNC directly. The external clock frequency can be set anywhere between 1.1x to 2x the internal clock frequency.

Using an external clock increases the maximum duty cycle by a factor equal to f_{SYNC}/f_{SW}. This factor should be accounted for in setting the maximum duty cycle using any of the methods described in the *Duty-Cycle Clamping* section. The formula below shows how the maximum duty cycle is affected by the external clock frequency:

$$D_{MAX} = \frac{V_{MIN}}{2.43V} \times \frac{f_{SYNC}}{f_{SW}}$$

where V_{MIN} is described in the *Duty-Cycle Clamping* section, f_{SW} is the switching frequency as set by the resistor connected between RT and GND, and f_{SYNC} is the external clock frequency.

Frequency Dithering for Spread-Spectrum Applications (Low EMI)

The switching frequency of the converter can be dithered in a range of ±10% by connecting a capacitor from DITHER/SYNC to GND, and a resistor from DITHER/SYNC to RT as shown in the *Typical Application Circuits*. This results in lower EMI.

A current source at DITHER/SYNC charges the capacitor C_{DITHER} to 2V at 50µA. Upon reaching this trip point, it discharges C_{DITHER} to 0.4V at 50µA. The charging and discharging of the capacitor generates a triangular waveform on DITHER/SYNC with peak levels at 0.4V and 2V and a frequency that is equal to:

$$f_{TRI} = \frac{50\mu A}{C_{DITHER} \times 3.2V}$$

Typically, f_{TRI} should be set close to 1kHz. The resistor R_{DITHER} connected from DITHER/SYNC to RT determines the amount of dither as follows:

$$\%DITHER = \frac{4}{3} \times \frac{R_{RT}}{R_{DITHER}}$$

where %DITHER is the amount of dither expressed as a percentage of the switching frequency. Setting R_{DITHER} to 10 x R_{RT} generates ±10% dither.

Programmable Slope Compensation

The device generates a current ramp at CSSC such that its peak is 50µA at 80% duty cycle of the oscillator. An external resistor connected from CSSC to the CS then converts this current ramp into programmable slope-compensation amplitude, which is added to the current-sense signal for stability of the peak current-mode control loop. The ramp rate of the slope compensation signal is given by:

$$m = \frac{R_{CSSC} \times 50\mu A \times f_{SW}}{80\%}$$

where m is the ramp rate of the slope-compensation signal, R_{CSSC} is the value of the resistor connected between CSSC and CS used to program the ramp rate, and f_{SW} is the switching frequency.

Error Amplifier

The MAX5974A/MAX5974B include an internal error amplifier with a sample-and-hold input. The feedback input of the MAX5974C/MAX5974D is continuously connected. The noninverting input of the error amplifier is connected to the internal reference and feedback is provided at the inverting input. High open-loop gain and unity-gain bandwidth allow good closed-loop bandwidth and transient response. Calculate the power-supply output voltage using the following equation:

$$V_{OUT} = V_{REF} \times \frac{R_{FB1} + R_{FB2}}{R_{FB2}}$$

where V_{REF} = 1.52V for the MAX5974A/MAX5974B and V_{REF} = 1.215V for the MAX5974C/MAX5974D. The amplifier's noninverting input is internally connected to a soft-start circuit that gradually increases the reference voltage during startup. This forces the output voltage to come up in an orderly and well-defined manner under all load conditions.

Applications Information

Startup Time Considerations

The bypass capacitor at IN, C_{IN}, supplies current immediately after the devices wake up (see the *Typical Application Circuits*). Large values of C_{IN} increase the startup time, but also supply gate charge for more cycles during initial startup. If the value of C_{IN} is too small, V_{IN} drops below 7V because NDRV does not have enough time to switch and build up sufficient voltage across the tertiary output (MAX5974C/MAX5974D) or coupled inductor output (MAX5974A/MAX5974B), which powers the device. The device goes back into UVLO and does not start. Use a low-leakage capacitor for C_{IN}.

Typically, offline power supplies keep startup times to less than 500ms even in low-line conditions (85V AC input for universal offline or 36V DC for telecom applications). Size the startup resistor, R_{IN}, to supply both the maximum startup bias of the device (150µA) and the charging current for C_{IN}. C_{IN} must be charged to 16V within the desired 500ms time period. C_{IN} must store enough charge to deliver current to the device for at least the soft-start time (t_{SS}) set by C_{SS}. To calculate the approximate amount of capacitance required, use the following formula:

$$I_G = Q_{GTOT} f_{SW}$$

$$C_{IN} = \frac{(I_{IN} + I_G)(t_{SS})}{V_{HYST}}$$

where I_{IN} is the ICs' internal supply current (1.8mA) after startup, Q_{GTOT} is the total gate charge for the n-channel and p-channel FETs, f_{SW} is the ICs' switching frequency, V_{HYST} is the bootstrap UVLO hysteresis (9V typ), and t_{SS} is the soft-start time. R_{IN} is then calculated as follows:

$$R_{IN} \cong \frac{V_{S(MIN)} - V_{INUVR}}{I_{START}}$$

where $V_{S(MIN)}$ is the minimum input supply voltage for the application (36V for telecom), V_{INUVR} is the bootstrap UVLO wake-up level (16V), and I_{START} is the IN supply current at startup (150µA max).

R_{IN} needs to be reduced when operating at +125°C ambient temperature since the IN supply current is increased.

Choose a higher value for R_{IN} than the one calculated above if a longer startup time can be tolerated in order to minimize power loss on this resistor.

Active Clamp Circuit

Traditional clamp circuits prevent transformer saturation by channeling the magnetizing current (I_M) of the transformer onto a dissipative RC network. To improve efficiency, the active clamp circuit recycles I_M between the magnetizing inductance and clamp capacitor. V_{CLAMP} is given by:

$$V_{CLAMP} = \frac{V_S}{1-D}$$

where V_S is the voltage of the power source and D is the duty cycle. To select n-channel and p-channel FETs with adequate breakdown voltages, use the maximum value of V_{CLAMP}. $V_{CLAMP(MAX)}$ occurs when the input voltage is at its minimum and the duty cycle is at its maximum. $V_{CLAMP(MAX-NORMAL)}$ during normal operation is therefore:

$$V_{CLAMP(MAX-NORMAL)} = \frac{V_{S(MIN)}}{1-\frac{N_P \times V_O}{N_S \times V_{S(MIN)}}}$$

where $V_{S(MIN)}$ is the minimum voltage of the power source, N_P/N_S is the primary to secondary turns ratio, and V_O is the output voltage. The clamp capacitor, n-channel, and p-channel FETs must have breakdown voltages exceeding this level.

If feed-forward maximum duty-cycle clamp is used then:

$$D_{MAX-FF} = \frac{V_{MIN}}{2.43} = \left(1-\frac{V_{DCLMP}}{2.43}\right)$$

$$= \left(1-\frac{V_S}{2.43} \times \frac{R_{DCLMP2}}{R_{DCLMP1}+R_{DCLMP2}}\right)$$

Therefore, $V_{CLAMP(MAX-FF)}$ during feed-forward maximum duty clamp is:

$$V_{CLAMP(MAX-FF)} = \frac{V_S}{1-D_{MAX-FF}}$$

$$= \frac{2.43 \times (R_{DCLMP1}+R_{DCLMP2})}{R_{DCLMP2}}$$

The AUX driver controls the p-channel FET through a level shifter. The level shifter consists of an RC network (formed by C_{AUX} and R_{AUX}) and diode D5, as shown in the *Typical Application Circuits*. Choose R_{AUX} and C_{AUX} so that the time constant exceeds $100/f_{SW}$. Diode D5 is a small-signal diode with a voltage rating exceeding 25V.

Additionally, C_{CLAMP} should be chosen such that the complex poles formed with magnetizing inductance (L_{MAG}) and C_{CLAMP} are 2x to 4x away from the loop bandwidth:

$$\frac{1\text{-}D}{2\pi\sqrt{L_{MAG} \times C_{CLAMP}}} > 3 \times f_{BW}$$

Bias Circuit

Optocoupler Feedback (MAX5974C/MAX5974D)

An in-phase tertiary winding is needed to power the bias circuit when using optocoupler feedback. The voltage across the tertiary V_T during the on-time is:

$$V_T = V_{OUT} \times \frac{N_T}{N_S}$$

where V_{OUT} is the output voltage and N_T/N_S is the turns ratio from the tertiary to the secondary winding. Select the turns ratio so that V_T is above the UVLO shutdown level (7.35V max) by a margin determined by the holdup time needed to “ride through” a brownout.

Coupled-Inductor Feedback (MAX5974A/MAX5974B)

When using coupled-inductor feedback, the power for the devices can be taken from the coupled inductor during the off-time. The voltage across the coupled inductor, $V_{COUPLED}$, during the off-time is:

$$V_{COUPLED} = V_{OUT} \times \frac{N_C}{N_O}$$

where V_{OUT} is the output voltage and N_C/N_O is the turns ratio from the coupled output to the main output winding. Select the turns ratio so that $V_{COUPLED}$ is above the UVLO shutdown level (7.5V max) by a margin determined by the holdup time needed to “ride through” a brownout.

This voltage appears at the input of the devices, less a diode drop. An RC network consisting of R_{SNUB} and C_{SNUB} is for damping the reverse recovery transients of diode D6.

During on-time, the coupled output is:

$$V_{COUPLED\text{-}ON} = -(V_S \times \frac{N_S}{N_P} - V_{OUT})\frac{N_C}{N_O}$$

where V_S is the input supply voltage.

Care must be taken to ensure that the voltage at FB (equal to $V_{COUPLED\text{-}ON}$ attenuated by the feedback resistive divider) is not more than 5V:

$$V_{FB\text{-}ON} = V_{COUPLED\text{-}ON} \times \frac{R_{FB2}}{(R_{FB1} + R_{FB2})} < 5V$$

If this condition is not met, a signal diode should be placed from GND (anode) to FB (cathode).

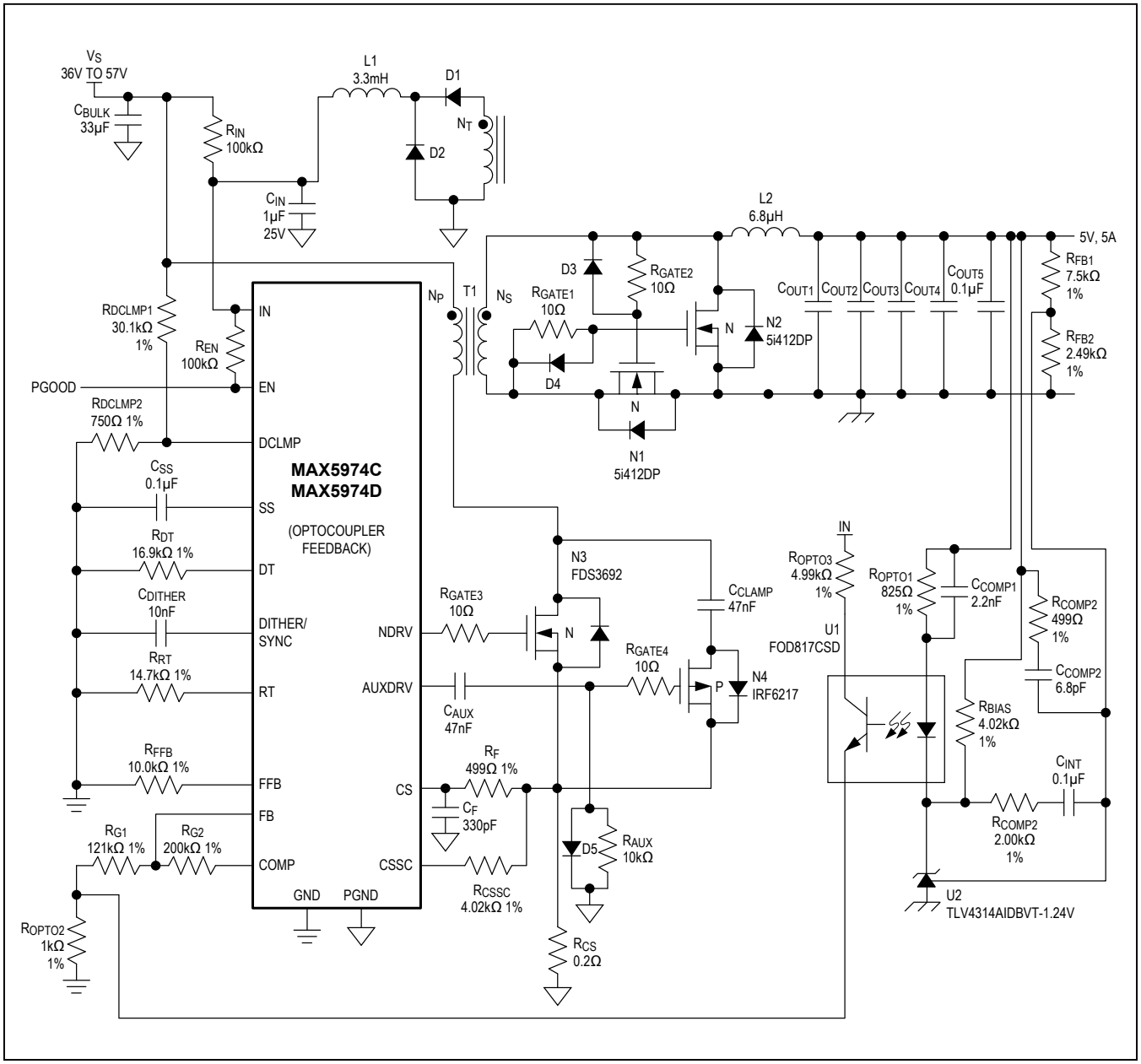
Layout Recommendations

Typically, there are two sources of noise emission in a switching power supply: high di/dt loops and high dV/dt surfaces. For example, traces that carry the drain current often form high di/dt loops. Similarly, the heatsink of the main MOSFET presents a dV/dt source; therefore, minimize the surface area of the MOSFET heatsink as much as possible. Keep all PCB traces carrying switching currents as short as possible to minimize current loops. Use a ground plane for best results.

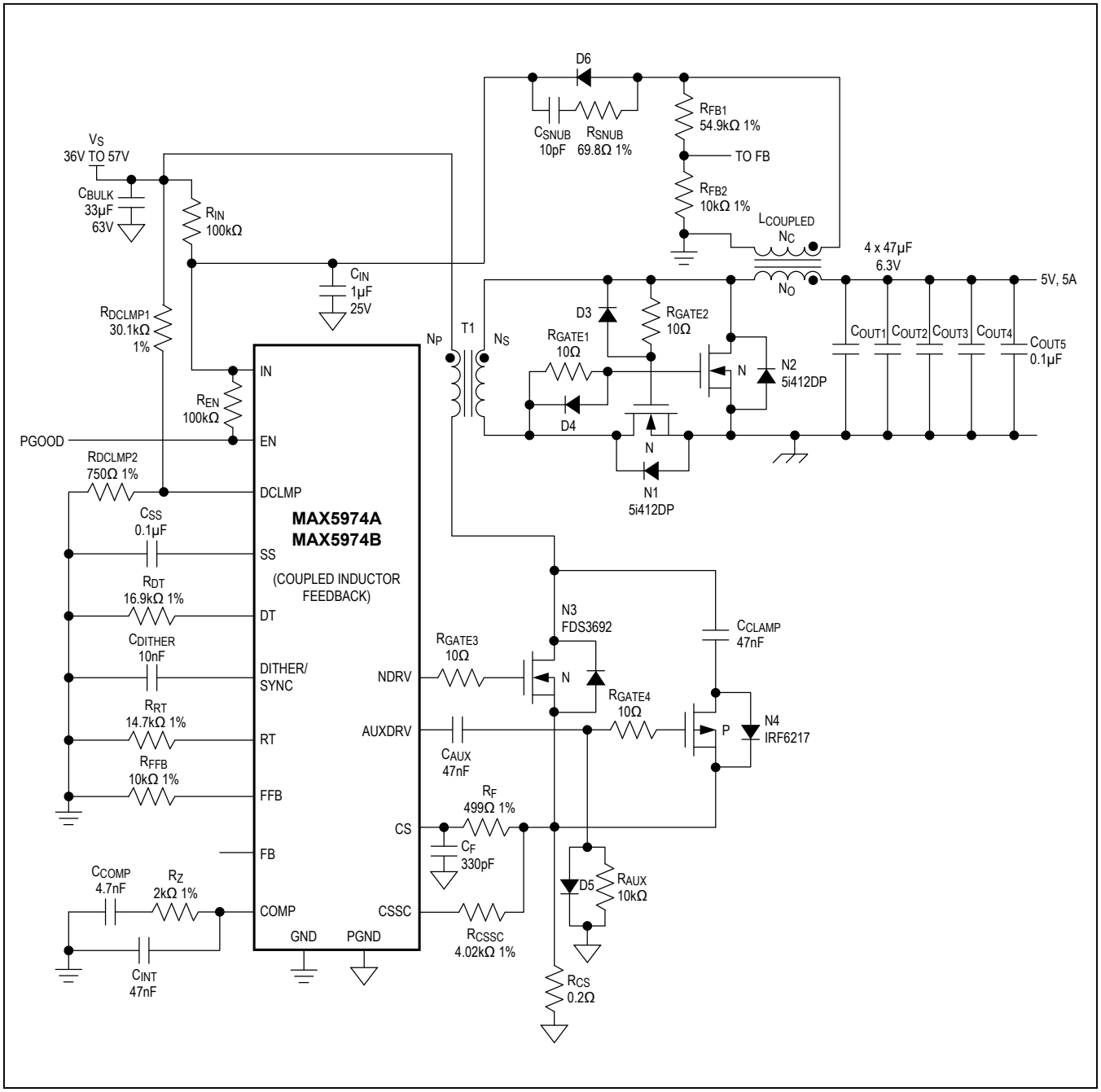
For universal AC input design, follow all applicable safety regulations. Offline power supplies can require UL, VDE, and other similar agency approvals.

Refer to the MAX5974A and MAX5974C Evaluation Kit data sheets for recommended layout and component values.

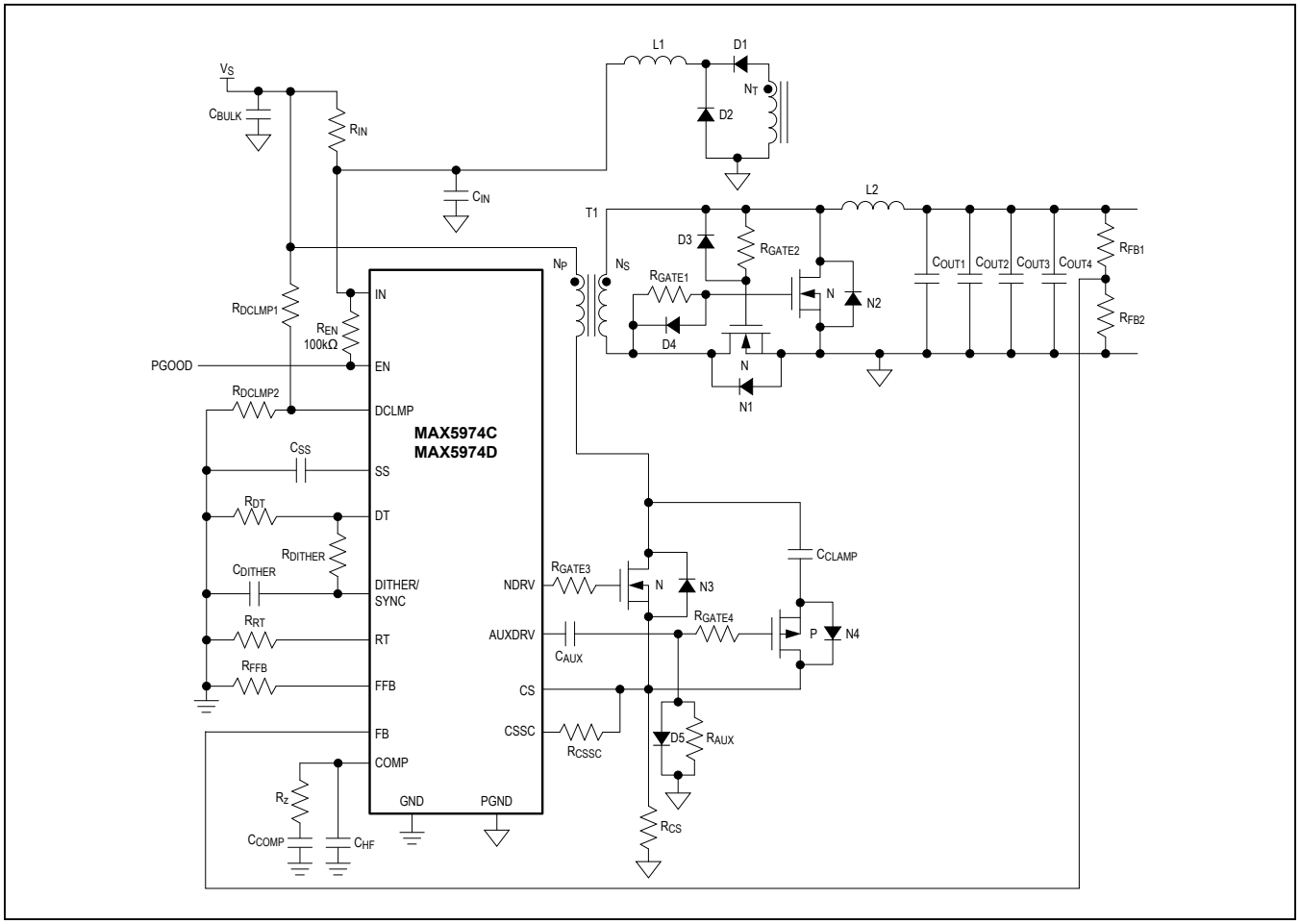
Typical Application Circuits



Typical Application Circuits (continued)



Typical Application Circuits (continued)



Ordering Information/Selector Guide

PART	TOP MARK	PIN-PACKAGE	TEMP RANGE	UVLO THRESHOLD (V)	FEEDBACK MODE
MAX5974AETE+	+AHY	16 TQFN-EP*	-40°C to +105°C	16	Sample/Hold
MAX5974AATE+**	+AHY	16 TQFN-EP*	-40°C to +125°C	16	Sample/Hold
MAX5974BETE+	+AHZ	16 TQFN-EP*	-40°C to +85°C	8.4	Sample/Hold
MAX5974BATE+	+AHZ	16 TQFN-EP*	-40°C to +125°C	8.4	Sample/Hold
MAX5974CETE+	+AIA	16 TQFN-EP*	-40°C to +85°C	16	Continuously Connected
MAX5974CATE+	+AIA	16 TQFN-EP*	-40°C to +125°C	16	Continuously Connected
MAX5974DETE+	+AIB	16 TQFN-EP*	-40°C to +85°C	8.4	Continuously Connected
MAX5974DATE+	+AIB	16 TQFN-EP*	-40°C to +125°C	8.4	Continuously Connected

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
***Future product—contact factory for availability.*

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/10	Initial release	—
1	9/10	Introduced the MAX5974B/MAX5974D. Updated the *Absolute Maximum Ratings*, *Electrical Characteristics*, *Pin Description*, the *p-Channel MOSFET Gate Driver*, *Frequency Foldback for High-Efficiency Light-Load Operation* sections, and *Typical Application Circuits*.	1, 2, 3, 12, 15, 17, 19, 21, 23, 24, 25
2	6/11	Added internal zener diode information	1–10, 12–17, 19–25
3	10/13	Updated COMP function in *Pin Description*, corrected pin name in *UVLO on Power Source* section, corrected Figures 1 and 2, corrected *Typical Application Circuits*	11, 16, 24–26
4	10/14	Added MAX5974DATE+ option to *Ordering Information*, *Electrical Characteristics*, and updated *Typical Application Circuits*	1, 2–5, 25–27
5	7/15	Removed EN from 2nd line in *Absolute Maximum Ratings* and changed the 1st line under Maximum Input/Output Current (continuous) from IN, NDRV, AUXDRV to EN	2
6	7/17	Updated *Absolute Maximum Ratings* section, *Electrical Characteristics* table, and *Ordering Information* table.	2–6, 27
7	12/17	Updated *Absolute Maximum Ratings* section, *Electrical Characteristics* table global characteristics, *Startup Time Considerations* section, and *Ordering Information* table.	2–6, 22, 27
7.1		Added future product designation to MAX5974AATE+in the *Ordering Information* table.	27
8	11/20	Updated *General Description*, *Electrical Characteristics* table, and *Ordering Information/Selector Guide* table.	1, 3–6, 27