-48V Hot-Swap Controller with External RSENSE

ABSOLUTE MAXIMUM RATINGS

All Voltages are Referenced to V_{EE}, Unless Otherwise Noted.
Supply Voltage (V_{DD} - V_{EE}) .....-0.3V to +100V
DRAIN, PWRGD, $\overline{PWRGD}$ .....-0.3V to +100V
PWRGD to DRAIN ..... -0.3V to +95V
PWRGD to V_{DD}.....-95V to +85V
SENSE (Internally Clamped) .....-0.3V to +1.0V
GATE (Internally Clamped) .....-0.3V to +18V
UV and OV.....-0.3V to +60V

Current Through SENSE.....±40mA
Current into GATE.....±300mA
Current into Any Other Pin.....±20mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 5.9mW/°C above +70°C).....471mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = 0V, V_{DD} = 48V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Notes 1, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Operating Input Voltage Range	V_{DD}		20		80	V
Supply Current	I_{DD}	(Note 2)		0.7	2	mA
GATE DRIVER AND CLAMPING CIRCUITS						
Gate Pin Pullup Current	I_{PU}	GATE drive on, V_{GATE} = V_{EE}	-30	-45	-60	µA
Gate Pin Pulldown Current	I_{PD}	GATE drive off , V_{GATE} = 2V	24	50	70	mA
External Gate Drive	ΔV_{GATE}	V_{GATE} - V_{EE}, 20V ≤ V_{DD} ≤ 80V	10	13.5	18	V
GATE to V_{EE} Clamp Voltage	V_{GSCLMP}	V_{GATE} - V_{EE}, I_{GS} = 30mA	15	16.4	18	V
CIRCUIT BREAKER						
Current-Limit Trip Voltage	V_{CL}	V_{CL} = V_{SENSE} - V_{EE}	40	50	60	mV
SENSE Input Bias Current		V_{SENSE} = 50mV	-1	-0.2	0	µA
UNDERVOLTAGE LOCKOUT						
Internal Undervoltage Lockout Voltage High	V_{UVLOH}	V_{DD} increasing	13.8	15.4	17.0	V
Internal Undervoltage Lockout Voltage Low	V_{UVLOL}	V_{DD} decreasing	11.8	13.4	15.0	V
UV PIN						
UV High Threshold	V_{UVH}	UV voltage increasing	1.240	1.255	1.270	V
UV Low Threshold	V_{UVL}	UV voltage decreasing	1.105	1.125	1.145	V
UV Hysteresis	$V_{UVHY\_}$			130		mV
UV Input Bias Current	I_{INUV}		-0.5		0	µA
OV PIN						
OV High Threshold	V_{OVH}	OV voltage increasing	1.235	1.255	1.275	V
OV Low Threshold	V_{OVL}	OV voltage decreasing	1.189	1.205	1.221	V
OV Voltage Reference Hysteresis	V_{OVHY}			50		mV
OV Input Bias Current	I_{INOV}	V_{OV} = V_{EE}	-0.5		0	µA
PWRGD OUTPUT SIGNAL REFERENCED TO DRAIN						
DRAIN Input Bias Current	I_{DRAIN}	V_{DRAIN} = 48V	10	80	250	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = 0V, V_{DD} = 48V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Notes 1, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRAIN Threshold for Power-Good	V_{DL}	V_{DRAIN} - V_{EE} threshold for power-good condition, DRAIN decreasing	1.1	1.7	2.0	V
GATE High Threshold	V_{GH}	ΔV_{GATE} - V_{GATE} threshold for power-good condition, ΔV_{GATE} - V_{GATE} decreasing	1.0	1.6	2.0	V
PWRGD, $\overline{PWRGD}$ Output Leakage	I_{OH}	$\overline{PWRGD}$ (MAX5920A) = 80V, V_{DRAIN} = 48V, PWRGD (MAX5920B) = 80V, V_{DRAIN} = 0V			10	µA
$\overline{PWRGD}$ Output Low Voltage	V_{OL}	$V_{\overline{PWRGD}}$ - V_{EE}; V_{DRAIN} - V_{EE} < V_{DL}, I_{SINK} = 5mA (MAX5920A)		0.11	0.4	V
PWRGD Output Low Voltage	V_{OL}	V_{PWRGD} - V_{DRAIN}; V_{DRAIN} = 5V, I_{SINK} = 5mA (MAX5920B)		0.11	0.4	V
OVERTEMPERATURE PROTECTION						
Overtemperature Threshold	T_{OT}	Junction temperature, temperature rising		135		°C
Overtemperature Hysteresis	T_{HYS}			20		°C
AC PARAMETERS						
OV High to GATE Low	t_{PHLOV}	Figures 1a, 2		0.5		µs
UV Low to GATE Low	t_{PHLUV}	Figures 1a, 3		0.4		µs
OV Low to GATE High	t_{PLHOV}	Figures 1a, 2		3.3		µs
UV High to GATE High	t_{PLHVL}	Figures 1a, 3		3.4		µs
SENSE High to GATE Low	$t_{PHLSENSE}$	Figures 1a, 4a		1	3	µs
Current Limit to GATE Low	t_{PHLCL}	Figures 1b, 4b	350	500	650	µs
DRAIN Low to $\overline{PWRGD}$ Low DRAIN Low to (PWRGD - DRAIN) High	t_{PHLDL}	MAX5920A, Figures 1a, 5a		1.8		µs
		MAX5920B, Figures 1a, 5a		3.4		
GATE High to $\overline{PWRGD}$ Low GATE High to (PWRGD-DRAIN) High	t_{PHLGH}	MAX5920A, Figures 1a, 5b		1.6		µs
		MAX5920B, Figures 1a, 5b		2.5		
TURN-OFF						
Latch-Off Period	t_{OFF}	(Note 3)		128 x t_{PHLCL}		ms

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to V_{EE}, unless otherwise specified.

Note 2: Current into V_{DD} with UV = 3V, OV, DRAIN, PWRGD, SENSE = V_{EE}, GATE = floating.

Note 3: Minimum duration of GATE pulldown following a circuit-breaker fault. The circuit breaker can be reset during this time by toggling UV low, but the GATE pulldown does not release until t_{OFF} has elapsed.

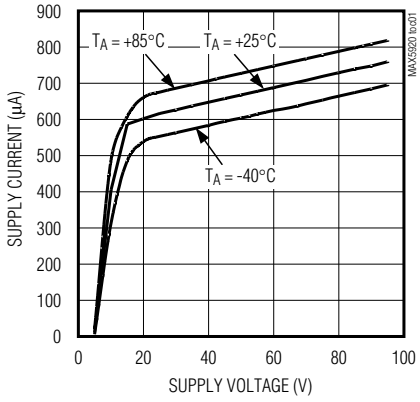
Note 4: Limits are 100% tested at T_A = +25°C and +85°C. Limits at -40°C are guaranteed by design.

-48V Hot-Swap Controller with External RSENSE

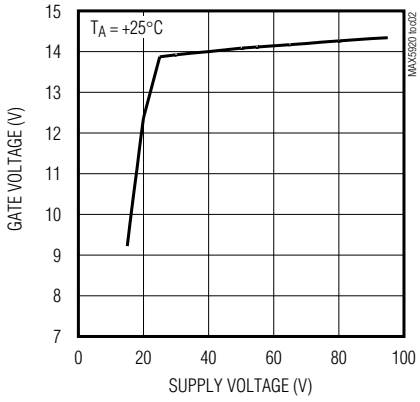
Typical Operating Characteristics

(V_{DD} = 48V, V_{EE} = 0V, T_A = +25°C, unless otherwise noted.)

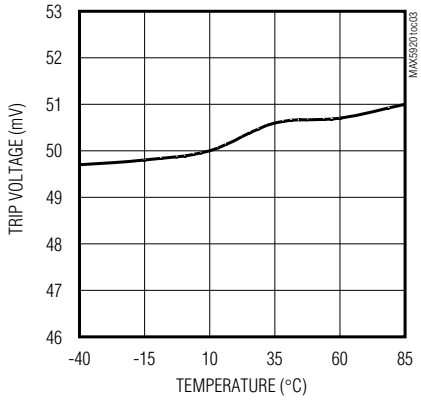
SUPPLY CURRENT vs. SUPPLY VOLTAGE



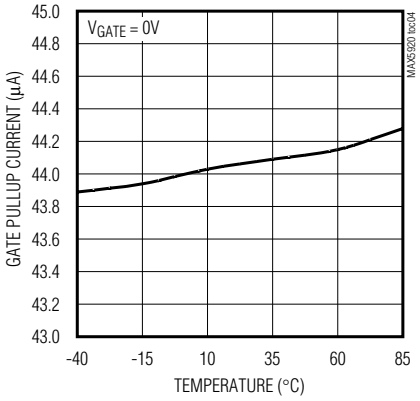
GATE VOLTAGE vs. SUPPLY VOLTAGE



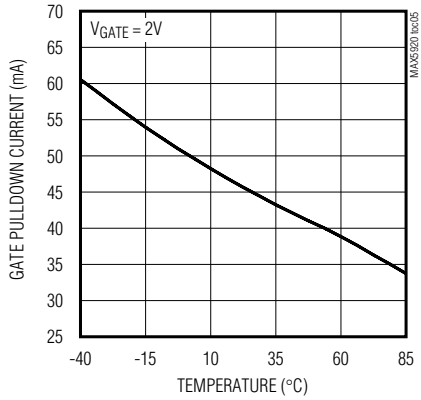
CURRENT-LIMIT TRIP VOLTAGE vs. TEMPERATURE



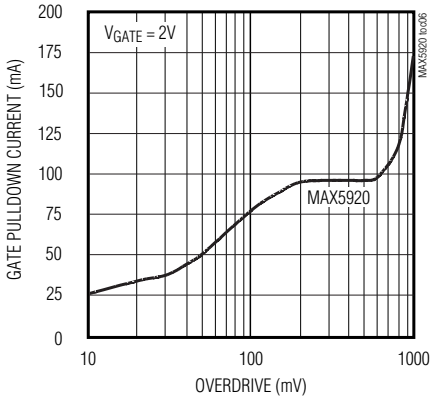
GATE PULLUP CURRENT vs. TEMPERATURE



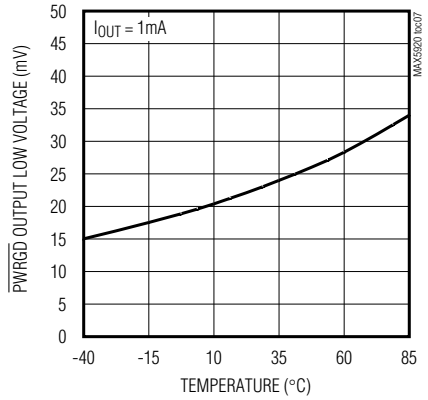
GATE PULLDOWN CURRENT vs. TEMPERATURE



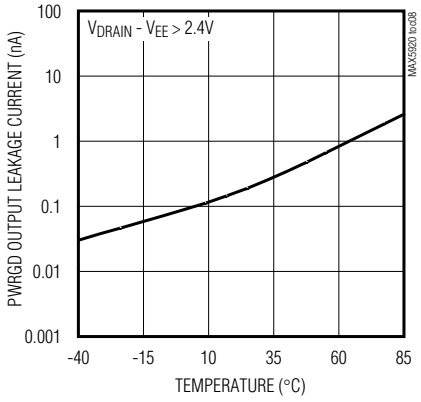
GATE PULLDOWN CURRENT vs. OVERDRIVE



$\overline{PWRGD}$ OUTPUT LOW VOLTAGE vs. TEMPERATURE (MAX5920A)



PWRGD OUTPUT LEAKAGE CURRENT vs. TEMPERATURE (MAX5920B)



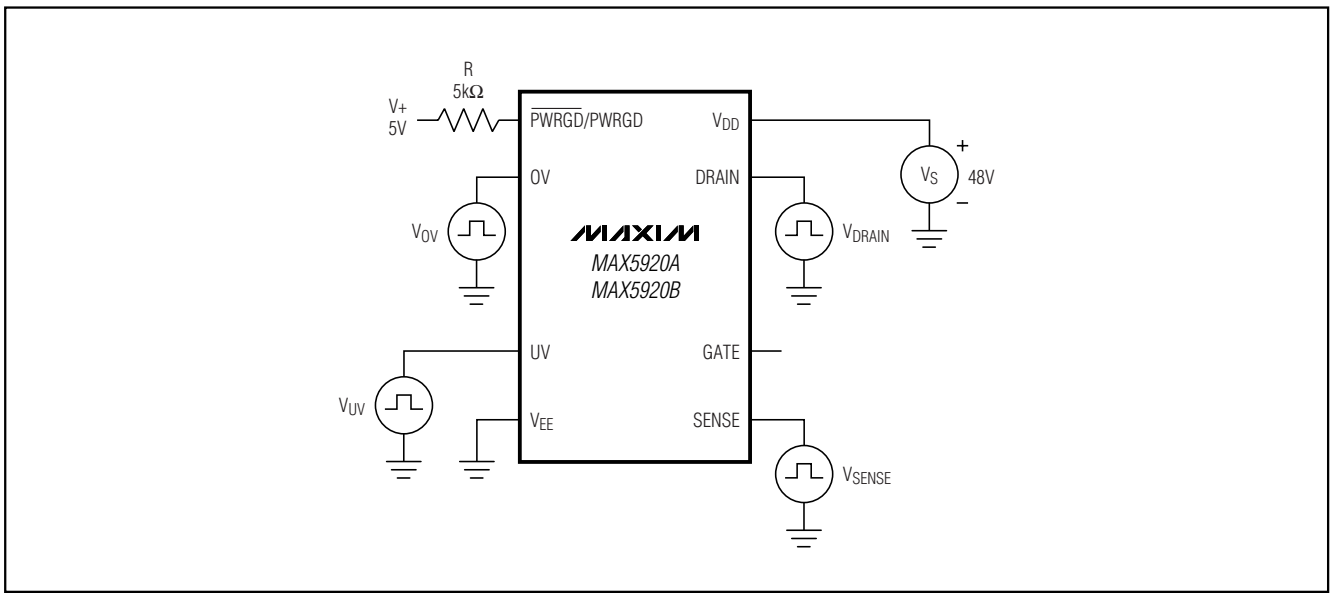


Figure 1a. Test Circuit 1

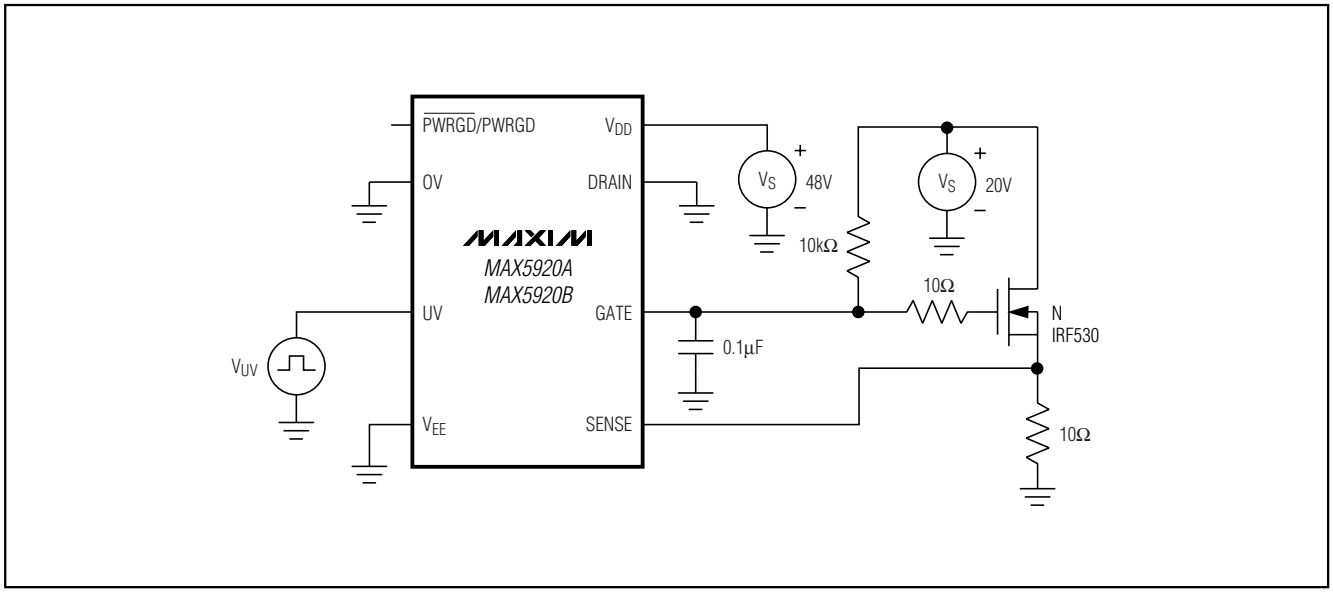


Figure 1b. Test Circuit 2

-48V Hot-Swap Controller with External RSENSE

Timing Diagrams

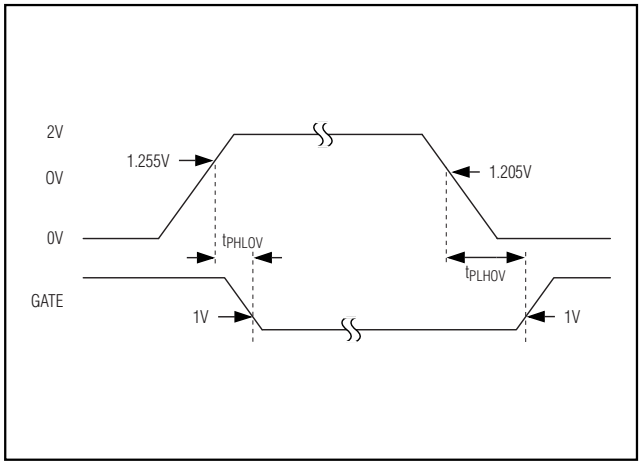


Figure 2. OV to GATE Timing

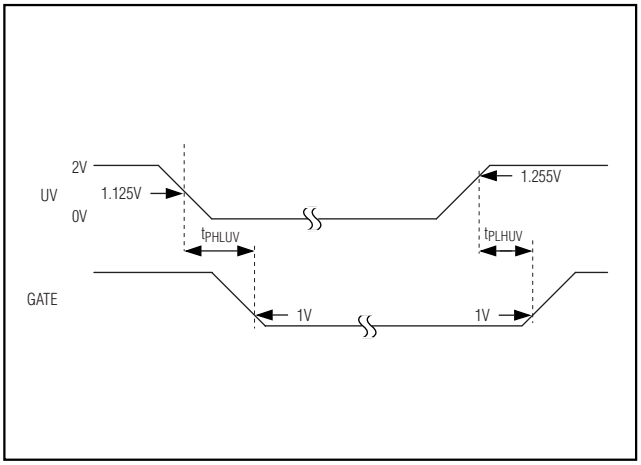


Figure 3. UV to GATE Timing

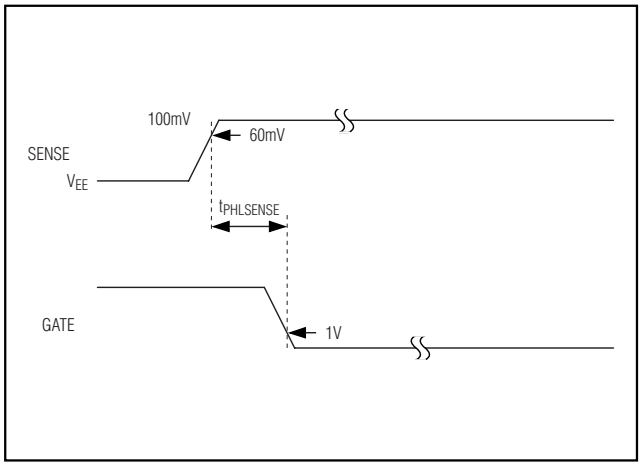


Figure 4a. SENSE to GATE Timing

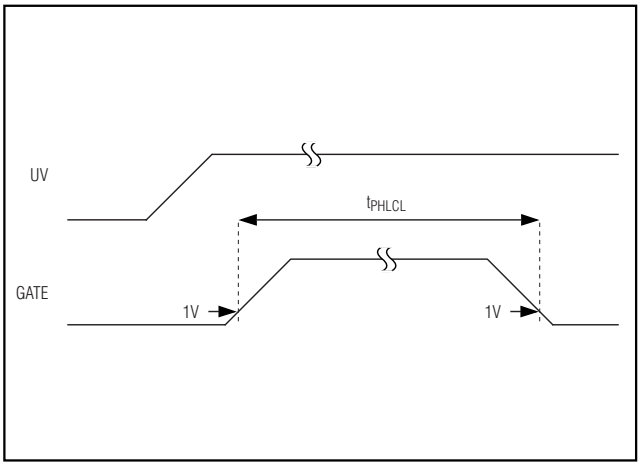


Figure 4b. Active Current-Limit Threshold

Timing Diagrams (continued)

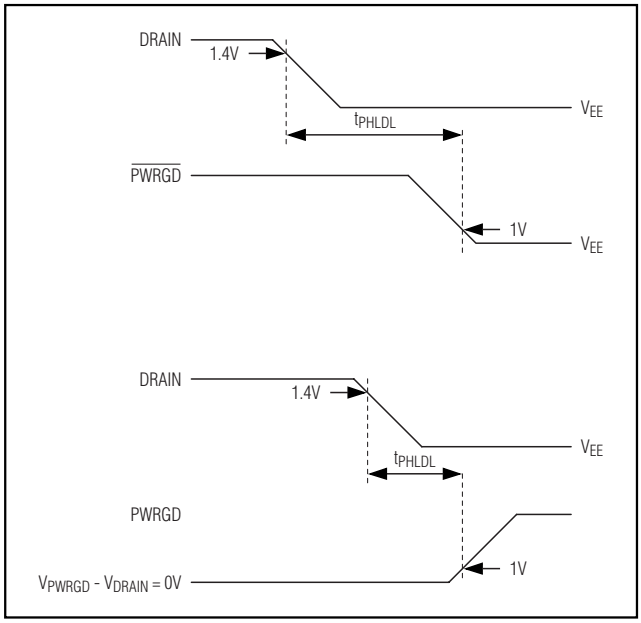


Figure 5a. DRAIN to $\overline{PWRGD}$/PWRGD Timing

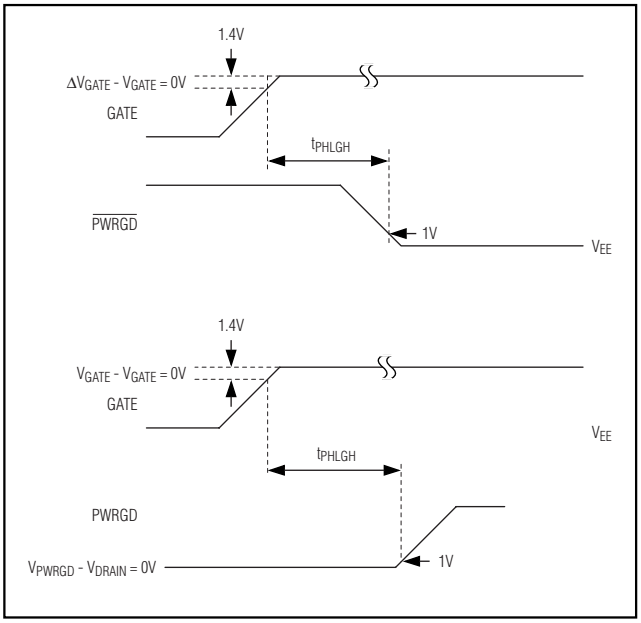
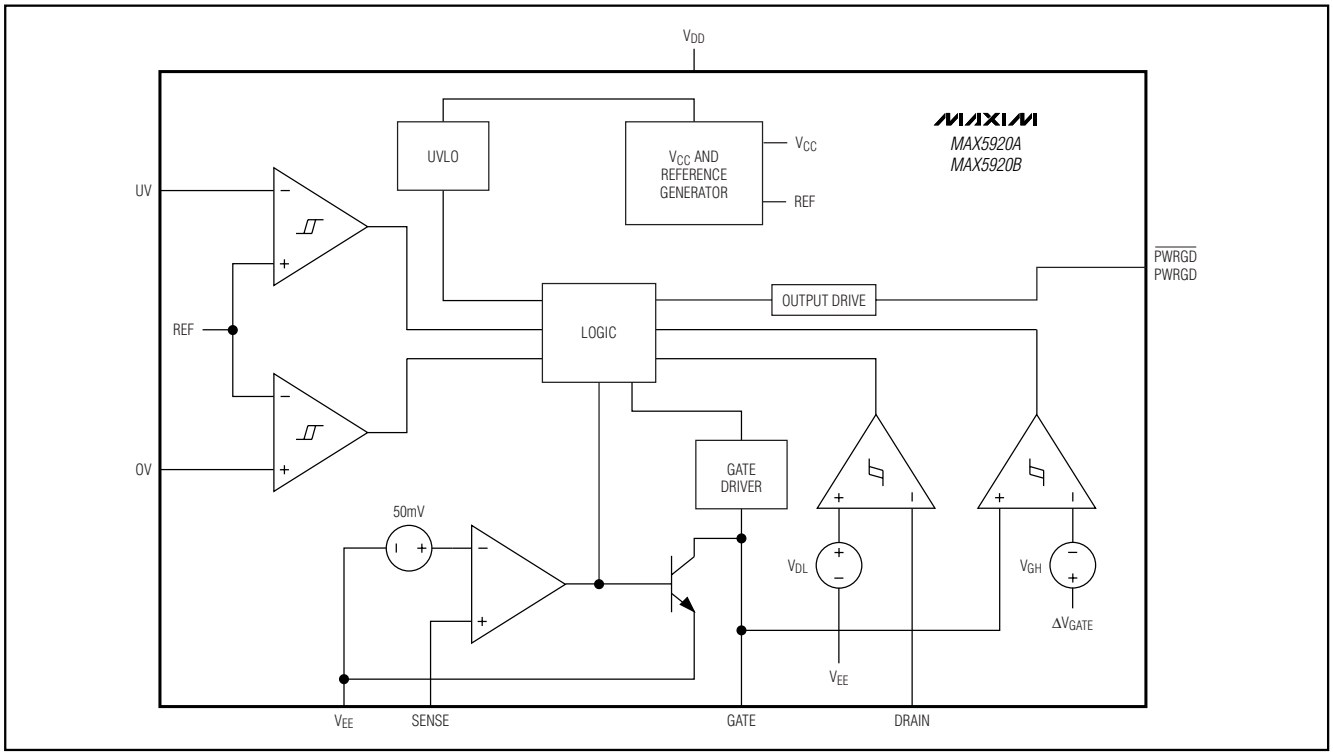


Figure 5b. GATE to $\overline{PWRGD}$/PWRGD Timing

Block Diagram



-48V Hot-Swap Controller with External RSENSE

Pin Description

PIN		NAME	FUNCTION
MAX5920A	MAX5920B		
1	—	$\overline{PWRGD}$	Power-Good Signal Output. $\overline{PWRGD}$ is an active-low open-drain status output referenced to V_{EE}. $\overline{PWRGD}$ is latched low when V_{DRAIN} - $V_{EE} \le V_{DL}$ and $V_{GATE} > (\Delta V_{GATE} - V_{GH})$, indicating a power-good condition. $\overline{PWRGD}$ is open drain otherwise.
—	1	PWRGD	Power-Good Signal Output. PWRGD is an active-high open-drain status output referenced to DRAIN. PWRGD latches in a high-impedance state when V_{DRAIN} - $V_{EE} \le V_{DL}$ and $V_{GATE} > (\Delta V_{GATE} - V_{GH})$, indicating a power-good condition. PWRGD is pulled low to DRAIN otherwise.
2	2	OV	Input Pin for Overvoltage Detection. OV is referenced to V_{EE}. When OV is pulled above V_{OVH} voltage, the GATE pin is immediately pulled low. The GATE pin remains low until the OV pin voltage reduces to V_{OVL}.
3	3	UV	Input Pin for Undervoltage Detection. UV is referenced to V_{EE}. When UV is pulled above V_{UVH} voltage, the GATE is enabled. When UV is pulled below V_{UVL}, GATE is pulled low. UV is also used to reset the circuit breaker after a fault condition. To reset the circuit breaker, pull UV below V_{UVL}. The reset command can be issued immediately after a fault condition; however, the device does not restart until a t_{OFF} delay time has elapsed after the fault.
4	4	V_{EE}	Device Negative Power-Supply Input. Connect to the negative power-supply rail.
5	5	SENSE	Current-Sense Voltage Input. Connect to an external sense resistor and the external MOSFET source. The voltage drop across the external sense resistor is monitored to detect overcurrent or short-circuit fault conditions. Connect SENSE to V_{EE} to disable the current-limiting feature.
6	6	GATE	Gate Drive Output. Connect to gate of the external N-channel MOSFET.
7	7	DRAIN	Output-Voltage Sense Input. Connect to the output-voltage node (drain of external N-channel MOSFET). Place the MAX5920_ so the DRAIN pin is close to the DRAIN of the external MOSFET for the best thermal protection.
8	8	V_{DD}	Positive Power-Supply Rail Input. This is the power ground in the negative-supply voltage system. Connect to the higher potential of the power-supply inputs.

Detailed Description

The MAX5920A/MAX5920B are integrated hot-swap controllers for -48V power systems. They allow circuit boards to be safely hot plugged into a live backplane without causing a glitch on the power-supply rail. When circuit boards are inserted into a live backplane, the bypass capacitors at the input of the board's power module or switching power supply can draw large inrush currents as they charge. The inrush currents can cause glitches on the system power-supply rail and damage components on the board.

The MAX5920A/MAX5920B provide a controlled turn-on to circuit cards preventing glitches on the power-supply rail and damage to board connectors and components. Both the MAX5920A and MAX5920B provide undervoltage, overvoltage, and overcurrent protection. The MAX5920A/MAX5920B ensure the input voltage is stable and within tolerance before applying power to the load. The devices also provide protection against input voltage steps. During an input voltage step, the MAX5920A/MAX5920B limit the current drawn by the load to a safe level without turning off power to the load.

Board Insertion

Figure 6a shows a typical hot-swap circuit for -48V systems. When the circuit board first makes contact with the backplane, the DRAIN to GATE capacitance (C_{gd}) of Q1 pulls up the GATE voltage to roughly $|V_{EE} \times C_{gd} / C_{gd} + C_{gs}|$. The MAX5920_ features an internal dynamic clamp between GATE and V_{EE} to keep the gate-to-source voltage of Q1 low during hot insertion, preventing Q1 from passing an uncontrolled current to the load. For most applications, the internal clamp between GATE and V_{EE} of the MAX5920A/MAX5920B eliminates the need for an external gate-to-source capacitor. Resistor R3 limits the current into the clamp circuitry during card insertion.

Power-Supply Ramping

The MAX5920A/MAX5920B can reside either on the backplane or the removable circuit board (Figure 6a). Power is delivered to the load by placing an external N-channel MOSFET pass transistor in the power-supply path.

After the circuit board is inserted into the backplane and the supply voltage at V_{EE} is stable and within the undervoltage and overvoltage tolerance, the MAX5920A/MAX5920B turn on Q1. The MAX5920A/MAX5920B gradually turn on the external MOSFET by charging the gate of Q1 with a 45µA current source.

Capacitor C2 provides a feedback signal to accurately limit the inrush current. The inrush current can be calculated:

$$I_{INRUSH} = I_{PU} \times C_L / C2$$

where C_L is the total load capacitance, C3 + C4, and I_{PU} is the MAX5920_ gate pullup current.

Figure 6b shows the inrush current waveform. The current through C2 controls the GATE voltage. At the end of the DRAIN ramp, the GATE voltage is charged to its final value. The GATE-to-SENSE clamp limits the maximum V_{GS} to about 18V under any condition.

Board Removal

If the circuit card is removed from the backplane, the voltage at the UV pin falls below the UVLO detect threshold, and the MAX5920_ turns off the external MOSFET.

Current Limit and Electronic Circuit Breaker

The MAX5920_ provides current-limiting and circuit-breaker features that protect against excessive load current and short-circuit conditions. The load current is monitored by sensing the voltage across an external sense resistor connected between V_{EE} and SENSE.

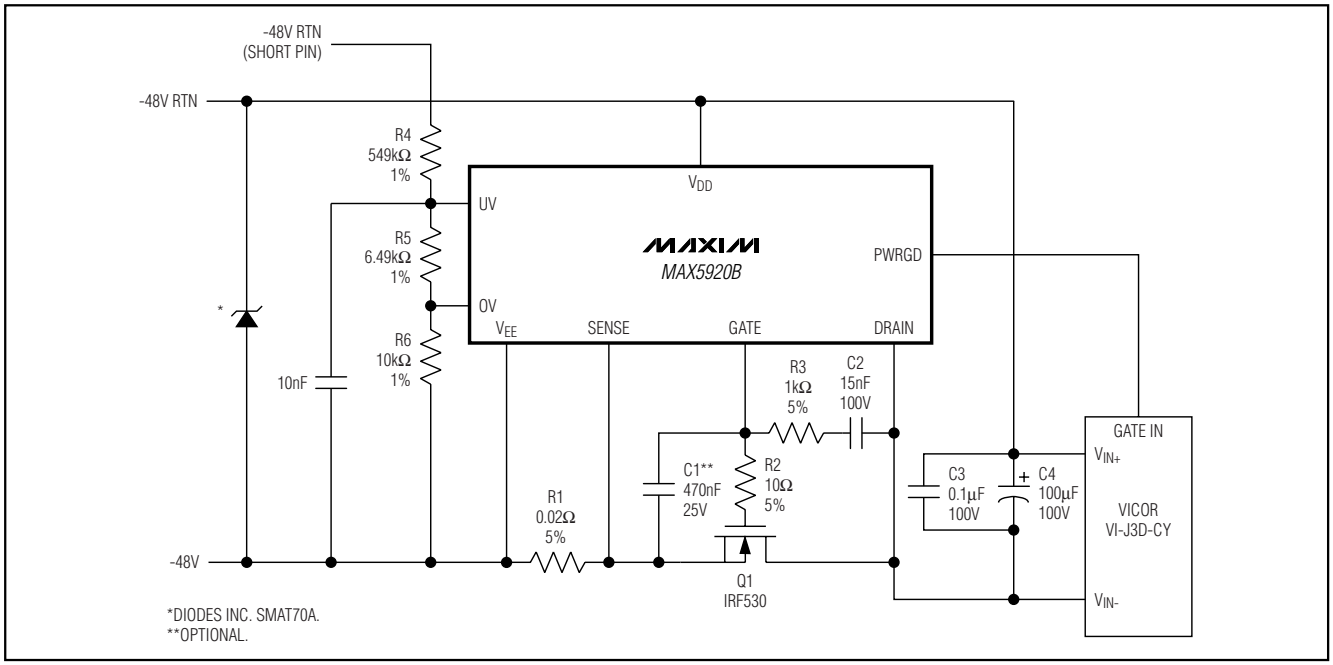


Figure 6a. Inrush Control Circuitry

-48V Hot-Swap Controller with External RSENSE

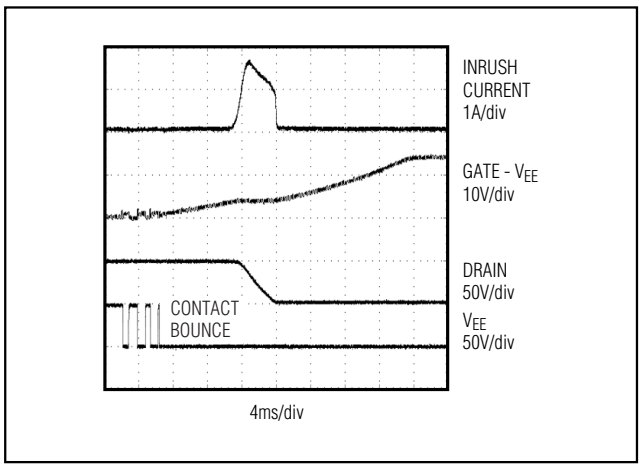


Figure 6b. Input Inrush Current

If the voltage between V_{EE} and SENSE reaches the current-limit trip voltage (V_{CL}), the MAX5920_ pulls down the GATE pin and regulates the current through the external MOSFET so $V_{SENSE} - V_{EE} \leq V_{CL}$. If the current drawn by the load drops below V_{CL} / R_{SENSE} limit, the GATE pin voltage rises again. However, if the load current is at the regulation limit of V_{CL} / R_{SENSE} for a period of t_{PHLCL}, the electronic circuit breaker trips, causing the MAX5920A/MAX5920B to turn off the external MOSFET.

After an overcurrent fault condition, the circuit breaker is reset by pulling the UV pin low and then pulling UV high or by cycling power to the MAX5920A/MAX5920B. Unless power is cycled to the MAX5920A/MAX5920B, the device waits until t_{OFF} has elapsed before turning on the gate of the external FET.

Overcurrent Fault Integrator

The MAX5920_ feature an overcurrent fault integrator. When an overcurrent condition exists, an internal digital counter increments its count. When the counter reaches 500µs (the maximum current-limit duration) for the MAX5920_, an overcurrent fault is generated. If the overcurrent fault does not last 500µs, then the counter begins decrementing at a rate 128 (maximum current-limit duty cycle) times slower than the counter was incrementing. Repeated overcurrent conditions will generate a fault if duty cycle of the overcurrent condition is greater than 1/128.

Load-Current Regulation

The MAX5920A/MAX5920B accomplish load-current regulation by pulling current from the GATE pin whenever $V_{SENSE} - V_{EE} > V_{CL}$ (see *Typical Operating Characteristics*). This decreases the gate-to-source voltage of the external MOSFET, thereby reducing the load current. When $V_{SENSE} - V_{EE} < V_{CL}$, the MAX5920A/MAX5920B pull the GATE pin high by a 45µA (I_{PU}) current.

Driving into a Shorted Load

In the event of a permanent short-circuit condition, the MAX5920A/MAX5920B limit the current drawn by the load to V_{CL} / R_{SENSE} for a period of t_{PHLCL}, after which the circuit breaker trips. Once the circuit breaker trips, the GATE of the external FET is pulled low by 50mA (I_{PD}) turning off power to the load.

Immunity to Input Voltage Steps

The MAX5920A/MAX5920B guard against input voltage steps on the input supply. A rapid increase in the input supply voltage ($V_{DD} - V_{EE}$ increasing) causes a current step equal to $I = C_L \times \Delta V_{IN} / \Delta T$, proportional to the input voltage slew rate ($\Delta V_{IN} / \Delta T$). If the load current exceeds V_{CL} / R_{SENSE} during an input voltage step, the MAX5920A/MAX5920B current limit activates, pulling down the gate voltage and limiting the load current to V_{CL} / R_{SENSE}. The DRAIN voltage (V_{DRAIN}) then slews at a slower rate than the input voltage. As the drain voltage starts to slew down, the drain-to-gate feedback capacitor C2 pushes back on the gate, reducing the gate-to-source voltage (V_{GS}) and the current through the external MOSFET. Once the input supply reaches its final value, the DRAIN slew rate (and therefore the inrush current) is limited by the capacitor C2 just as it is limited in the startup condition. To ensure correct operation, R_{SENSE} must be chosen to provide a current limit larger than the sum of the load current and the dynamic current into the load capacitance in the slewing mode.

If the load current plus the capacitive charging current is below the current limit, the circuit breaker does not trip.

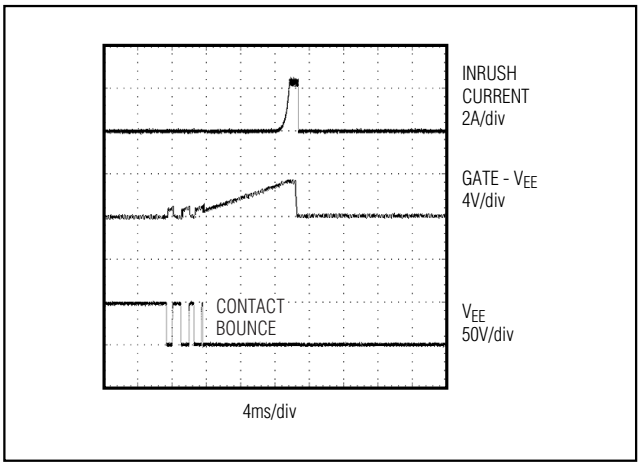


Figure 7a. Startup Into a Short Circuit

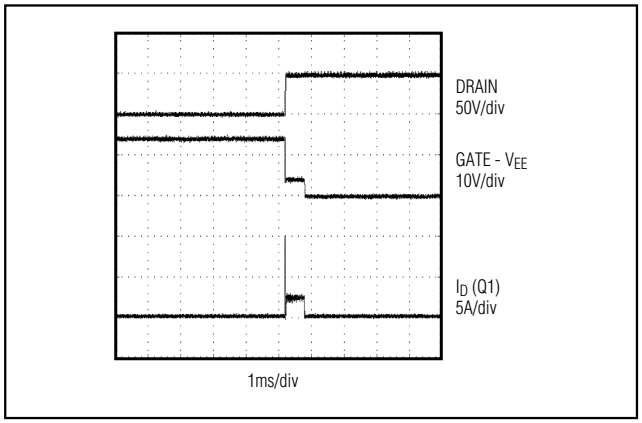


Figure 7b. Short-Circuit Protection Waveform

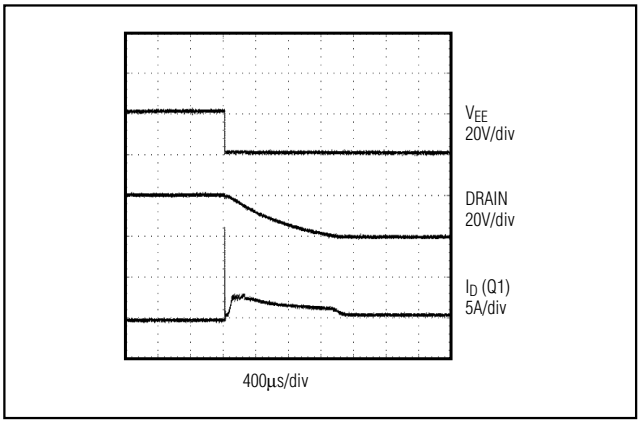


Figure 8. Voltage Step-On Input Supply

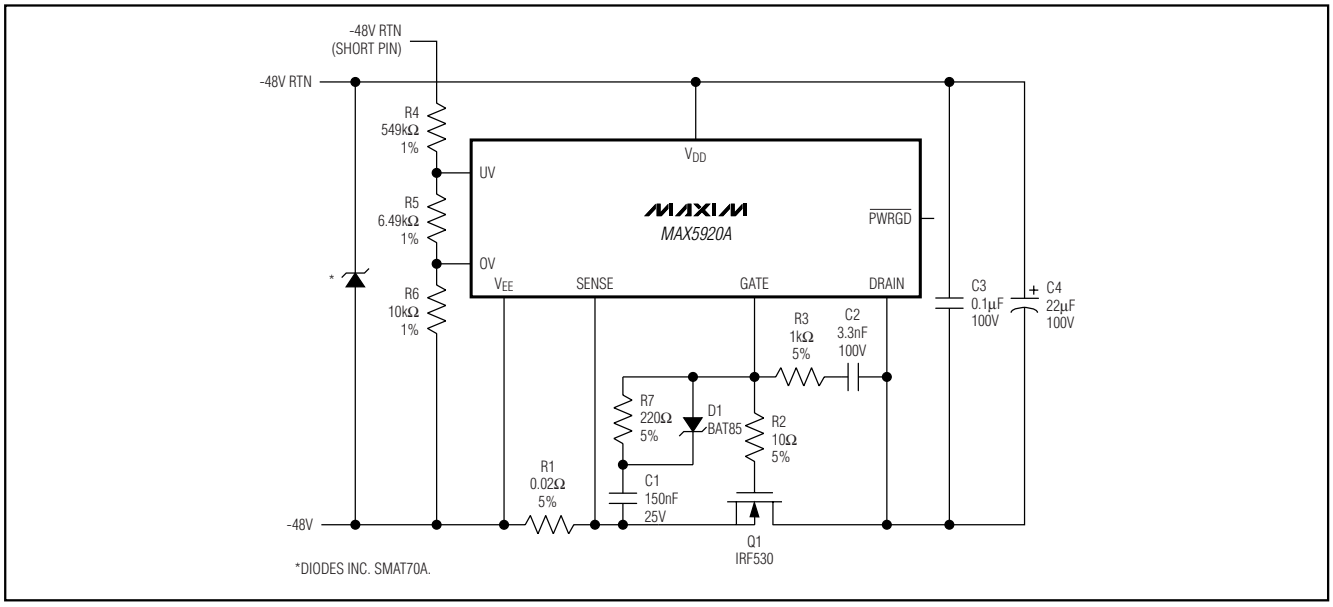


Figure 9. Circuit for Input Steps with Small C1

For C2 values less than 10nF, a positive voltage step on the input supply can result in Q1 turning off momentarily, which can shut down the output. By adding an additional resistor and diode, Q1 remains on during the voltage step. This is shown as D1 and R7 in Figure 9. The purpose of D1 is to shunt current around R7 when the power pins first make contact and allow C1 to hold the GATE low. The value of R7 should be sized to generate an R7 x C1 time constant of 33µs.

Undervoltage and Overvoltage Protection

The UV and OV pins can be used to detect undervoltage and overvoltage conditions. The UV and OV pins are internally connected to analog comparators with 130mV (UV) and 50mV (OV) of hysteresis. When the UV voltage falls below its threshold or the OV voltage rises above its threshold, the GATE pin is immediately pulled low. The GATE pin is held low until UV goes high and OV is low, indicating that the input supply voltage is within specification. The MAX5920_ includes an internal lockout (UVLO) that keeps the external MOSFET off until the input supply voltage exceeds 15.4V, regardless of the UV input.

The UV pin is also used to reset the circuit breaker after a fault condition has occurred. The UV pin can be pulled below V_{UVL} to reset the circuit breaker.

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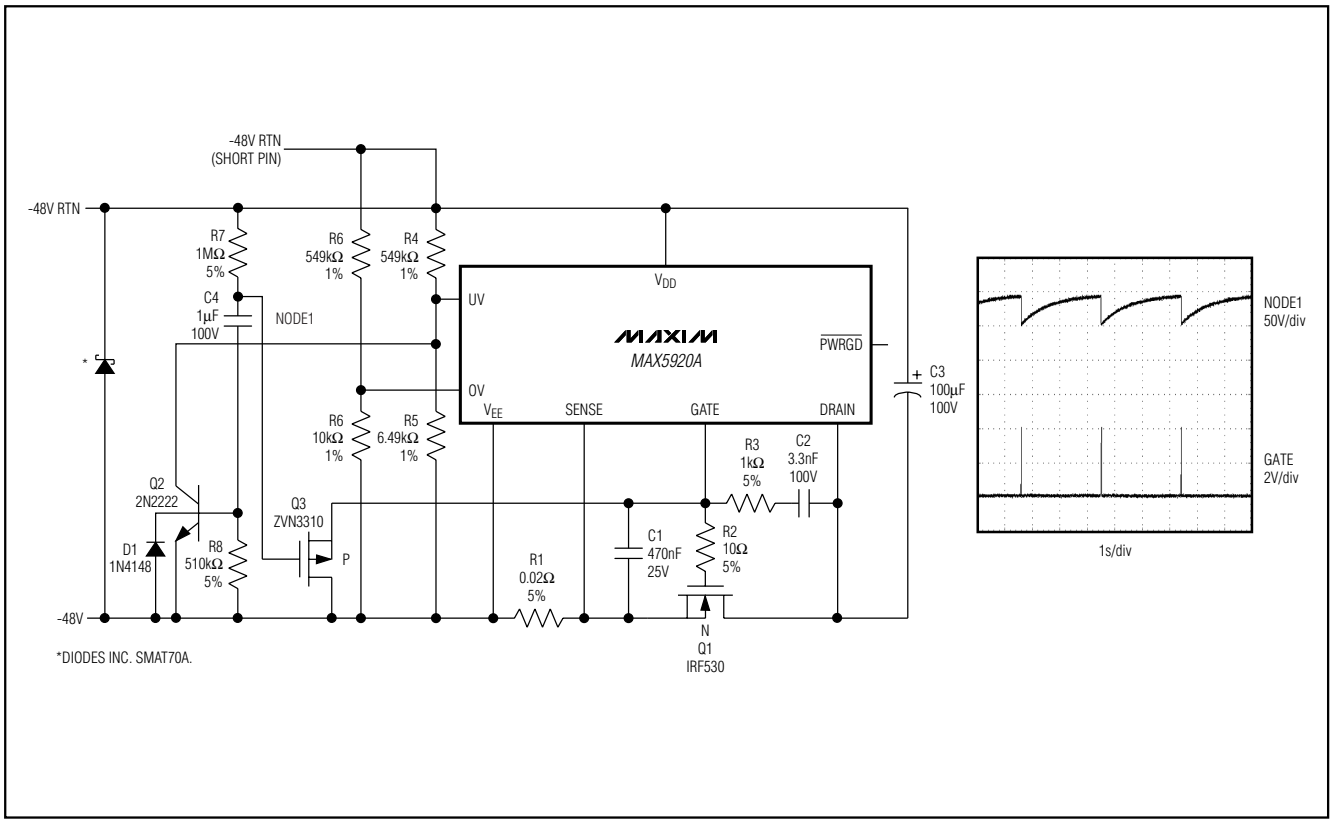

Figure 10. Automatic Restart After Current Fault

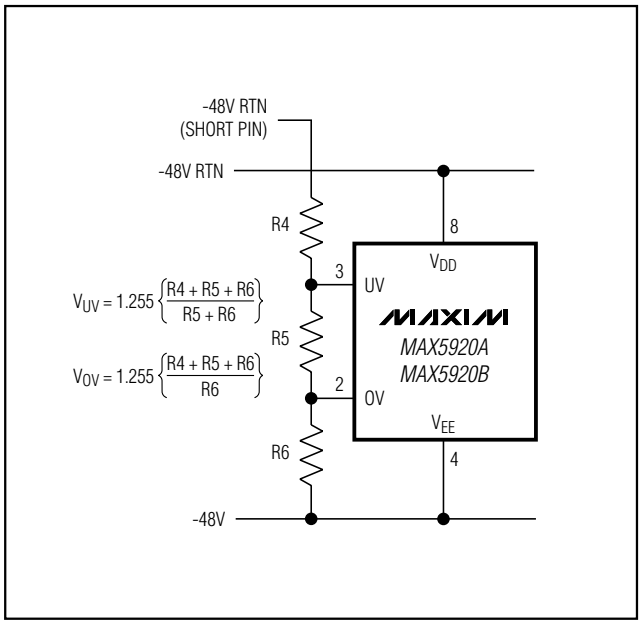

Figure 11. Undervoltage and Overvoltage Sensing

Figure 11 shows how to program the undervoltage and overvoltage trip thresholds using three resistors. With R4 = 549kΩ, R5 = 6.49kΩ, and R6 = 10kΩ, the undervoltage threshold is set to 38.5V (with a 43V release from undervoltage), and the overvoltage is set to 71V. The resistor-divider also increases the hysteresis and overvoltage lockout to 4.5V and 2.8V at the input supply, respectively.

$\overline{\text{PWRGD}}$/PWRGD Output

The $\overline{\text{PWRGD}}$ (PWRGD) output can be used directly to enable a power module after hot insertion. The MAX5920A ($\overline{\text{PWRGD}}$) can be used to enable modules with an active-low enable input (Figure 13), while the MAX5920B (PWRGD) is used to enable modules with an active-high enable input (Figure 12).

The PWRGD signal is referenced to the DRAIN terminal, which is the negative supply of the power module. The $\overline{\text{PWRGD}}$ signal is referenced to V_{EE}.

When the DRAIN voltage of the MAX5920A is high with respect to V_{EE} or the GATE voltage is low, the internal pulldown MOSFET Q2 is off and the $\overline{\text{PWRGD}}$ pin is in a high-impedance state (Figure 13). The $\overline{\text{PWRGD}}$ pin is

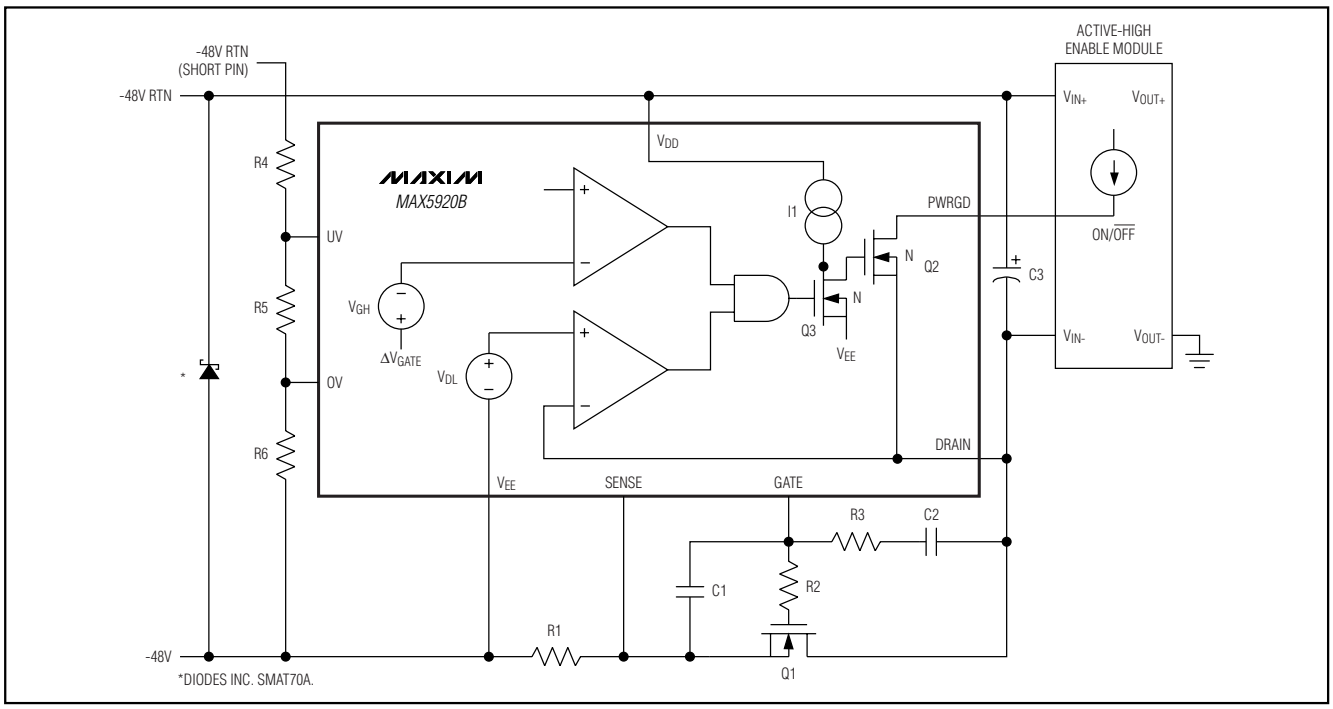

Figure 12. Active-High Enable Module

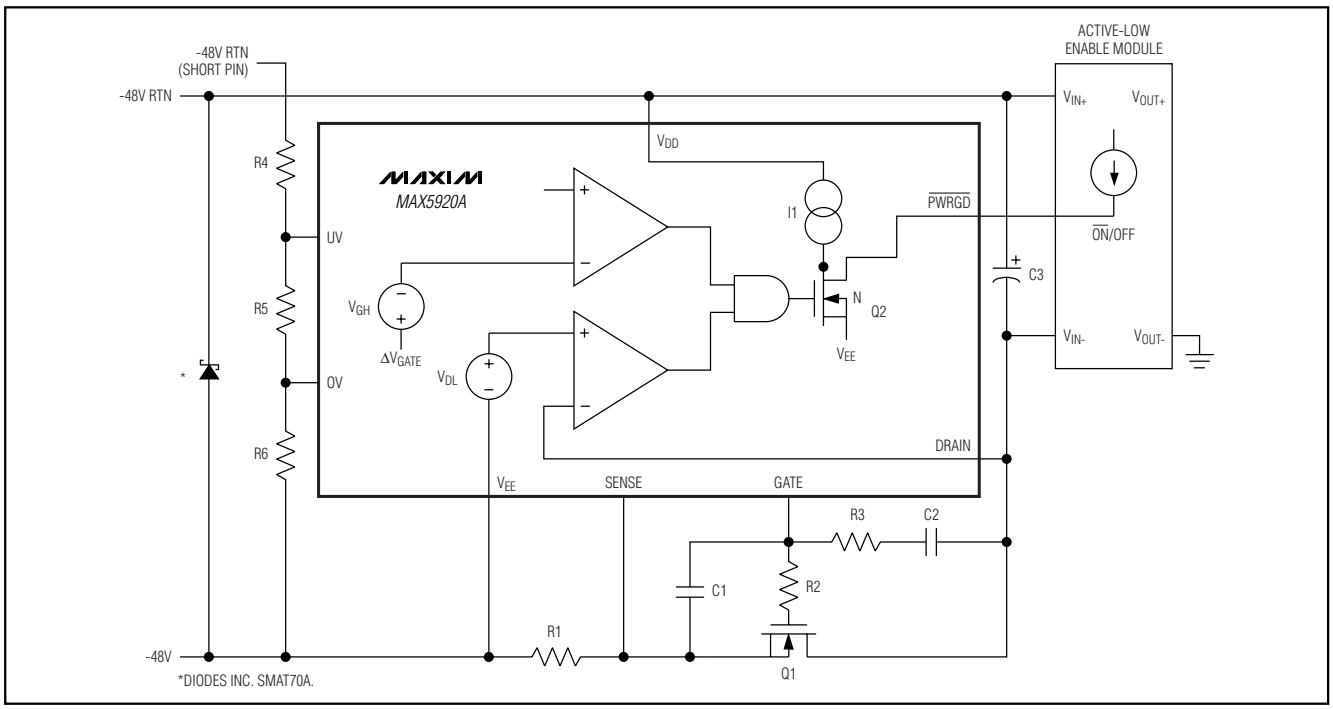

Figure 13. Active-Low Enable Module

-48V Hot-Swap Controller with External RSENSE

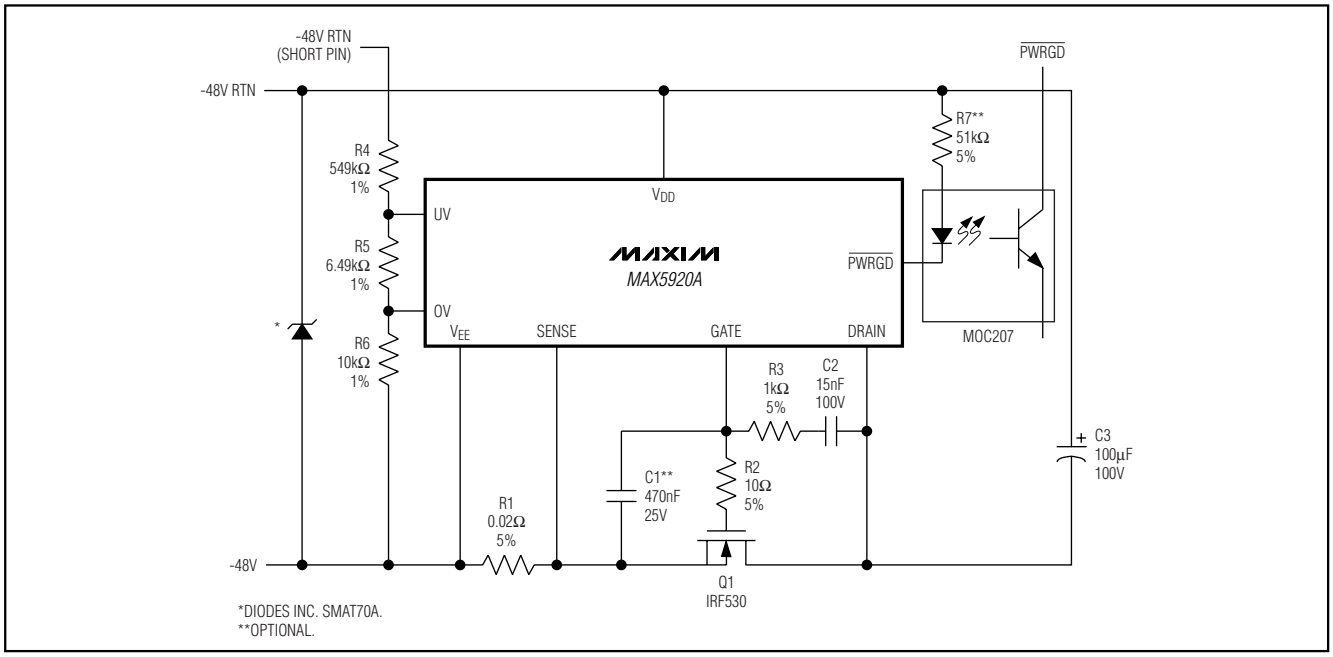

Figure 14. Using $\overline{PWRGD}$ to Drive an Optoisolator

pulled high by the module's internal pullup current source, turning the module off. When the DRAIN voltage drops below V_{DL} and the GATE voltage is greater than ΔV_{GATE} - V_{GH}, Q2 turns on and the $\overline{PWRGD}$ pin pulls low, enabling the module.

The $\overline{PWRGD}$ signal can also be used to turn on an LED or optoisolator to indicate that the power is good (Figure 14) (see the *Component Selection Procedure* section).

When the DRAIN voltage of the MAX5920B is high with respect to V_{EE} (Figure 12) or the GATE voltage is low, the internal MOSFET Q3 is turned off so that I1 and the internal MOSFET Q2 clamp the PWRGD pin to the DRAIN pin. MOSFET Q2 sinks the module's pullup current, and the module turns off.

When the DRAIN voltage drops below V_{DL} and the GATE voltage is greater than ΔV_{GATE} - V_{GH}, MOSFET Q3 turns on, shorting I1 to V_{EE} and turning Q2 off. The pullup current in the module pulls the PWRGD pin high, enabling the module.

GATE Pin Voltage Regulation

The GATE pin goes high when the following startup conditions are met: the UV pin is high, the OV pin is low, the supply voltage is above V_{UVLOH}, and (V_{SENSE} - V_{EE}) is less than 50mV. The gate is pulled up with a 45µA current source and is regulated at 13.5V above V_{EE}. The MAX5920A/MAX5920B include an internal clamp that ensures the GATE voltage of the external MOSFET never exceeds 18V. During a fast-rising V_{DD}, the clamp also keeps the GATE and SENSE potentials as close as possible to prevent the FET from accidentally turning on. When a fault condition is detected, the GATE pin is pulled low with a 50mA current.

Thermal Shutdown

The MAX5920A/MAX5920B include internal die-temperature monitoring. When the die temperature reaches the thermal-shutdown threshold, T_{OT}, the MAX5920A/MAX5920B pull the GATE pin low and turn off the external MOSFET. If a good thermal path is provided between the MOSFET and the MAX5920A/MAX5920B, the device offers thermal protection for the external MOSFET. Placing the MAX5920A/MAX5920B near the drain of the external MOSFET offers the best thermal protection because most of the power is dissipated in its drain.

After a thermal shutdown fault has occurred, the MAX5920A/MAX5920B turn the external FET off. To clear a thermal shutdown fault condition, toggle the UV pin or cycle the power to the device. The device keeps the external FET off for a minimum time of t_{OFF} after UV is toggled, allowing the MOSFET to cool down. The device restarts after the temperature drops 20°C below the thermal-shutdown threshold.

Applications Information

Sense Resistor

The circuit-breaker current-limit threshold is set to 50mV (typically). Select a sense resistor that causes a drop equal to or above the current-limit threshold at a current level above the maximum normal operating current. Typically, set the overload current to 1.5 to 2.0 times the nominal load current plus the load-capacitance charging current during startup. Choose the sense resistor power rating to be greater than $(V_{CL})^2 / R_{SENSE}$.

Component Selection Procedure

- Determine load capacitance:

  C_L = C2 + C3 + module input capacitance

- Determine load current, I_{LOAD}.
- Select circuit-breaker current, for example:

  $$I_{CB} = 2 \times I_{LOAD}$$

- Calculate R_{SENSE}:

  $$R_{SENSE} = \frac{50mV}{I_{CB}}$$

  Realize that I_{CB} varies ±20% due to trip-voltage tolerance.

- Set allowable inrush current:

  $$I_{INRUSH} \le 0.8 \times \frac{40mV}{R_{SENSE}} - I_{LOAD} \text{ or}$$
  $$I_{INRUSH} + I_{LOAD} \le 0.8 \times I_{CB(MIN)}$$

- Determine value of C2:

  $$C_2 = \frac{45\mu A \times C_L}{I_{INRUSH}}$$

- Calculate value of C1:

  $$C_1 = (C_2 + C_{gd}) \times \left(\frac{V_{IN(MAX)} - V_{GS(TH)}}{V_{GS(TH)}} \right)$$

- Determine value of R3:

  $$R_3 \le \frac{150\mu s}{C_2} \text{ (typically } 1k\Omega)$$

- Set R2 = 10Ω.
- If an optocoupler is utilized as in Figure 14, determine the LED series resistor:

  $$R_7 = \frac{V_{IN(NOMINAL)} - 2V}{3mA \le I_{LED} \le 5mA}$$

Although the suggested optocoupler is not specified for operation below 5mA, its performance is adequate for 36V temporary low-line voltage where LED current would then be ≈2.2mA to 3.7mA. If R7 is set as high as 51kΩ, optocoupler operation should be verified over the expected temperature and input voltage range to ensure suitable operation when LED current ≈0.9mA for 48V input and ≈0.7mA for 36V input.

If input transients are expected to momentarily raise the input voltage to >100V, select an input transient-voltage-suppression diode (TVS) to limit maximum voltage on the MAX5920 to less than 100V. A suitable device is the Diodes Inc. SMAT70A telecom-specific TVS.

Select Q1 to meet supply voltage, load current, efficiency, and Q1 package power-dissipation requirements:

$$BV_{DSS} \ge 100V$$

$$I_{D(ON)} \ge 3 \times I_{LOAD}$$

DPAK, D^2PAK, or TO-220AB

The lowest practical $R_{DS(ON)}$, within budget constraints and with values from 14mΩ to 540mΩ, are available at 100V breakdown.

Ensure that the temperature rise of Q1 junction is not excessive at normal load current for the package selected. Ensure that I_{CB} current during voltage transients does not exceed allowable transient-safe operating-area limitations. This is determined from the SOA and transient-thermal-resistance curves in the Q1 manufacturer's data sheet.

Example 1:

I_{LOAD} = 2.5A, efficiency = 98%, then V_{DS} = 0.96V is acceptable, or $R_{DS(ON)} \le 384m\Omega$ at operating temperature is acceptable. An IRL520NS 100V NMOS with $R_{DS(ON)} \le 180m\Omega$ and $I_{D(ON)}$ = 10A is available in D^2PAK. (A Vishay Siliconix SUD40N10-25 100V NMOS with $R_{DS(ON)} \le 25m\Omega$ and $I_{D(ON)}$ = 40A is available in DPAK, but may be more costly because of a larger die size).

Using the IRL520NS, $V_{DS} \le 0.625V$ even at +80°C so efficiency ≥ 98.6% at 80°C. $P_D \le 1.56W$ and junction temperature rise above case temperature would be 5°C due to the package θ_{JC} = 3.1°C/W thermal resistance. Of course, using the SUD40N10-25 would yield an efficiency greater than 99.8% to compensate for the increased cost.

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If I_{CB} is set to twice I_{LOAD}, or 5A, V_{DS} momentarily doubles to ≤ 1.25V. If C_{OUT} = 4000µF, transient-line input voltage is Δ36V, the 5A charging-current pulse is:

$$t = \frac{4000\mu F \times 1.25V}{5A} = 1ms$$

Entering the data sheet transient-thermal-resistance curves at 1ms provides a θJC = 0.9°C/W. P_D = 6.25W, so Δt_{JC} = 5.6°C. Clearly, this is not a problem.

Example 2:

I_{LOAD} = 10A, efficiency = 98%, allowing V_{DS} = 0.96V but $R_{DS(ON)} \le 96m\Omega$. An IRF530 in a D^2PAK exhibits $R_{DS(ON)} \le 90m\Omega$ at +25°C and ≤ 135mΩ at +80°C. Power dissipation is 9.6W at +25°C or 14.4W at +80°C. Junction-to-case thermal resistance is 1.9W/°C, so the junction temperature rise would be approximately 5°C above the +25°C case temperature. For higher efficiency, consider IRL540NS with $R_{DS(ON)} \le 44m\Omega$. This allows η = 99%, $P_D \le 4.4W$, and T_{JC} = +4°C (θ_{JC} = 1.1°C/W) at +25°C.

Thermal calculations for the transient condition yield I_{CB} = 20A, V_{DS} = 1.8V, t = 0.5ms, transient θ_{JC} = 0.12°C/W, P_D = 36W and Δt_{JC} = 4.3°C.

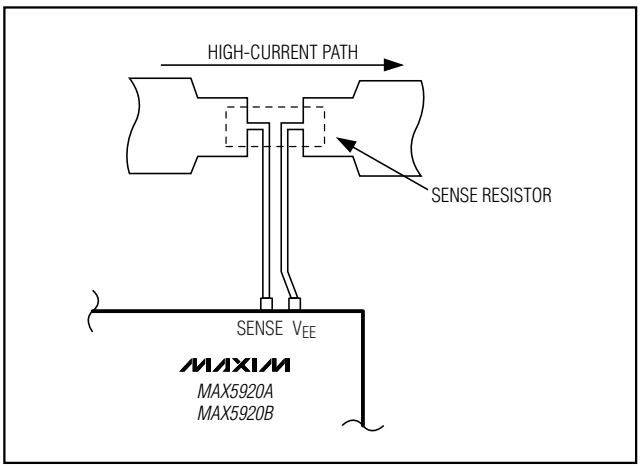


Figure 15. Recommended Layout for Kelvin-Sensing Current Through Sense Resistor

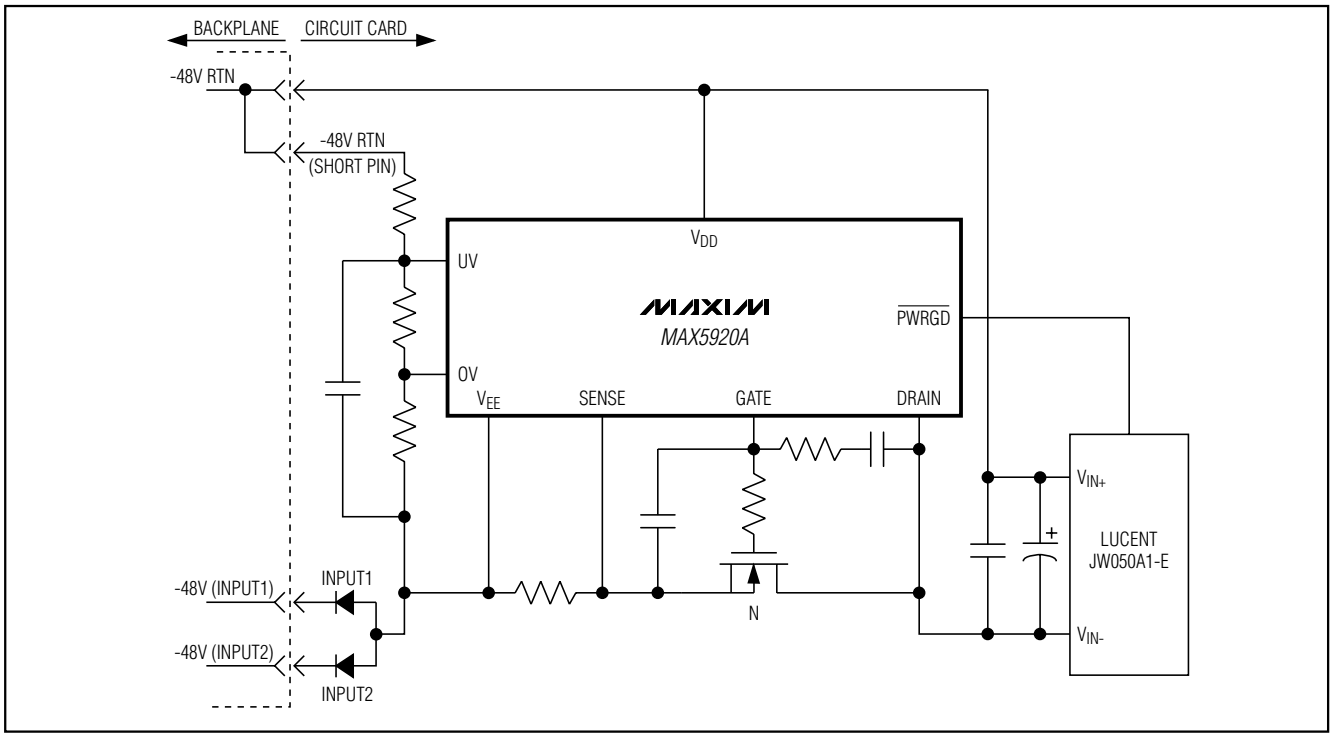
Layout Guidelines

Good thermal contact between the MAX5920A/MAX5920B and the external MOSFET is essential for the thermal-shutdown feature to operate effectively. Place the MAX5920A/MAX5920B as close as possible to the drain of the external MOSFET and use wide circuit-board traces for good heat transfer (see Figure 15).

Selector Guide

PART	PWRGD POLARITY	FAULT MANAGEMENT
MAX5920AESA	Active low ($\overline{PWRGD}$)	Latched
MAX5920BESA	Active high (PWRGD)	Latched

Typical Operating Circuit



Chip Information

TRANSISTOR COUNT: 2645

PROCESS: BiCMOS

-48V Hot-Swap Controller with External RSENSE

Package Information

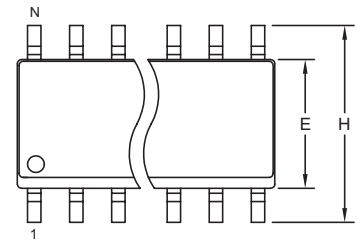
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOICN .EPS

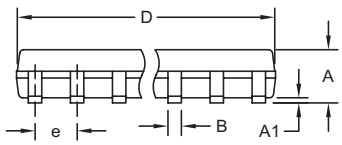
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

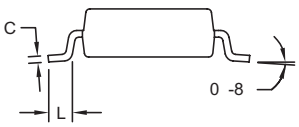
	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



TOP VIEW



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1