Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND)
V+, IN_ .....-0.3V to +6V
COM_, NO_, NC_ (Note 1) .....-0.3V to (V+ + 0.03V)
Continuous Current (any terminal).....±75mA
Peak Current (NO_, NC_, COM_)
(pulsed at 1ms, 10% duty cycle).....±200mA

Continuous Power Dissipation (T_A = +70°C)
14-Pin TSSOP (derate 6.3mW/°C above +70°C) 500mW
14-Pin Narrow SO (derate 8.00mW/°C above +70°C) ..640mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C)...800mW
Operating Temperature Ranges
MAX461_C_ _ .....0°C to +70°C
MAX461_E_ _.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Signals on NO_, NC_, or COM_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, V_{IN_H} = 2.4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range (Note 3)	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			0		V+	V
On-Resistance	R_{ON}	V+ = 4.5V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ = $V_{NC\_}$ = 3V	T_A = +25°C		8	10	Ω
			T_A = T_{MIN} to T_{MAX}			13	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = 4.5V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ = $V_{NC\_}$ = 3V	T_A = +25°C		0.2	1	Ω
			T_A = T_{MIN} to T_{MAX}			1.2	
On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	V+ = 4.5V; $I_{COM\_}$ = 10mA; $V_{NO\_}$ = $V_{NC\_}$ = 3V, 2V, 1V	T_A = +25°C		0.3	1	Ω
			T_A = T_{MIN} to T_{MAX}			1.2	
NO_ or NC_ Off-Leakage Current (Note 6)	$I_{NO(OFF)}$	V+ = 5.5V; $V_{COM\_}$ = 1V, 4.5V; $V_{NO\_}$ = 4.5V, 1V	T_A = +25°C	-1	0.01	1	nA
			T_A = T_{MIN} to T_{MAX}	-6		6	
COM_ Off-Leakage Current (Note 6)	$I_{COM(OFF)}$	V+ = 5.5V; $V_{COM\_}$ = 1V, 4.5V; $V_{NO\_}$ = $V_{NC\_}$ = 4.5V, 1V	T_A = +25°C	-1	0.01	1	nA
			T_A = T_{MIN} to T_{MAX}	-6		6	
COM_ On-Leakage Current (Note 6)	$I_{COM(ON)}$	V+ = 5.5V; $V_{COM\_}$ = 1V, 4.5V; $V_{NO\_}$ = $V_{NC\_}$ = 1V, 4.5V, or floating	T_A = +25°C	-2	0.02	2	nA
			T_A = T_{MIN} to T_{MAX}	-12		12	

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +5V ±10%, V_{IN_H} = 2.4V, V_{IN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUT							
Input Current with Input Voltage High	I_{IN_H}	$V_{IN\_}$ = 2.4V		-10	0.3	10	nA
Input Current with Input Voltage Low	I_{IN_L}	$V_{IN\_}$ = 0.8V		-10	0.3	10	nA
Input Voltage High	V_{IN_H}			2.4			V
Input Voltage Low	V_{IN_L}					0.8	V
SWITCH DYNAMIC							
Turn-On Time (Note 3)	t_{ON}	$V_{COM\_}$ = 3V, Figure 2	T_A = +25°C		5	12	ns
			T_A = T_{MIN} to T_{MAX}			14	
Turn-Off Time (Note 3)	t_{OFF}	$V_{COM\_}$ = 3V, Figure 2	T_A = +25°C		2.5	10	ns
			T_A = T_{MIN} to T_{MAX}			12	
On-Channel Bandwidth	BW	Signal = 0dBm, Figure 4, 50Ω in and out, T_A = +25°C			70		MHz
Charge Injection	Q	Signal = 0dBm, Figure 4, 50Ω in and out, T_A = +25°C			6.5		pC
Off-Isolation (Note 7)	V_{ISO}	R_L = 50Ω, f = 100kHz, Figure 4, T_A = +25°C			-85		dB
Crosstalk (Note 8)	V_{CT}	R_L = 50Ω, f = 100kHz, Figure 5, T_A = +25°C			-96		dB
NO_ or NC_ Capacitance	$C_{(OFF)}$	f = 1MHz, Figure 6, T_A = +25°C			5		pF
COM_ Off-Capacitance	$C_{COM(OFF)}$	f = 1MHz, Figure 6, T_A = +25°C			5		pF
COM_ On-Capacitance	$C_{COM(ON)}$	f = 1MHz, Figure 6, T_A = +25°C			11		pF
Total Harmonic Distortion	THD	600Ω IN and OUT, f = 20Hz to 20kHz, 2Vp-p, T_A = +25°C			0.034		%
POWER SUPPLY							
Power-Supply Range				2		5.5	V
Power-Supply Current	I+	V_{IN} = 0 or V+, all switches on or off		-1	0.001	1	µA

Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches

ELECTRICAL CHARACTERISTICS—Single +3.3V Supply

(V+ = +3.3V ±10%, V_{IN_H} = 2.4V, V_{IN_L} = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range (Note 3)	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			0		V+	V
On-Resistance	R_{ON}	V+ = 3V, I_{NO} = 10mA, $V_{COM\_}$ = 1.5V	T_A = +25°C		8	20	Ω
			T_A = T_{MIN} to T_{MAX}			25	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = 3V, $I_{COM\_}$ = 1mA, $V_{NO\_}$ = $V_{NC\_}$ = 1.5V	T_A = +25°C		0.5	1.5	Ω
			T_A = T_{MIN} to T_{MAX}			2	
NO_ or NC_ Off-Leakage Current (Notes 3, 6)	$I_{NO(OFF)}$	V+ = 3.6V; $V_{COM\_}$ = 1V, 3V; $V_{NO\_}$ = $V_{NC\_}$ = 3V, 1V	T_A = +25°C	-1	0.002	1	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	
COM_ Off-Leakage Current (Notes 3, 6)	$I_{COM(OFF)}$	V+ = 3.6V; $V_{COM\_}$ = 1V, 3V; $V_{NO\_}$ = $V_{NC\_}$ = 3V, 1V	T_A = +25°C	-1	0.002	1	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	
COM_ On-Leakage Current (Notes 3, 6)	$I_{COM(ON)}$	V+ = 3.6V; $V_{COM\_}$ = 1V, 3V; $V_{NO\_}$ = $V_{NC\_}$ = 1V, 3V, or floating	T_A = +25°C	-1	0.002	1	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	
LOGIC INPUT							
Input Current with Input Voltage High	I_{IN_H}	$V_{IN\_}$ = 2V		-10	0.003	10	nA
Input Current with Input Voltage Low	I_{IN_L}	$V_{IN\_}$ = 0.8V		-10	0.003	10	nA
Input Voltage High	V_{IN_H}			2.0			V
Input Voltage Low	V_{IN_L}					0.8	V
SWITCH DYNAMIC (Note 3)							
Turn-On Time	t_{ON}	$V_{COM\_}$ = 1.5V, Figure 2	T_A = +25°C		6	15	ns
			T_A = T_{MIN} to T_{MAX}			20	
Turn-Off Time	t_{OFF}	$V_{COM\_}$ = 1.5V, Figure 2	T_A = +25°C		4	12	ns
			T_A = T_{MIN} to T_{MAX}			15	
Charge Injection	Q	C_L = 1nF, V_{GEN} = 0, R_{GEN} = 0, T_A = +25°C			6.5		pC
POWER SUPPLY							
Power-Supply Current	I+	V+ = 3.6V, V_{IN} = 0 or V+, all channels on or off		-1	0.001	1	µA

ELECTRICAL CHARACTERISTICS—Single +2.5V Supply

(V+ = +2.5V, V_{INH} = 0.7V_{CC}, V_{INL} = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range (Note 3)	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			0		V+	V
COM_ to NO_ or NC_ On-Resistance	R_{ON}	V+ = 2.5V, $I_{COM\_}$ = 10mA, V_{NO} = 1.2V	T_A = +25°C		30	60	Ω
			T_A = T_{MIN} to T_{MAX}			100	
SWITCH DYNAMIC (Note 3)							
Turn-On Time	t_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = 1V, T_A = +25°C			6.5		ns
Turn-Off Time	t_{OFF}	$V_{NO\_}$ or $V_{NC\_}$ = 1V, T_A = +25°C			2.8		ns

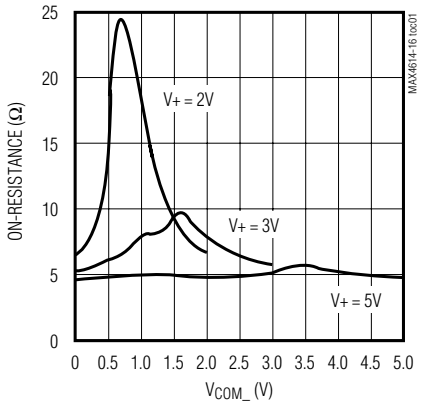
Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.
Note 3: Guaranteed by design.
Note 4: ΔR_{ON} = R_{ON} (max) - R_{ON} (min).
Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
Note 6: Leakage parameters are 100% tested at maximum-rated hot temperature and guaranteed by correlation at +25°C.
Note 7: Off-Isolation = $20\log_{10}$ ($V_{COM\_}$ / $V_{NO\_}$), $V_{COM\_}$ = output, $V_{NO\_}$ = input to off switch.
Note 8: Between any two switches.

Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches

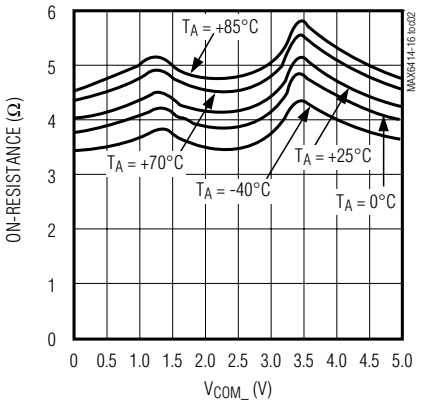
Typical Operating Characteristics

(V+ = +5V, GND = 0, T_A = +25°C, unless otherwise noted.)

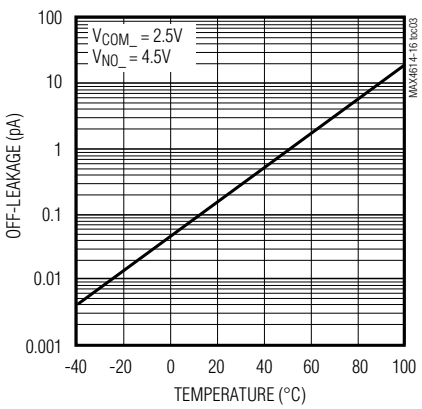
ON-RESISTANCE vs. $V_{COM\_}$



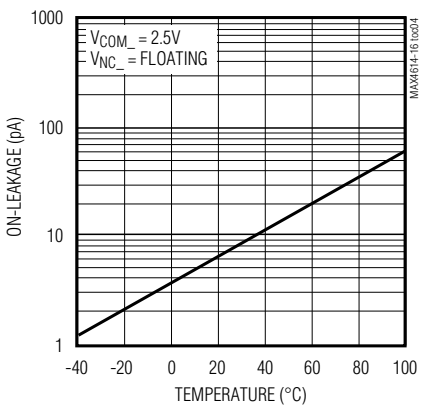
ON-RESISTANCE vs. $V_{COM\_}$ AND TEMPERATURE



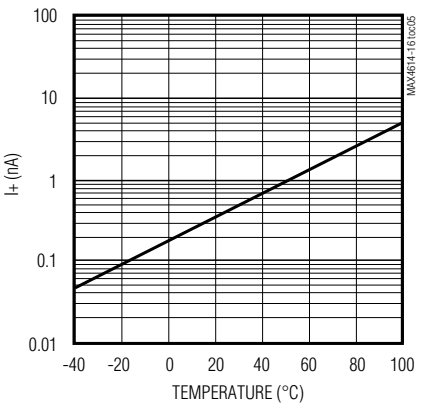
OFF-LEAKAGE vs. TEMPERATURE



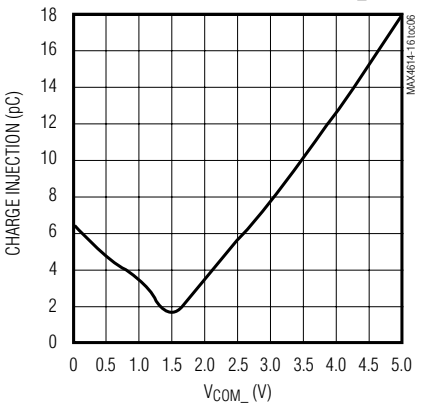
ON-LEAKAGE vs. TEMPERATURE



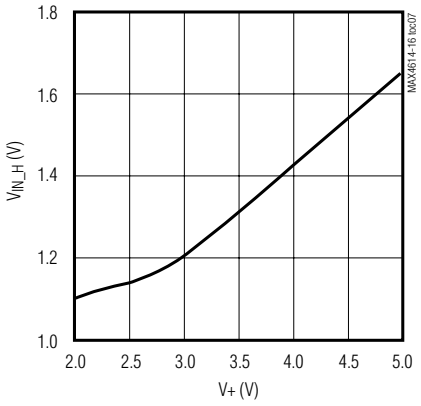
SUPPLY CURRENT vs. TEMPERATURE



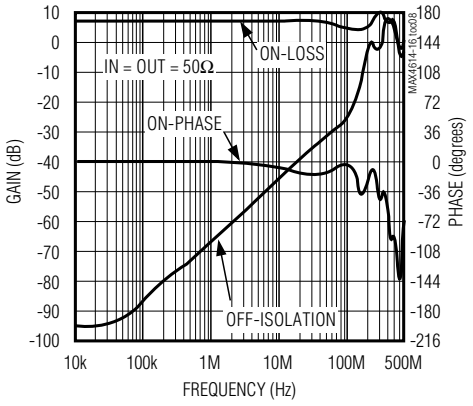
CHARGE INJECTION vs. $V_{COM\_}$



V_{IN_H} INPUT LOGIC HIGH THRESHOLD vs. V+



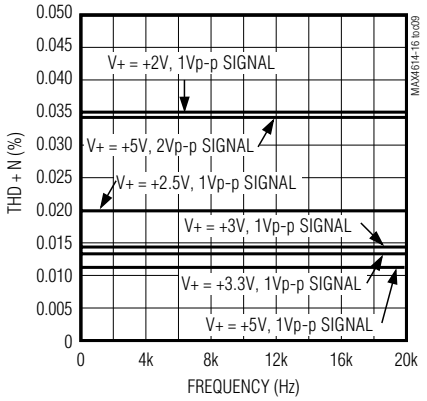
FREQUENCY RESPONSE



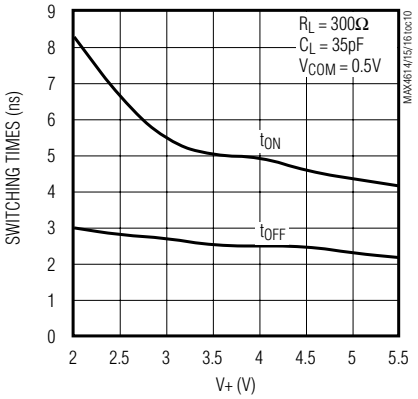
Typical Operating Characteristics (continued)

(V+ = +5V, GND = 0, T_A = +25°C, unless otherwise noted.)

TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



SWITCHING TIME vs. VOLTAGE



Pin Description

PIN			NAME	FUNCTION
MAX4614	MAX4615	MAX4616		
1, 3, 8	—	1, 8	NO1–NO3	Analog Switch Normally Open Terminal (bidirectional)
—	1, 3, 8	—	NC1–NC3	Analog Switch Normally Closed Terminal (bidirectional)
—	—	3	NC2	Analog Switch Normally Closed Terminal (bidirectional)
2, 4, 9, 10	2, 4, 9, 10	2, 4, 9, 10	COM1–COM4	Analog Switch Common Terminal (bidirectional)
5, 6, 12, 13	5, 6, 12, 13	5, 6, 12, 13	IN1–IN4	Logic Control Inputs
7	7	7	GND	Ground
—	11	11	NC4	Analog Switch Normally Closed Terminal (bidirectional)
11			NO4	Analog Switch Normally Open Terminal (bidirectional)
14	14	14	V+	Positive Supply Voltage

Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches

Applications Information

Power-Supply Sequencing and Overvoltage Protection

Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals or logic inputs, especially if the analog or logic signals are not current limited. If this sequencing is not possible, and if the analog or logic inputs are not current limited to 20mA, add a small-signal diode (D1) as shown in Figure 1. If the analog signal can dip below GND, add D2. Adding protection diodes reduces the analog signal range to a diode drop (about 0.7V) below V+ (for D1), and to a diode drop above ground (for D2). Leakage is unaffected by adding the diodes. On-resistance increases by a small amount at low supply voltages. Maximum supply voltage (V+) must not exceed 6V.

Adding protection diodes causes the logic thresholds to be shifted relative to the power-supply rails. This can be significant when low supply voltages (+5V or less) are used. With a +5V supply, TTL compatibility is not guaranteed when protection diodes are added. Driving IN1 and IN2 all the way to the supply rails (i.e., to a diode drop higher than the V+ pin, or to a diode drop lower than the GND pin) is always acceptable.

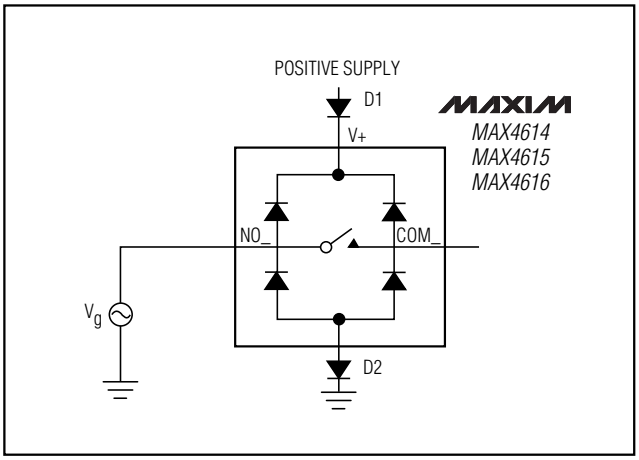


Figure 1. Overvoltage Protection Using Two External Blocking Diodes

Protection diodes D1 and D2 also protect against some overvoltage situations. With Figure 1's circuit, if the supply voltage is below the absolute maximum rating, and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin, no damage will result.

Test Circuits/Timing Diagrams

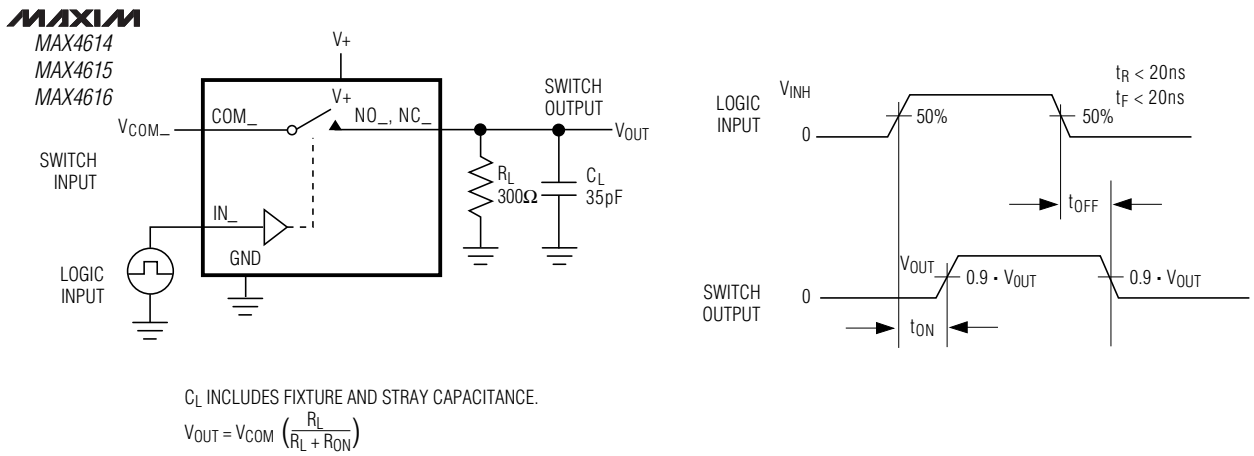


Figure 2. Switching Time

Test Circuits/Timing Diagrams (continued)

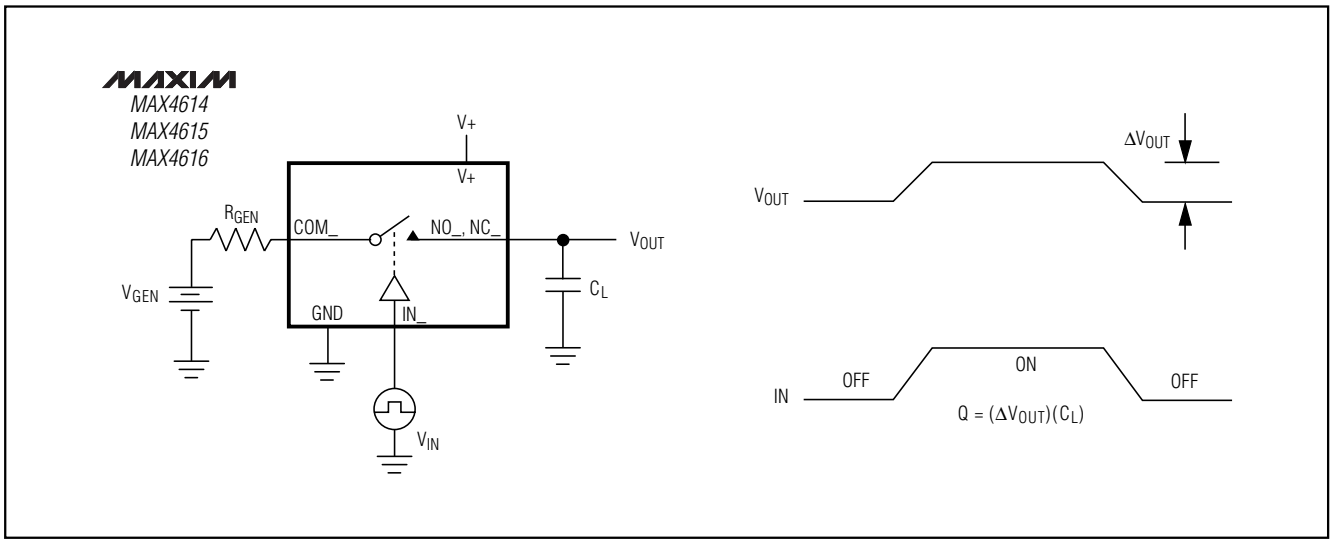


Figure 3. Charge Injection

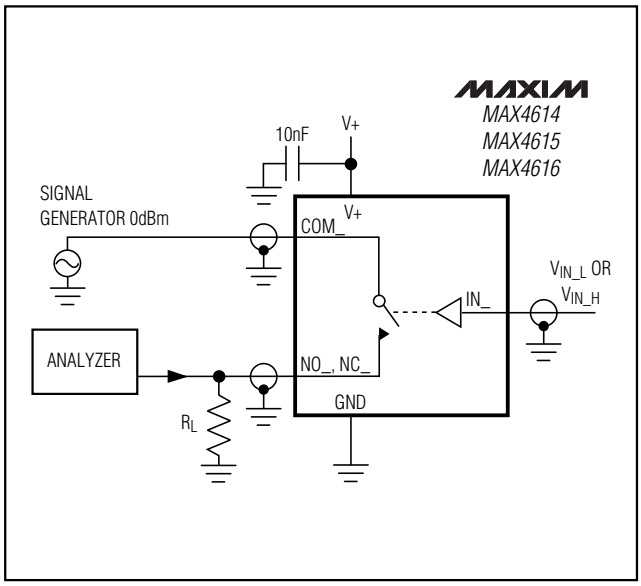


Figure 4. Off-Isolation/On-Channel Bandwidth

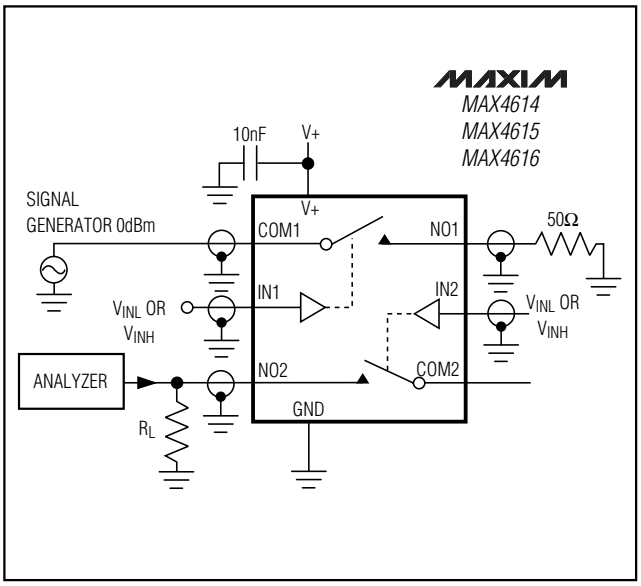


Figure 5. Crosstalk

Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches

Test Circuits/Timing Diagrams (continued)

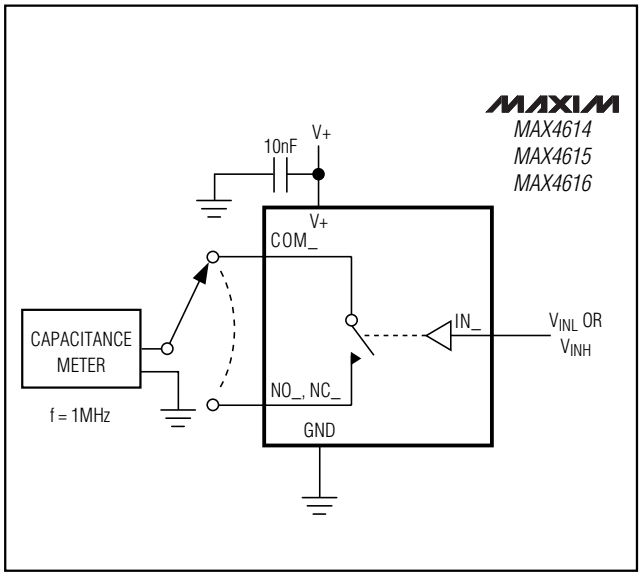


Figure 6. Channel Off/On-Capacitance

Ordering Information (continued)

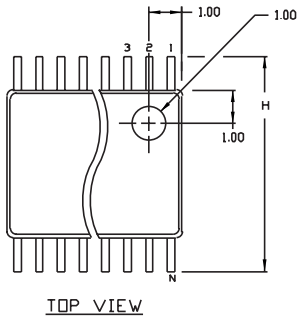
PART	TEMP. RANGE	PIN-PACKAGE
MAX4615CUD	0°C to +70°C	14 TSSOP
MAX4615CSD	0°C to +70°C	14 Narrow SO
MAX4615CPD	0°C to +70°C	14 Plastic DIP
MAX4615EUD	-40°C to +85°C	14 TSSOP
MAX4615ESD	-40°C to +85°C	14 Narrow SO
MAX4615EPD	-40°C to +85°C	14 Plastic DIP
MAX4616CUD	0°C to +70°C	14 TSSOP
MAX4616CSD	0°C to +70°C	14 Narrow SO
MAX4616CPD	0°C to +70°C	14 Plastic DIP
MAX4616EUD	-40°C to +85°C	14 TSSOP
MAX4616ESD	-40°C to +85°C	14 Narrow SO
MAX4616EPD	-40°C to +85°C	14 Plastic DIP

Chip Information

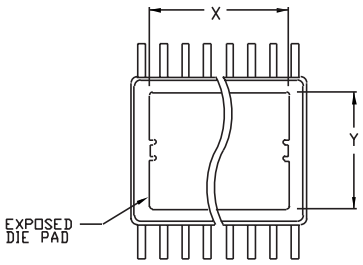
TRANSISTOR COUNT: 89

Package Information

TSSOP.EPS

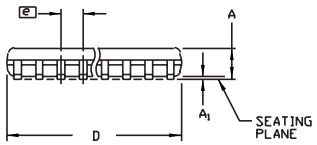


TOP VIEW

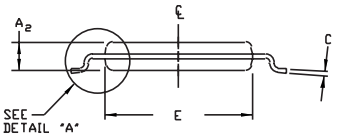


BOTTOM VIEW

SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	.112	.124
α	0°	8°	0°	8°

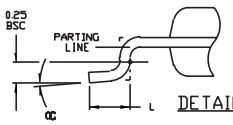


SIDE VIEW

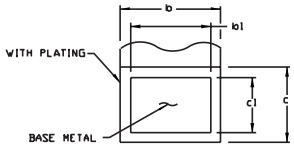


END VIEW

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB	14	D	4.90	5.10	.193	.201
AC	16	D	4.90	5.10	.193	.201
AC-EP	16	D	4.90	5.10	.193	.201
		X	2.85	3.15	.112	.124
AD	20	D	6.40	6.60	.252	.260
AD-EP	20	D	6.40	6.60	.252	.260
		X	4.00	4.34	.157	.171
AE	24	D	7.70	7.90	.303	.311
AF	28	D	9.60	9.80	.378	.386
AF-EP		D	9.60	9.80	.378	.386
		X	5.35	5.65	.211	.222



DETAIL 'A'



LEAD TIP DETAIL

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC OUTLINE MO-153 VARIATIONS AB, AC, AD, AE, AF.
5. DIMENSIONS X AND Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

MAXIM

PROPRIETARY INFORMATION

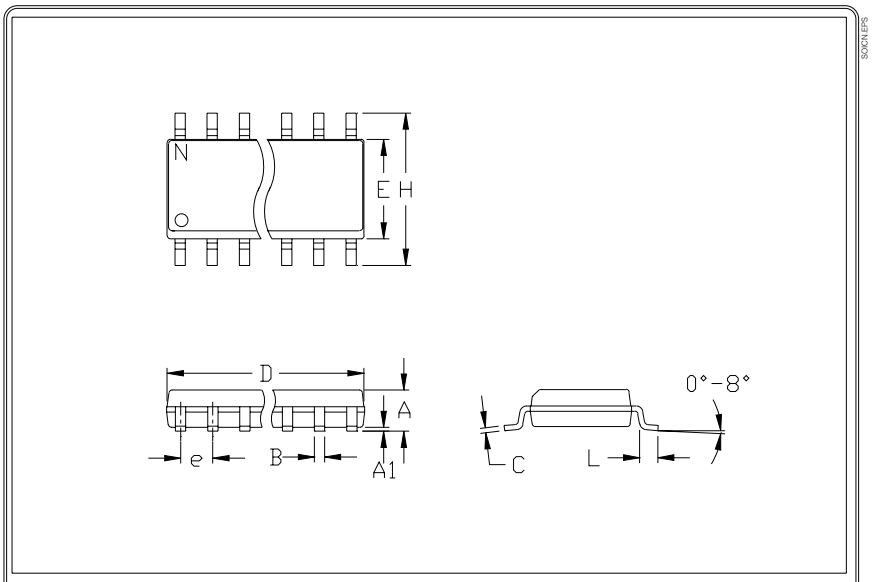
TITLE:

PACKAGE OUTLINE, TSSOP, 4.40mm BODY, 0.65mm PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0066	C	1/1

Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION

TITLE: PACKAGE FAMILY OUTLINE: SOIC .150" | 1/1 | 21-0041 A DOCUMENT CONTROL NUMBER REV