### **ABSOLUTE MAXIMUM RATINGS**

V <sub>CC</sub> , OUT to GND	0.3V to +6V
IN+, IN-, BIAS, SHDN to GND	
Output Short Circuit (OUT+ to OUT-) (I	Note 1)Continuous
Continuous Power Dissipation (T <sub>A</sub> = +	70°C)
8-Pin µMAX (derate 4.8mW/°C above	e +70°C)
8-Pin TDFN (derate 24.4mW/°C abov	ve +70°Ć)1951mW

Junction Temperature	+150°C
Operating Temperature Range	40°C to +85°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SO

### PACKAGE THERMAL CHARACTERISTICS (Note 2)

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a fourlayer board. For detailed information on package thermal considerations, refer to <u>www.maxim-ic.com/thermal-tutorial</u>.

### **ELECTRICAL CHARACTERISTICS—5V**

(V<sub>CC</sub> = 5V, R<sub>L</sub> = ∞, C<sub>BIAS</sub> = 1µF to GND, V<sub>SHDN</sub> = V<sub>GND</sub>, T<sub>A</sub> = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDI	MIN	TYP	MAX	UNITS	
Supply Voltage Range	VCC	Inferred from PSRR tes	2.7		5.5	V	
		MAX4364 MAX4364, T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			7	13	
Cuerche Current						17	
Supply Current	lcc	(Note 4) MAX43	65		5	8	mA
		MAX43	65, $T_A = T_{MIN}$ to $T_{MAX}$			11	
Shutdown Supply Current	ISHDN	V <sub>SHDN</sub> = V <sub>CC</sub>			0.01	4	μA
SHDN Threshold	Mu .	$T_A = +25^{\circ}C$					
	VIH	T <sub>A</sub> = -40°C to +85°C (Note 5)	o +85°C				
	VIL	$T_A = +25^{\circ}C$				V <sub>CC</sub> x 0.3	V
		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$ (Note 5)				V <sub>CC</sub> x 0.3	
Common-Mode Bias Voltage	VBIAS	(Note 6)		V <sub>CC</sub> /2 - 5%	V <sub>CC</sub> /2	V <sub>CC</sub> /2 + 5%	V
Output Offset Voltage	Vos	IN- = OUT+, IN+ = BIAS (Note 7)			±1	±10	mV
		$V_{CC} = 2.7V \text{ to } 5.5V$	DC	55	75		
Power-Supply Rejection Ratio	PSRR	$\begin{array}{c} \text{PSRR} & V_{\text{RIPPLE}} = 200 \text{mV}_{\text{P-P}}, & 217 \text{Hz} \\ \text{R}_{\text{L}} = 8 \Omega & 1 \text{kHz} \end{array}$	217Hz		68		dB
			1kHz		58		
Output Power	Pout	$R_{\rm L} = 8\Omega$ , THD+N = 1%, MAX43	, MAX4364	1200	1400		m)//
Oulpul Fower		f <sub>IN</sub> = 1kHz (Note 8) MAX4365		800	1000		mW

### ELECTRICAL CHARACTERISTICS—5V (continued)

(V<sub>CC</sub> = 5V, R<sub>L</sub> =  $\infty$ , C<sub>BIAS</sub> = 1µF to GND, V<sub>SHDN</sub> = V<sub>GND</sub>, T<sub>A</sub> = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS			TYP	MAX	UNITS	
Total Harmonic Distortion Plus Noise	THD+N	rtion Plus $\Delta v = -2V/V B_1 = 80$ POUT	MAX4364, P <sub>OUT</sub> = 1W		0.04		~ %	
	THD+N	f <sub>IN</sub> = 1kHz (Notes 5, 9)	MAX4365, P <sub>OUT</sub> = 750mW		0.1		70	
Noise		$f_{IN} = 10$ kHz, BW = 22Hz t	o 22kHz		12		μV <sub>RMS</sub>	
Short-Circuit Current	ISC	OUT+ to OUT- (Note 10)			600		mA	
Thermal Shutdown Threshold					160		°C	
Thermal Shutdown Hysteresis					15		°C	
		$T_A = +25^{\circ}C$			50			
Power-Up Time	tpu	$C_{BIAS} = 0.22 \mu F$ , $T_A = -40$ (Note 5)	°C to +85°C		14	35	ms	
Shutdown Time	<b>t</b> SHDN				10		μs	
		$T_A = +25^{\circ}C$			50			
Enable Time from Shutdown	<sup>t</sup> ENABLE	C <sub>BIAS</sub> = 0.22µF, T <sub>A</sub> = -40 (Note 5)	°C to +85°C		12	35	ms	

### **ELECTRICAL CHARACTERISTICS—3V**

 $(V_{CC} = 3V, R_L = \infty, C_{BIAS} = 1\mu F$  to GND,  $V_{SHDN} = V_{GND}, T_A = +25^{\circ}C$ , unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	ТҮР	МАХ	UNITS
Quere la Quere et	Icc	(Note 4)	MAX4364		6		mA
Supply Current		(11018 4)	MAX4365		4.5		
Shutdown Supply Current	ISHDN	$V_{SHDN} = V_{CC}$			10		nA
Output Power	Роит	R <sub>L</sub> = 8Ω, THD+N = 1%, f <sub>IN</sub> = 1kHz	MAX4364	400	500		mW
		(Note 8)	MAX4365	350	450		
Total Harmonic Distortion Plus Noise	armonic Distortion Plus THD + N	$A_V = -2V/V, R_L = 8\Omega,$	MAX4364, P <sub>OUT</sub> = 400mW	0.05	0(		
		$\label{eq:relation} \begin{split} A_V &= -2V/V, \ R_L = 8\Omega, \\ f_{IN} &= 1 \text{kHz} \ (\text{Notes 5}, 9) \end{split}$	MAX4365, P <sub>OUT</sub> = 400mW		0.08		%

**Note 3:** All specifications are 100% tested at  $T_A = +25^{\circ}C$ .

**Note 4:** Quiescent power-supply current is specified and tested with no load on the outputs. Quiescent power-supply current depends on the offset voltage when a practical load is connected to the amplifier.

**Note 5:** Guaranteed by design, not production tested.

Note 6: Common-mode bias voltage is the voltage on BIAS and is nominally  $V_{CC}/2$ .

Note 7: Maximum differential-output offset voltage is tested in a unity-gain configuration.  $V_{OS} = V_{OUT+} - V_{OUT-}$ .

Note 8: Output power is specified by a combination of a functional output-current test, and characterization analysis.

**Note 9:** Measurement bandwidth for THD+N is 22Hz to 22kHz.

Note 10: Extended short-circuit conditions result in a pulsed output.



MAX4364/MAX4365

### **Typical Operating Characteristics (continued)**

 $(V_{CC} = 5V, THD+N \text{ measurement bandwidth} = 22Hz \text{ to } 22kHz, T_A = +25^{\circ}C, \text{ unless otherwise noted.})$ 





MAX4364/MAX4365

### **Typical Operating Characteristics (continued)**

 $(V_{CC} = 5V, THD+N \text{ measurement bandwidth} = 22Hz \text{ to } 22kHz, T_A = +25^{\circ}C, \text{ unless otherwise noted.})$ 



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MAX4364/MAX4365



### **Pin Description**

P	PIN		
MAX4364 MAX4365		NAME	FUNCTION
SO	µMAX/TDFN		
1	7	SHDN	Active-High Shutdown. Connect SHDN to GND for normal operation.
2	1	BIAS	DC Bias Bypass. See BIAS Capacitor section for capacitor selection. Connect $C_{BIAS}$ capacitor from BIAS to GND.
3	2	IN+	Noninverting Input
4	4	IN-	Inverting Input
5	5	OUT+	Bridged Amplifier Positive Output
6	6	V <sub>CC</sub>	Power Supply
7	3	GND	Ground
8	8	OUT-	Bridged Amplifier Negative Output
	_	EP	Exposed Pad (TDFN Only). Internally connected to GND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.
	1		

### **Detailed Description**

The MAX4364/MAX4365 bridged audio power amplifiers can deliver 1.4W into  $8\Omega$  (MAX4364) or 1W into  $8\Omega$ (MAX4365) while operating from a single 5V supply. These devices consist of two high-output-current op amps configured as a bridge-tied load (BTL) amplifier (see Typical Application Circuit/Functional Diagram). The gain of the device is set by the closed-loop gain of the input op amp. The output of the first amplifier serves as the input to the second amplifier, which is configured as an inverting unity-gain follower in both devices. This results in two outputs, identical in magnitude, but 180° out of phase.

BIAS The MAX4364/MAX4365 feature an internally generated common-mode bias voltage of V<sub>CC</sub>/2 referenced to GND. BIAS provides both click-and-pop suppression and the DC bias level for the audio signal. BIAS is internally connected to the noninverting input of one amplifier, and should be connected to the noninverting input of the other amplifier for proper signal biasing (see Typical Application Circuit/Functional Diagram). Choose the value of the bypass capacitor as described in the BIAS Capacitor section.

The MAX4364/MAX4365 feature a 10nA. low-power shutdown mode that reduces guiescent current consumption. Pulling SHDN high disables the device's bias circuitry, the amplifier outputs go high impedance, and BIAS is driven to GND. Connect SHDN to GND for normal operation.

**Current Limit** The MAX4364/MAX4365 feature a current limit that protects the device during output short circuit and overload conditions. When both amplifier outputs are shorted to either V<sub>CC</sub> or GND, the short-circuit protection is enabled and the amplifier enters a pulsing mode, reducing the average output current to a safe level. The amplifier remains in this mode until the overload or short-circuit condition is removed.

### **Applications Information**

#### **Bridge-Tied Load**

The MAX4364/MAX4365 are designed to drive a load differentially in a BTL configuration. The BTL configuration (Figure 1) offers advantages over the single-ended configuration, where one side of the load is connected to ground. Driving the load differentially doubles the output voltage compared to a single-ended amplifier under similar conditions. Thus, the differential gain of

#### Shutdown



+1 VOUT(P-P) 2 x VOUT(P-P) -1 VOUT(P-P)

Figure 1. Bridge-Tied Load Configuration

the device is twice the closed-loop gain of the input amplifier. The effective gain is given by:

$$A_{VD} = 2 \times \frac{R_F}{R_{IN}}$$

Substituting  $2 \times V_{OUT(P-P)}$  into the following equations yields four times the output power due to doubling of the output voltage.

$$V_{RMS} = \frac{V_{OUT(P-P)}}{2\sqrt{2}}$$
$$P_{OUT} = \frac{V_{RMS}^{2}}{R_{I}}$$

Since the differential outputs are biased at midsupply, there is no net DC voltage across the load. This eliminates the need for DC-blocking capacitors required for single-ended amplifiers. These capacitors can be large. expensive, consume board space, and degrade low-frequency performance.

### **Power Dissipation**

Under normal operating conditions, the MAX4364/ MAX4365 can dissipate a significant amount of power. The maximum power dissipation for each package is given in the Absolute Maximum Ratings section under Continuous Power Dissipation or can be calculated by the following equation:

$$P_{\text{DISSPKG}(\text{MAX})} = \frac{T_{\text{J}(\text{MAX})} - T_{\text{A}}}{\theta_{\text{JA}}}$$

where T<sub>J(MAX)</sub> is +150°C, T<sub>A</sub> is the ambient temperature and  $\theta_{JA}$  is the reciprocal of the derating factor in °C/W as specified in the Package Thermal Characteristics section. For example,  $\theta_{JA}$  of the  $\mu$ MAX package is 206.3°C/W.

The increase in power delivered by the BTL configuration directly results in an increase in internal power dissipation over the single-ended configuration. The maximum power dissipation for a given  $V_{CC}$  and load is given by the following equation:

$$P_{\text{DISS}(\text{MAX})} = \frac{2V_{\text{CC}}^2}{\pi^2 R_1}$$

If the power dissipation for a given application exceeds the maximum allowed for a given package, reduce  $V_{CC}$ , increase load impedance, decrease the ambient temperature or add heat sinking to the device. Large output, supply, and ground PC board traces improve the maximum power dissipation in the package.

Thermal-overload protection limits total power dissipation in the MAX4364/MAX4365. When the junction temperature exceeds +160°C, the thermal protection circuitry disables the amplifier output stage. The amplifiers are enabled once the junction temperature cools by 15°C. This results in a pulsing output under continuous thermal overload conditions as the device heats and cools.

The MAX4365 TDFN package features an exposed thermal pad on its underside. This pad lowers the thermal resistance of the package by providing a direct heat conduction path from the die to the PC board. Connect the exposed thermal pad to circuit ground by using a large pad, ground plane, or multiple vias to the ground plane.

**Efficiency** The efficiency of the MAX4364/MAX4365 is calculated by taking the ratio of the power delivered to the load to the power consumed from the power supply. Output power is calculated by the following equations:

$$P_{OUT} = \frac{V_{PEAK}^2}{2R_I}$$

where VPEAK is half the peak-to-peak output voltage. In BTL amplifiers, the supply current waveform is a fullwave rectified sinusoid with the magnitude proportional to the peak output voltage and load. Calculate the supply current and power drawn from the power supply by the following:

$$I_{CC} = \frac{2V_{PEAK}}{\pi R_{I}}$$

 $P_{IN} = V_{CC} \left( \frac{2V_{PEAK}}{\pi R_L} \right)$ 

The efficiency of the MAX4364/MAX4365 is:

$$\eta = \frac{P_{OUT}}{P_{N}} = \frac{\pi \sqrt{\frac{P_{OUT}R_{L}}{2}}}{2V_{CC}}$$

The device efficiency values in Table 1 are calculated based on the previous equation and do include the effects of quiescent current. Note that efficiency is low at low output-power levels, but remains relatively constant at normal operating, output-power levels.

#### **Component Selection**

#### **Gain-Setting Resistors**

External feedback components set the gain of both devices. Resistors R<sub>F</sub> and R<sub>IN</sub> (see *Typical Application Circuit/Functional Diagram*) set the gain of the amplifier as follows:

$$A_{VD} = 2 \times \frac{R_F}{R_{IN}}$$

Optimum output offset is achieved when  $R_F = 20k\Omega$ . Vary the gain by changing the value of  $R_{IN}$ . When using the MAX4364/MAX4365 in a high-gain configuration (greater than 8V/V), a feedback capacitor may be required to maintain stability (see Figure 2).  $C_F$  and  $R_F$ limit the bandwidth of the device, preventing high-frequency oscillations. Ensure that the pole created by  $C_F$ and  $R_F$  is not within the frequency band of interest.

#### Input Filter

The input capacitor ( $C_{IN}$ ), in conjunction with  $R_{IN}$  forms a highpass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming zero source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{\rm IN} C_{\rm IN}}$$

Choose  $R_{IN}$  according to the *Gain-Setting Resistors* section. Choose  $C_{IN}$  such that  $f_{-3dB}$  is well below the lowest frequency of interest. Setting  $f_{-3dB}$  too high affects the low-frequency response of the amplifier. Use capacitors whose dielectrics have low-voltage coeffi-





Figure 2. High-Gain Configuration

OUTPUT POWER (W)	INTERNAL POWER DISSIPATION (W)	EFFICIENCY (%)
0.25	0.55	31.4
0.50	0.63	44.4
0.75	0.63	54.4
1.00	0.59	62.8
1.25	0.53	70.2
1.40	0.48	74.3

#### Table 1. Efficiency in a 5V, 8Ω BTL System

cients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in an increase distortion at low frequencies.

Other considerations when designing the input filter include the constraints of the overall system, the actual frequency band of interest and click-and-pop suppression. Although high-fidelity audio calls for a flat gain response between 20Hz and 20kHz, portable voicereproduction devices such as cellular phones and twoway radios need only concentrate on the frequency range of the spoken human voice (typically 300Hz to 3.5kHz). In addition, speakers used in portable devices typically have a poor response below 150Hz. Taking these two factors into consideration, the input filter may not need to be designed for a 20Hz to 20kHz response, saving both board space and cost due to the use of smaller capacitors.

#### **BIAS Capacitor**

The BIAS bypass capacitor,  $C_{BIAS}$ , improves PSRR and THD+N by reducing power-supply noise at the commonmode bias node, and serves as the primary click-andpop suppression mechanism.  $C_{BIAS}$  is fed from an internal 25k $\Omega$  source, and controls the rate at which the common-mode bias voltage rises at startup and falls during shutdown. For optimum click-and-pop suppression, ensure that the input capacitor ( $C_{IN}$ ) is fully charged (ten time constants) before  $C_{BIAS}$ . The value of  $C_{BIAS}$  for best click-and-pop suppression is given by:

$$C_{\text{BIAS}} \ge 10 \left[ \frac{C_{\text{IN}} R_{\text{IN}}}{25 k \Omega} \right]$$

In addition, a larger CBIAS value yields higher PSRR.



#### Clickless/Popless Operation

Proper selection of AC-coupling capacitors (C<sub>IN</sub>) and C<sub>BIAS</sub> achieves clickless/popless shutdown and startup. The value of C<sub>BIAS</sub> determines the rate at which the midrail bias voltage rises on startup and falls when entering shutdown. The size of the input capacitor also affects clickless/popless operation. On startup, C<sub>IN</sub> is charged to its quiescent DC voltage through the feedback resistor (R<sub>F</sub>) from the output. This current creates a voltage transient at the amplifier's output, which can result in an audible pop. Minimizing the size of C<sub>IN</sub> reduces this effect, optimizing click-and-pop suppression.

#### Supply Bypassing

Proper supply bypassing ensures low-noise, low-distortion performance. Place a  $0.1\mu$ F ceramic capacitor in parallel with a  $10\mu$ F ceramic capacitor from V<sub>CC</sub> to GND. Locate the bypass capacitors as close to the device as possible.

#### **Adding Volume Control**

The addition of a digital potentiometer provides simple volume control. Figure 3 shows the MAX4364/MAX4365 with the MAX5407 log taper digital potentiometer used as an input attenuator. Connect the high terminal of the MAX5407 to the audio input, the low terminal to ground and the wiper to  $C_{IN}$ . Setting the wiper to the top posi-



Figure 3. MAX4364/MAX4365 and MAX5160 Volume Control Circuit

tion passes the audio signal unattenuated. Setting the wiper to the lowest position fully attenuates the input.

#### Layout Considerations

Good layout improves performance by decreasing the amount of stray capacitance and noise at the amplifier's inputs and outputs. Decrease stray capacitance by minimizing PC board trace lengths, using surface-mount components and placing external components as close to the device as possible. Also refer to the *Power Dissipation* section for heatsinking considerations.

### **Chip Information**

PROCESS: BICMOS



## **Package Information**

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SO	S8+5	<u>21-0041</u>	<u>90-0096</u>
8 µMAX	U8+1	<u>21-0036</u>	<u>90-0092</u>
8 TDFN	T833+2	<u>21-0137</u>	<u>90-0059</u>



### **Revision History**

REVISION	REVISION	DESCRIPTION	PAGES
NUMBER	DATE		CHANGED
4	5/11	Added EP information to <i>Pin Description</i> ; updated <i>Ordering Information</i> and <i>Pin Configurations</i> for lead-free parts; updated specifications in <i>Absolute Maximum Ratings</i> , <i>Package Thermal Characteristics</i> and <i>Electrical Characteristics</i> sections	1, 2, 3, 8, 9, 12, 13

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