

Low-Capacitance, 2/3/4/6-Channel, $\pm 15\text{kV}$ ESD Protection Arrays for High-Speed Data Interfaces

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND -0.3V to +7.0V
 I/O_{-} to GND -0.3V to (V_{CC} + 0.3V)
 Continuous Power Dissipation (T_A = +70°C)
 2 × 2 WLP (derate 11.5mW/°C above +70°C).....920mW
 3 × 2 WLP (derate 12.3mW/°C above +70°C).....984mW
 3 × 3 WLP (derate 14.1mW/°C above +70°C).....1128mW

6-Pin TDFN (derate 24.4mW/°C above +70°C)1951mW
 12-Pin TQFN (derate 16.9mW/°C above +70°C)1349mW
 Operating Temperature Range-40°C to +85°C
 Storage Temperature Range-65°C to +150°C
 Junction Temperature+150°C
 Lead Temperature (soldering, 10s)+300°C
 Soldering Temperature (reflow)+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

4 WLP
 Junction-to-Ambient Thermal Resistance (θ_{JA}).....87°C/W
 6 WLP
 Junction-to-Ambient Thermal Resistance (θ_{JA}).....84°C/W
 9 WLP
 Junction-to-Ambient Thermal Resistance (θ_{JA}).....71°C/W

6 TDFN
 Junction-to-Ambient Thermal Resistance (θ_{JA}).....42°C/W
 Junction-to-Case Thermal Resistance (θ_{JC}).....9°C/W
 12 TQFN
 Junction-to-Ambient Thermal Resistance (θ_{JA}).....41°C/W
 Junction-to-Case Thermal Resistance (θ_{JC}).....6°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V $\pm 5\%$, T_A = T_{MIN} to T_{MAX} , unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|----------|---|------|----------|----------------|-------|
| Supply Voltage | V_{CC} | | 0.9 | | 5.5 | V |
| Supply Current | I_{CC} | | | 1 | 100 | nA |
| Diode Forward Voltage | V_F | I_F = 10mA | 0.65 | | 0.95 | V |
| Channel Clamp Voltage (Note 3) | V_C | T_A = +25°C, $\pm 15\text{kV}$ Human Body Model, I_F = 10A | | | $V_{CC} + 25$ | V |
| | | Negative transients | | | -25 | |
| | | T_A = +25°C, $\pm 8\text{kV}$ Contact Discharge (IEC 61000-4-2), I_F = 24A | | | $V_{CC} + 60$ | |
| | | Negative transients | | | -60 | |
| | | T_A = +25°C, $\pm 15\text{kV}$ Air-Gap Discharge (IEC 61000-4-2), I_F = 45A | | | $V_{CC} + 100$ | |
| | | Negative transients | | | -100 | |
| Channel Leakage Current | | T_A = 0°C to +50°C (Note 4) | -1 | | +1 | nA |
| Channel Input Capacitance | | V_{CC} = 5V, bias of $V_{CC}/2$ | | 5 | 7 | pF |
| ESD PROTECTION | | | | | | |
| Human Body Model | | | | ± 15 | | kV |
| IEC 61000-4-2 Contact Discharge | | | | ± 8 | | kV |
| IEC 61000-4-2 Air-Gap Discharge | | | | ± 15 | | kV |

Note 2: Limits over temperature are guaranteed by design, not production tested.

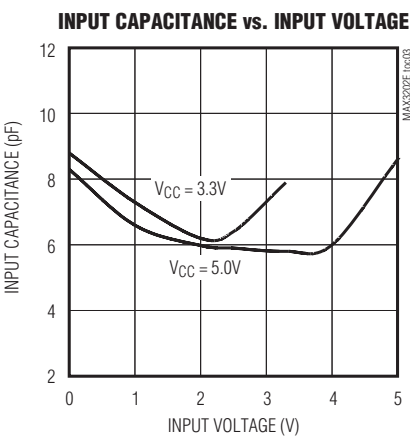
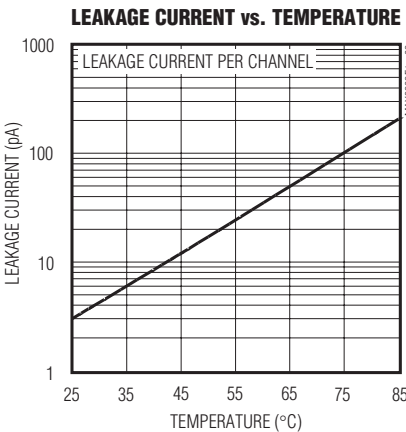
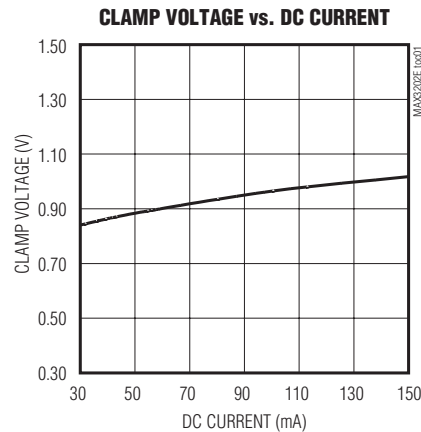
Note 3: Idealized clamp voltages ($L1 = L2 = L3 = 0$) (Figure 1); see the *Applications Information* section for more information.

Note 4: Guaranteed by design. Not production tested.

Low-Capacitance, 2/3/4/6-Channel, $\pm 15\text{kV}$ ESD Protection Arrays for High-Speed Data Interfaces

Typical Operating Characteristics

($V_{CC} = +5\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



Pin/Bump Description

| PIN/BUMP | | | | | | | | NAME | FUNCTION |
|----------|---------|------------|---------|----------------|------------|------------------------|------------------|------------------|---|
| MAX3202E | | MAX3203E | | MAX3204E | | MAX3206E | | | |
| WLP | TDFN-EP | WLP | TDFN-EP | WLP | TDFN-EP | WLP | TQFN-EP | | |
| A1, B2 | 3, 6 | A1, A2, B3 | 1, 2, 4 | A1, A2, B2, B3 | 1, 2, 4, 5 | A1, A3, B1, B3, C1, C3 | 1, 2, 3, 7, 8, 9 | I/O _— | ESD-Protected Channel |
| A2 | 4 | B1 | 3 | B1 | 3 | A2 | 5 | GND | Ground |
| B1 | 1 | A3 | 6 | A3 | 6 | C2 | 11 | V _{CC} | Power-Supply Input. Bypass V _{CC} to GND with a 0.1µF ceramic capacitor. |
| — | 2, 5 | — | 5 | — | — | — | 4, 6, 10, 12 | N.C. | No Connection. Not internally connected. |
| — | — | — | — | — | — | — | — | EP | Exposed Pad. Connect to GND. Only for TDFN and TQFN packages. |

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Detailed Description

The MAX3202E/MAX3203E/MAX3204E/MAX3206E are diode arrays designed to protect sensitive electronics against damage resulting from ESD conditions or transient voltages. The low input capacitance makes these devices ideal for high-speed data lines. The MAX3202E, MAX3203E, MAX3204E, and MAX3206E protect two, three, four, and six channels, respectively.

The MAX3202E/MAX3203E/MAX3204E/MAX3206E are designed to work in conjunction with a device's intrinsic ESD protection. The MAX3202E/MAX3203E/MAX3204E/MAX3206E limit the excursion of the ESD event to below $\pm 25\text{V}$ peak voltage when subjected to the Human Body Model waveform. When subjected to the IEC 61000-4-2 waveform, the peak voltage is limited to $\pm 60\text{V}$ when subjected to Contact Discharge and $\pm 100\text{V}$ when subjected to Air-Gap Discharge. The device that is being protected by the MAX3202E/MAX3203E/MAX3204E/MAX3206E must be able to withstand these peak voltages plus any additional voltage generated by the parasitic board.

Applications Information

Design Considerations

Maximum protection against ESD damage results from proper board layout (see the *Layout Recommendations* section and Figure 2). A good layout reduces the parasitic series inductance on the ground line, supply line, and protected signal lines.

The MAX3202E/MAX3203E/MAX3204E/MAX3206E ESD diodes clamp the voltage on the protected lines during an ESD event and shunt the current to GND or V_{CC} . In an ideal circuit, the clamping voltage, V_C , is defined as the forward voltage drop, V_F , of the protection diode plus any supply voltage present on the cathode.

For positive ESD pulses:

$$V_C = V_{CC} + V_F$$

For negative ESD pulses:

$$V_C = -V_F$$

In reality, the effect of the parasitic series inductance on the lines must also be considered (Figure 1).

For positive ESD pulses:

$$V_C = V_{CC} + V_{F(D1)} + \left(L1 \times \frac{d(I_{ESD})}{dt} \right) + \left(L2 \times \frac{d(I_{ESD})}{dt} \right)$$

For negative ESD pulses:

$$V_C = - \left(V_{F(D2)} + \left(L1 \times \frac{d(I_{ESD})}{dt} \right) + \left(L3 \times \frac{d(I_{ESD})}{dt} \right) \right)$$

where I_{ESD} is the ESD current pulse.

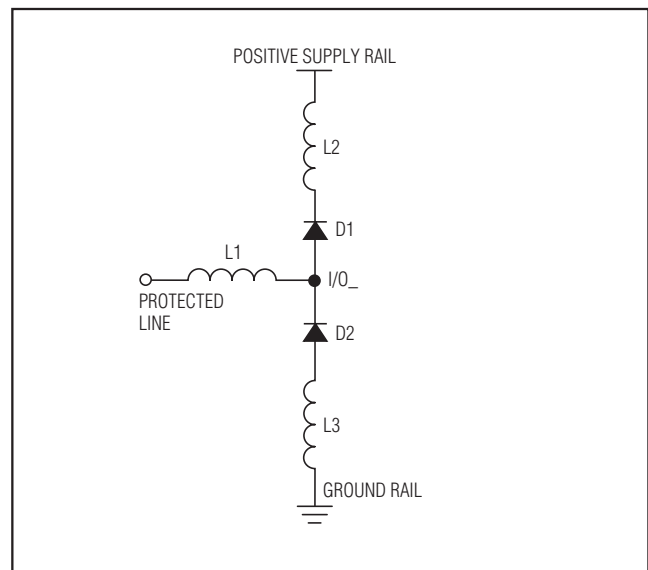


Figure 1. Parasitic Series Inductance

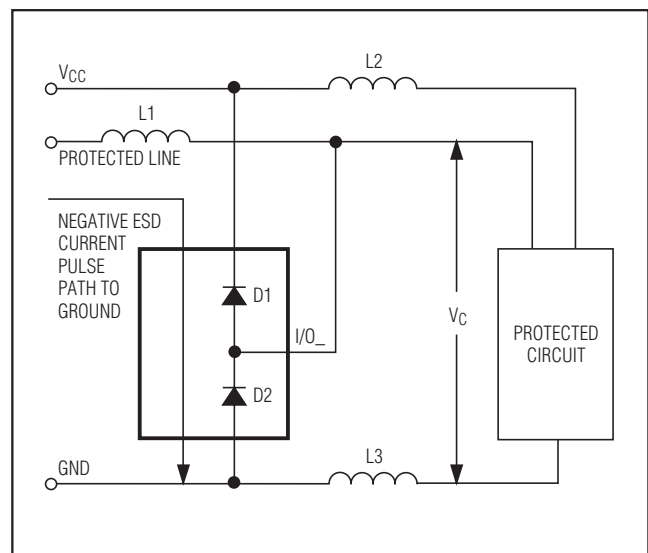


Figure 2. Layout Considerations

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During an ESD event, the current pulse rises from zero to peak value in nanoseconds (Figure 3). For example, in a 15kV IEC-61000 Air-Gap Discharge ESD event, the pulse current rises to approximately 45A in 1ns ($di/dt = 45 \times 10^9$). An inductance of only 10nH adds an additional 450V to the clamp voltage. An inductance of 10nH represents approximately 0.5in of board trace. Regardless of the device's specified diode clamp voltage, a poor layout with parasitic inductance significantly increases the effective clamp voltage at the protected signal line.

A low-ESR 0.1 μF capacitor must be used between V_{CC} and GND. This bypass capacitor absorbs the charge transferred by an +8kV IEC-61000 Contact Discharge ESD event.

Ideally, the supply rail (V_{CC}) would absorb the charge caused by a positive ESD strike without changing its regulated value. In reality, all power supplies have an effective output impedance on their positive rails. If a power supply's effective output impedance is 1 Ω , then by using $V = I \times R$, the clamping voltage of V_C increases by the equation $V_C = I_{ESD} \times R_{OUT}$. An +8kV IEC 61000-4-2 ESD event generates a current spike of 24A, so the clamping voltage increases by $V_C = 24\text{A} \times 1\Omega$, or $V_C = 24\text{V}$. Again, a poor layout without proper bypassing increases the clamping voltage. A ceramic chip capacitor mounted as close to the MAX3202E/MAX3203E/MAX3204E/MAX3206E V_{CC} pin is the best choice for this application. A bypass capacitor should also be placed as close to the protected device as possible.

$\pm 15\text{kV}$ ESD Protection

ESD protection can be tested in various ways; the MAX3202E/MAX3203E/MAX3204E/MAX3206E are characterized for protection to the following limits:

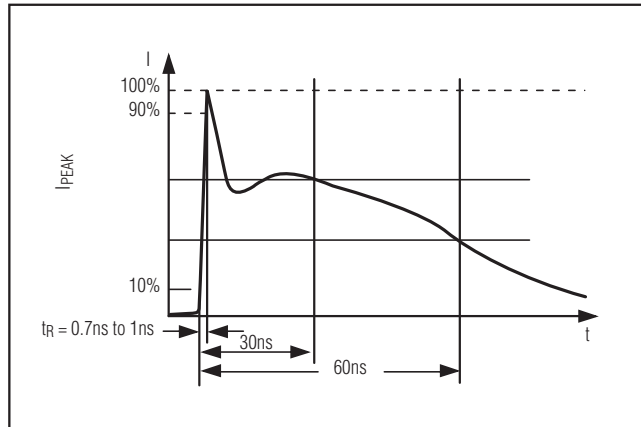


Figure 3. IEC 61000-4-2 ESD Generator Current Waveform

- $\pm 15\text{kV}$ using the Human Body Model
- $\pm 8\text{kV}$ using the Contact Discharge method specified in IEC 61000-4-2
- $\pm 15\text{kV}$ using the IEC 61000-4-2 Air-Gap Discharge method

ESD Test Conditions

ESD performance depends on a number of conditions. Contact Maxim for a reliability report that documents test setup, methodology, and results.

Human Body Model

Figure 4 shows the Human Body Model, and Figure 5 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5k Ω resistor.

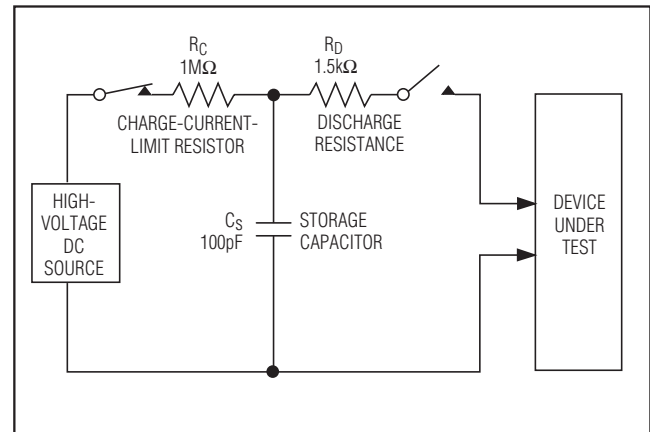


Figure 4. Human Body ESD Test Model

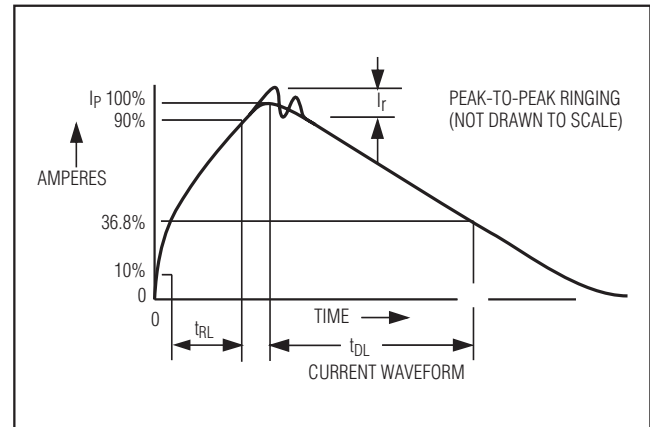


Figure 5. Human Body Model Current Waveform

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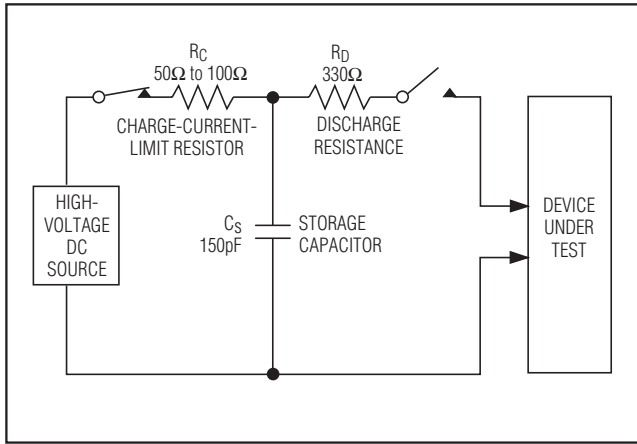


Figure 6. IEC 61000-4-2 ESD Test Model

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. The MAX3202E/MAX3203E/MAX3204E/MAX3206E help users design equipment that meets Level 4 of IEC 61000-4-2.

The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 6) the ESD-withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 3 shows the current waveform for the $\pm 8\text{kV}$ IEC 61000-4-2 Level 4 ESD Contact Discharge test.

The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

Layout Recommendations

Proper circuit-board layout is critical to suppress ESD-induced line transients. The MAX3202E/MAX3203E/MAX3204E/MAX3206E clamp to 100V; however, with improper layout, the voltage spike at the device is much higher. A lead inductance of 10nH with a 45A current spike at a dv/dt of 1ns results in an **ADDITIONAL** 450V spike on the protected line. It is **essential** that the layout of the PC board follows these guidelines:

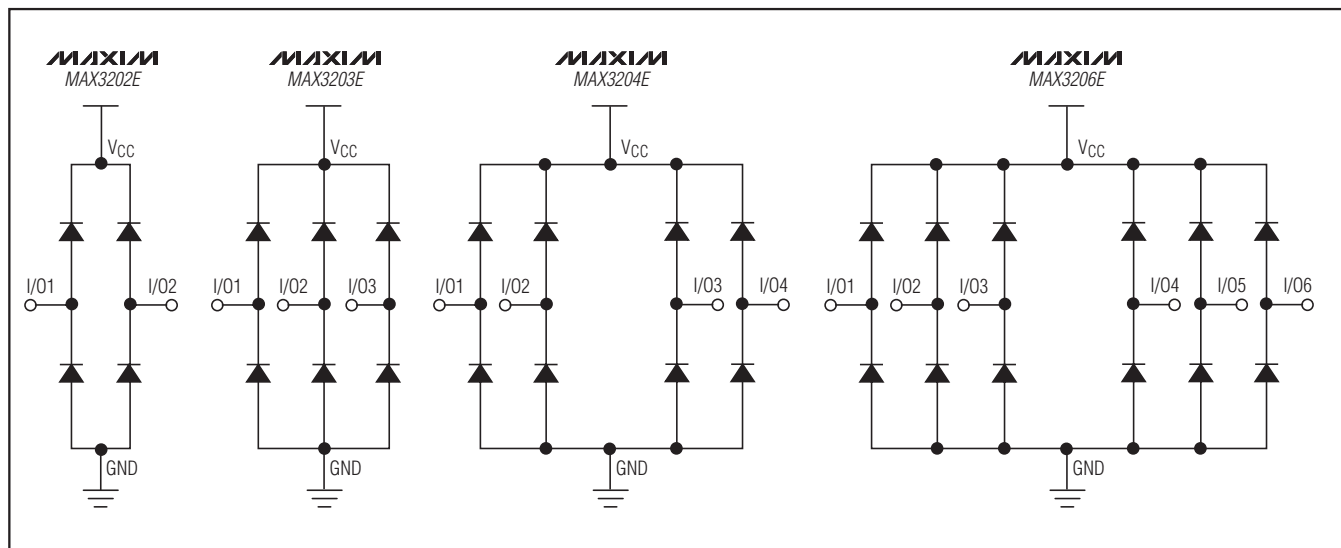
- 1) Minimize trace length between the connector or input terminal, I/O_, and the protected signal line.
- 2) Use separate planes for power and ground to reduce parasitic inductance and to reduce the impedance to the power rails for shunted ESD current.
- 3) Ensure short ESD transient return paths to GND and VCC.
- 4) Minimize conductive power and ground loops.
- 5) Do not place critical signals near the edge of the PC board.
- 6) Bypass VCC to GND with a low-ESR ceramic capacitor as close to VCC as possible.
- 7) Bypass the supply of the protected device to GND with a low-ESR ceramic capacitor as close to the supply pin as possible.

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Table 1. Reliability Test Data

| TEST | CONDITIONS | DURATION | FAILURES PER SAMPLE SIZE |
|---------------------------------|---------------------------------------|---------------------------|--------------------------|
| Temperature Cycle | -35°C to +85°C, -40°C to +100°C | 150 cycles, 900 cycles | 0/10, 0/200 |
| Operating Life | $T_A = +70^\circ\text{C}$ | 240hr | 0/10 |
| Moisture Resistance | -20°C to +60°C, 90% RH | 240hr | 0/10 |
| Low-Temperature Storage | -20°C | 240hr | 0/10 |
| Low-Temperature Operational | -10°C | 24hr | 0/10 |
| Solderability | 8hr steam age | — | 0/15 |
| ESD | $\pm 2000\text{V}$, Human Body Model | — | 0/5 |
| High-Temperature Operating Life | $T_J = +150^\circ\text{C}$ | 168hr | 0/45 |

Functional Diagrams

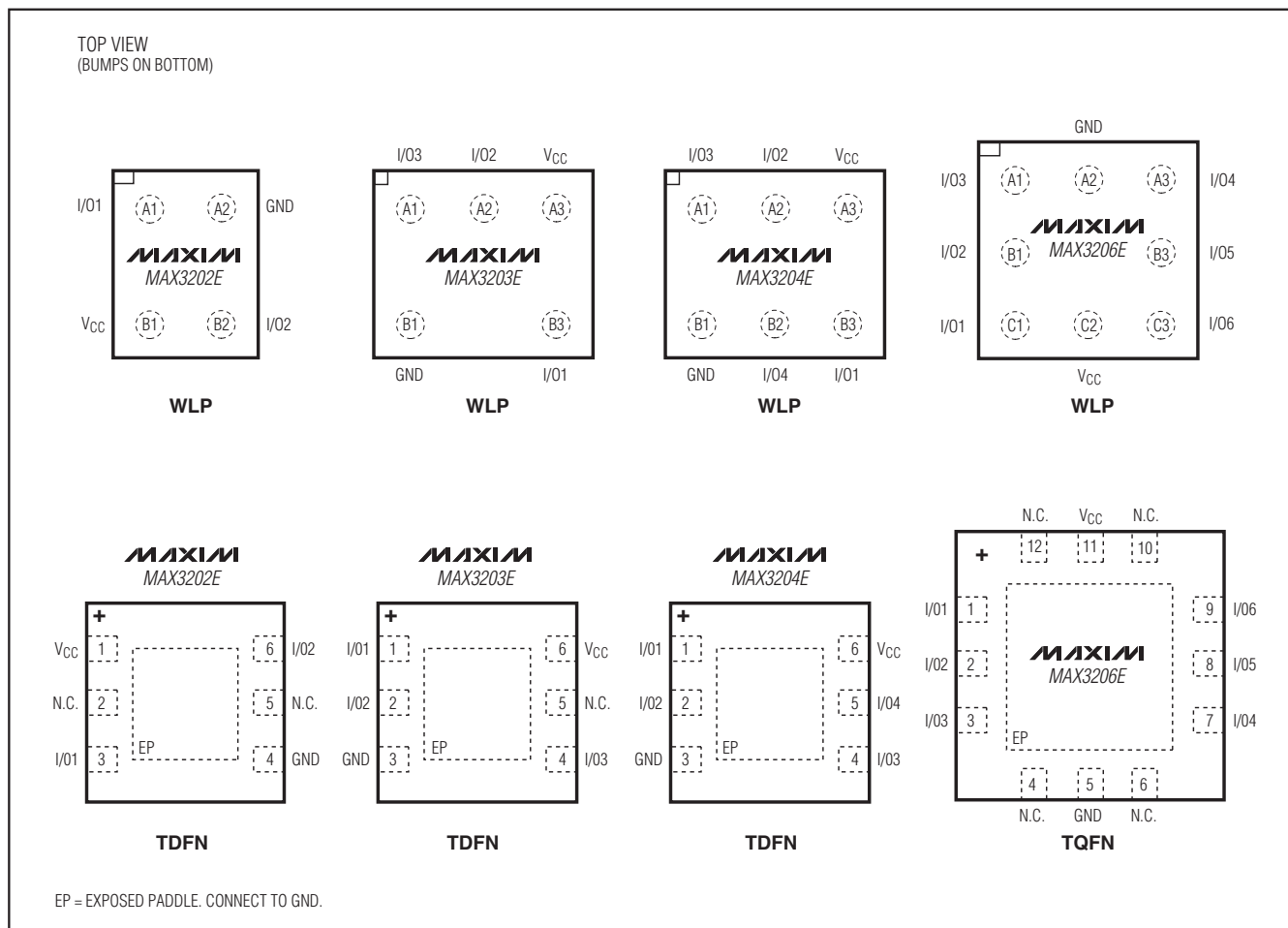


Chip Information

PROCESS: BiCMOS

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Pin Configurations



Package Information

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------------------|--|
| 4 WLP | W41A1+2 | 21-0455 | Refer to Application Note 1891 |
| 6 WLP | W61C1+2 | 21-0463 | Refer to Application Note 1891 |
| 9 WLP | W91B1+5 | 21-0067 | Refer to Application Note 1891 |
| 6 TDFN-EP | T633+2 | 21-0137 | 90-0058 |
| 12 TQFN-EP | T1244+4 | 21-0139 | 90-0068 |

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Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|--|-------------------------|
| 3 | 12/07 | Added 3202EEWS+T TDFN and TQFN packages, updated Package Information | 1, 2, 3, 4, 6, 8, 12–15 |
| 4 | 12/09 | Corrected part numbers and pin packages in the <i>Ordering Information</i> table, <i>Absolute Maximum Ratings</i> , <i>Selector Guide</i> , <i>Pin Description</i> , and <i>Pin Configurations</i> . | 1–3, 8–15 |
| 5 | 6/11 | Updated to show available packages as WLP, not UCSP | 1, 2, 3, 6, 8 |

MAX3202E/MAX3203E/MAX3204E/MAX3206E

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Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600 9

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