ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC}, S5V, H0, V0, SDA0, SCL0, $\overline{ENU}$, $\overline{ENV}$, SDA1, SCL1, USB1, USB2, $\overline{MD}$, $\overline{F1}$, $\overline{F2}$ (Note 1) .....-0.3V to +6V
R0, G0, B0, R1, G1, B1, H1, V1 .....-0.3V to V_{CC} + 0.3V
Continuous Current Out of USB1, USB2.....500mA
Continuous Current Out of S5V.....60mA
Continuous Current Through all I/O Pins ..... ±50mA
Peak Current Through RGB, DDC Switches (1ms Pulse, 10% Duty Cycle)..... ±100mA

Continuous Power Dissipation (T_A = +70C)
TQFN (derate 27.8mW/°C above +70C).....2222.2mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

PACKAGE THERMAL CHARACTERISTICS (Note 2)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....36°C/W
Junction-to-Case Resistance (θ_{JA}) .....3°C/W

Note 1: When $\overline{F1}$ and $\overline{F2}$ are connected to a voltage higher than V_{CC}, some current will be sinked (see the *Detailed Description*).
Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 5.0V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
Supply Voltage	V_{CC}		4.75		5.25	V
Supply Current	I_{CC}	V_{CC} = +5.25V, $V_{\overline{ENV}}$ = $V_{\overline{ENU}}$ = 0V, SCL0 and SDA0 not connected		2.3	5	mA
		V_{CC} = +5.25V, $V_{\overline{ENV}}$ = $V_{\overline{ENU}}$ = 0V, V_{SCL0} = V_{SDA0} = 0V		6.6	10	
Shutdown Supply Current	I_{SHDN}	V_{CC} = +5.25V, $V_{\overline{ENV}}$ = $V_{\overline{ENU}}$ = V_{CC}		29	100	µA
5-VOLT SWITCH (S5V)						
Voltage Drop	V_{S5V}	I_{OUT} = 55mA		135	300	mV
Reverse Leakage Current	I_L	V_{S5V} = +5.25V, V_{CC} = 0V, $V_{\overline{ENV}}$ = 0V			10	µA
Current Limit	I_{LIM}		55	305	500	mA
USB SWITCHES (USB1, USB2)						
Voltage Drop	V_{USB}	I_{OUT} = 500mA			250	mV
Continuous Load Current	I_{LOAD}		500			mA
Current-Limit Threshold	I_{LIM}		0.5		1.0	A
Current-Limit Blanking Period	t_{BLANK}	(Note 4)	7.5		50	ms
Output Rise Time	t_R	R_L = 10Ω, C_L = 1µF, 10%–90%, Figure 1		11.6		µs
Output Fall Time	t_F	R_L = 10Ω, C_L = 1µF, 90%–10%, Figure 1		25.2		µs
Turn-On Delay	t_{ON}	R_L = 10Ω, C_L = 1µF, to 10% of V_{OUT}, Figure 1			100	µs
Turn-Off Delay	t_{OFF}	R_L = 10Ω, C_L = 1µF, to 90% of V_{OUT}, Figure 1			100	µs
Reverse Leakage Current	I_{LUSB}	V_{USB} = 5.25V, V_{CC} = 0V, $V_{\overline{ENU}}$ = 0V			10	µA
Pulldown Resistance					1200	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5.0V ± 5%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 5.0V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
DDC SWITCHES (SDA0, SCL0, SDA1, SCL1)						
SDA1/SCL1 Off-Leakage Current	I_{OFF}	$V_{\overline{ENV}}$ = V_{CC}, V_{SDA1} = V_{SCL1} = 0V or 5.25V	-1		+1	µA
SDA0/SCL0 Off-Leakage Current	I_{LDDC}	V_{CC} = 0V, 3.3kΩ pullup to +3.3V on SDA0 and SCL0			10	µA
On-Resistance	R_{ONDDC}	V_{IN} = +0.8V, I_{IN} = ±10mA		7		Ω
LOGIC INPUTS (H0, V0, $\overline{ENV}$, $\overline{ENU}$)						
Input Logic-Low	V_{IL}		0.8			V
Input Logic-High	V_{IH}				2.0	V
Input Leakage Current	I_L	V_{IN} = 0V or 5.25V	-1		+1	µA
Input Hysteresis (H0, V0)	V_{HYST}			100		mV
PUSH-PULL LOGIC OUTPUTS (H1, V1)						
Output Logic-Low	V_{OL}	I_{SINK} = 8mA, V_{CC} = +4.75V			0.5	V
Output Logic-High	V_{OH}	I_{SOURCE} = 8mA, V_{CC} = +4.75V	2.4			V
Rise/Fall Time	t_R, t_F	10% to 90%, R_L = 2.2kΩ, C_L = 10pF		2.1		ns
OPEN-DRAIN LOGIC OUTPUTS ($\overline{F1}$, $\overline{F2}$, $\overline{MD}$)						
Output Leakage Current	I_{LKG}	Output not asserted, V_{IN} = 5.25V			1	µA
Output Logic-Low	V_{OL}	I_{SINK} = 1mA			0.3	V
RGB ANALOG SWITCHES (R0, G0, B0, R1, G1, B1)						
Bandwidth	f_{MAX}	R_S = R_L = 50Ω		1000		MHz
On-Loss	I_{LOSS}	f = 50MHz, R_S = R_L = 50Ω, 0V ≤ V_{IN} ≤ +0.7V, Figure 2		0.4		dB
On-Resistance	R_{ON}	V_{IN} = +0.7V, I_{IN} = ±10mA		5	8	Ω
On-Resistance Matching	ΔR_{ON}	0V ≤ V_{IN} ≤ +0.7V, I_{IN} = ±10mA, same device			1	Ω
On-Resistance Flatness	$R_{FLAT(ON)}$	0V ≤ V_{IN} ≤ +0.7V, I_{IN} = ±10mA		0.25	1	Ω
On-Capacitance	C_{ON}	f = 1MHz, switches enabled		6		pF
Off-Capacitance	C_{OFF}	f = 1MHz, switches disabled		2		pF
PROTECTION SPECIFICATIONS						
High-ESD Pins ESD Protection		Human Body Model (Note 5)		±8		kV
All Other Pins ESD Protection		Human Body Model (Note 6)		±2		kV
Thermal-Shutdown Threshold	T_{SHDN}			+155		°C
Thermal-Shutdown Hysteresis	T_{SHDN_HYS}			25		°C

Note 3: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 4: t_{BLANK} is the period between detecting an overcurrent condition and the fault output asserting.
Note 5: See the *Pin Description* section for the ESD status of each pin.
Note 6: Terminal tested vs. GND. Apply 1µF-bypass capacitors on V_{CC}, USB1, USB2, and S5V.

Test Circuits/Timing Diagrams

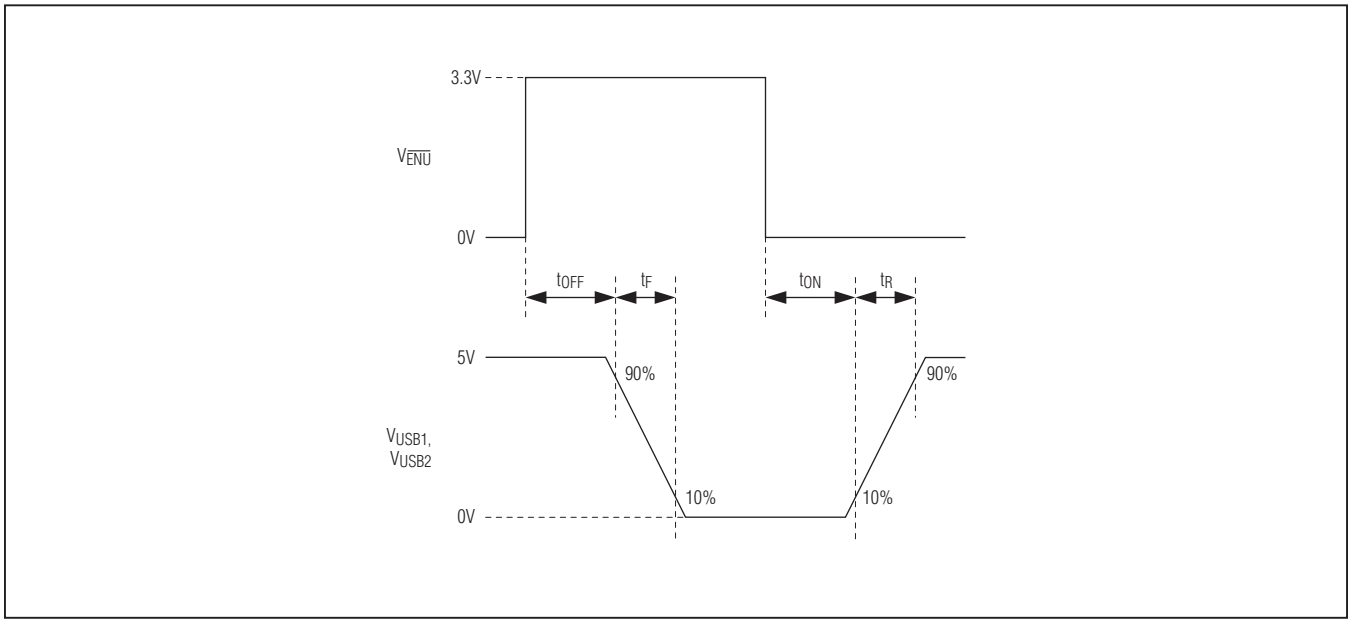


Figure 1. Timing Diagram for USB Switch Parameters

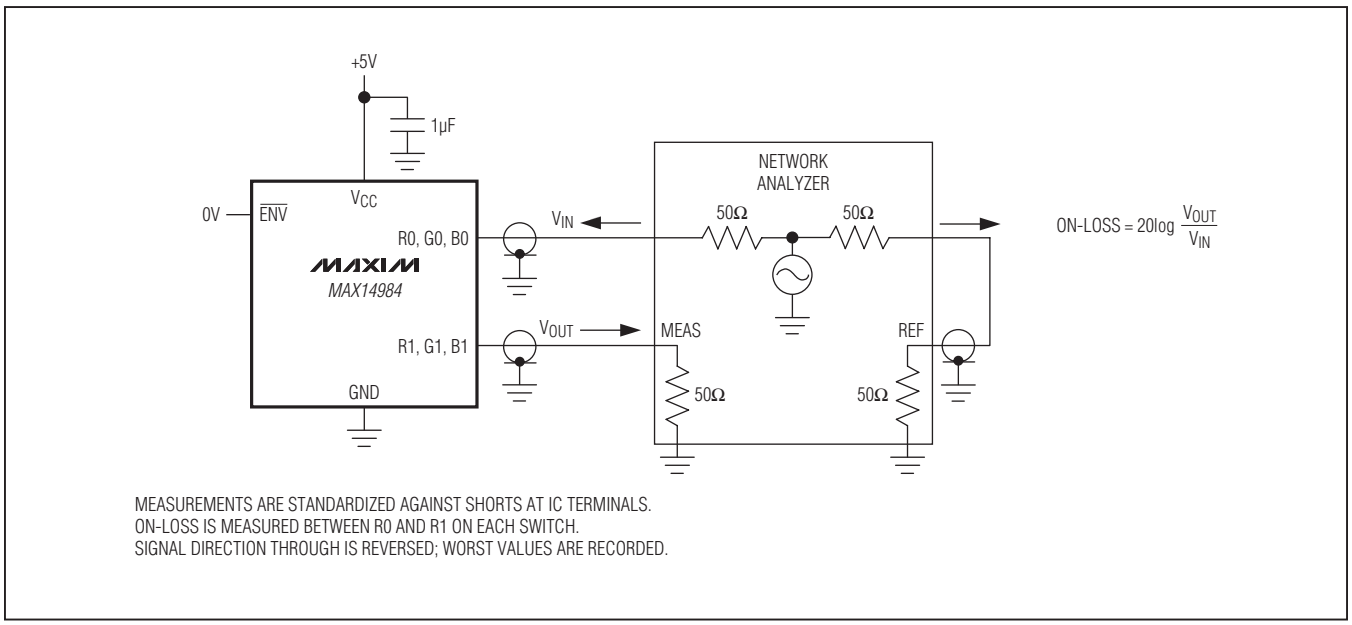


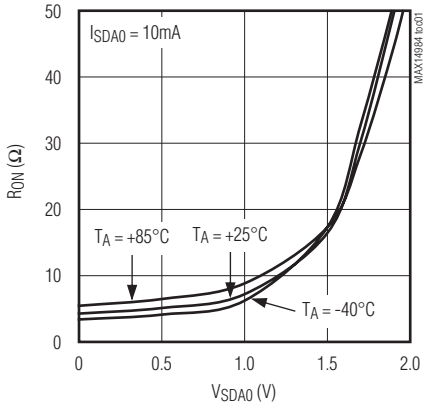
Figure 2. On-Loss

Enhanced VGA Port Protector with Monitor Detection and Dual USB Power Switches

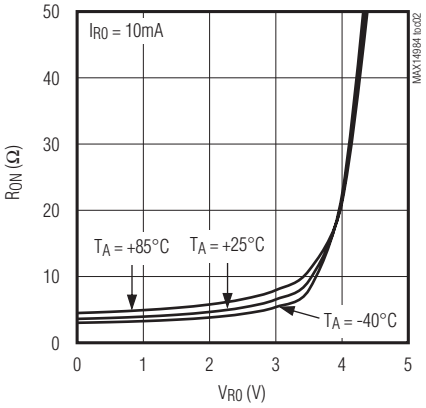
Typical Operating Characteristics

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted)

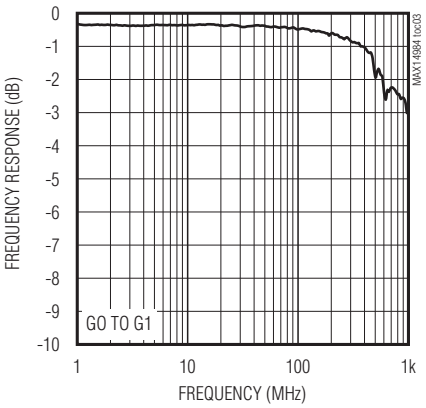
DDC ON-RESISTANCE vs. ANALOG SIGNAL VOLTAGE



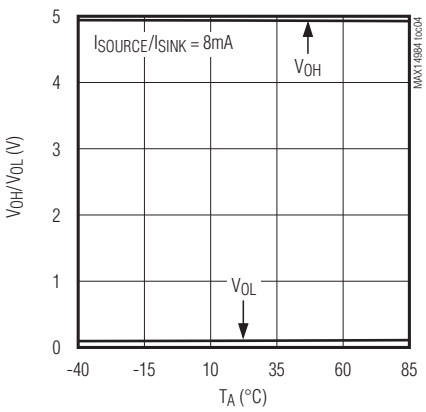
RGB ON-RESISTANCE vs. ANALOG SIGNAL VOLTAGE



FREQUENCY RESPONSE

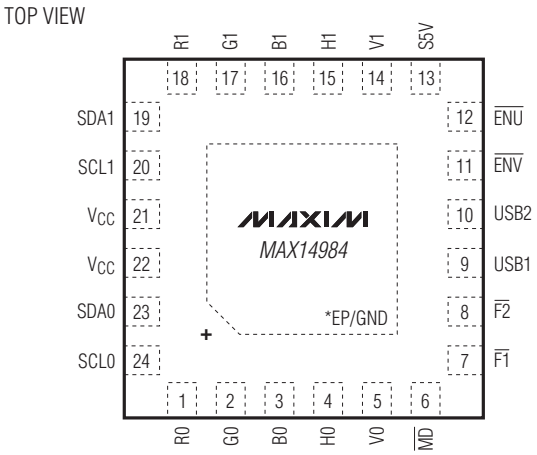


HSYNC/VSYNC OUTPUT VOLTAGE vs. TEMPERATURE



Enhanced VGA Port Protector with Monitor Detection and Dual USB Power Switches

Pin Configuration



TQFN
(4mm x 4mm)

*CONNECT THE EXPOSED PAD (EP/GND) TO THE GROUND PLANE.

Pin Description

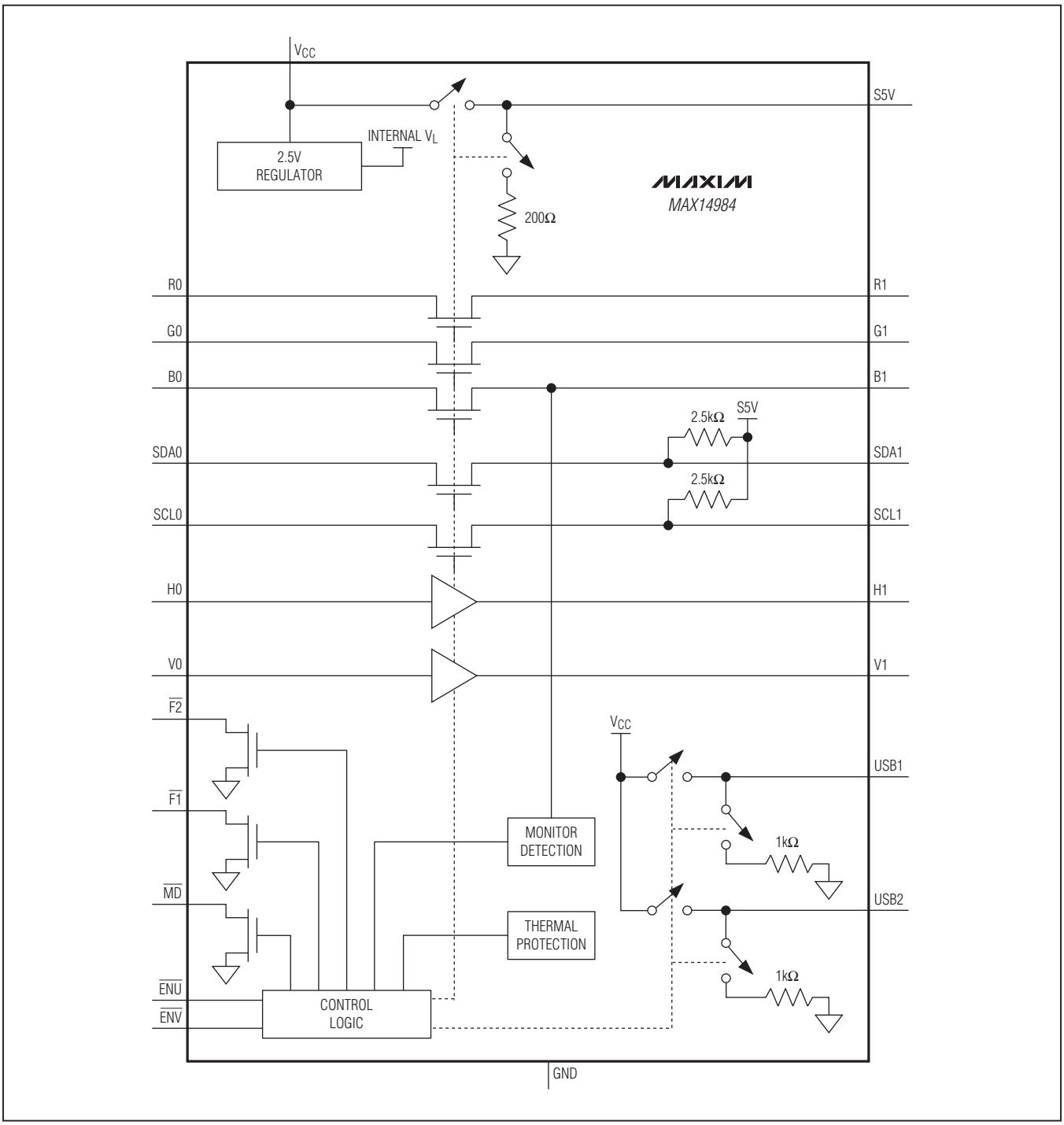
PIN	NAME	FUNCTION	ESD
1	R0	RGB Analog Input	Standard
2	G0	RGB Analog Input	Standard
3	B0	RGB Analog Input	Standard
4	H0	Horizontal Sync Input	Standard
5	V0	Vertical Sync Input	Standard
6	$\overline{MD}$	Monitor Detect Output. $\overline{MD}$ is an active-low, open-drain output.	Standard
7	$\overline{F1}$	Fault Output 1. $\overline{F1}$ is an active-low, open-drain output that asserts when a fault condition is detected on USB1.	Standard
8	$\overline{F2}$	Fault Output 2. $\overline{F2}$ is an active-low, open-drain output that asserts when a fault condition is detected on USB2.	Standard
9	USB1	5V USB Power Output 1. USB1 is internally pulled down when not enabled.	High
10	USB2	5V USB Power Output 2. USB2 is internally pulled down when not enabled.	High
11	$\overline{ENV}$	Video Enable Input. Drive $\overline{ENV}$ low to connect the VGA signals to the VGA port.	High
12	$\overline{ENU}$	USB Enable Input. Drive $\overline{ENU}$ low to enable the USB power-supply outputs.	High

Pin Description (continued)

PIN	NAME	FUNCTION	ESD
13	S5V	Switched 5V Output. S5V is connected when $\overline{ENV}$ is low and is internally pulled down when not connected.	High
14	V1	Vertical Sync Output	High
15	H1	Horizontal Sync Output	High
16	B1	RGB Analog Output	High
17	G1	RGB Analog Output	High
18	R1	RGB Analog Output	High
19	SDA1	DDC Input/Output. SDA1 has an internal 2.5kΩ pullup resistor to S5V	High
20	SCL1	DDC Input/Output. SCL1 has an internal 2.5kΩ pullup resistor to S5V	High
21, 22	V_{CC}	Supply Voltage. V_{CC} = 5.0V ±5%. Bypass V_{CC} to GND with a 1µF or larger ceramic capacitor as close as possible to V_{CC}.	Standard
23	SDA0	DDC Input/Output	Standard
24	SCL0	DDC Input/Output	Standard
—	EP/GND	Exposed Pad. The exposed pad is the ground connection for the device. Connect EP/GND to the ground plane.	—

Enhanced VGA Port Protector with Monitor Detection and Dual USB Power Switches

Functional Diagram



Detailed Description

The MAX14984 integrates high-bandwidth analog switches and level-translating buffers with current-limited power switches to implement a VGA port protector. The device provides switching for red-green-blue (RGB) signals, horizontal and vertical synchronization (H/V) pulses, display data channel (DDC) signals, and 5V power supplies. The power switches provide +5V power with current limiting and reverse voltage protection to the VGA port and up to two USB ports.

The device uses a simplified power-supply interface that operates from a single +5V supply. An internal 2.5V regulator limits the voltage passed by the DDC switches to provide compatibility with low-voltage graphics controllers.

The device features two enable inputs, a monitor detection output, and two fault outputs. $\overline{ENV}$ can be connected to $\overline{MD}$ to automatically connect the graphics signal when a monitor is inserted. The fault outputs signal when a fault condition is detected on either of the USB power outputs and they are enabled by $\overline{ENU}$.

5V Power Switch (S5V)

The MAX14984 provides a switched +5V output in addition to the regular VGA signals (S5V). This output can supply 55mA with less than 300mV drop from V_{CC}. The S5V output tolerates +5V while turned off or when V_{CC} is not present.

The power switches are protected against overcurrent and overtemperature faults. The device limits current supplied to the monitor side to 300mA (typ). Thermal protection circuitry shuts off the switch when the temperature exceeds +155°C. The device is re-enabled once the temperature has fallen to below +130°C.

S5V is connected whenever $\overline{ENV}$ is low and has a 200Ω (typ) pulldown resistor to discharge filter capacitors when the switch is off.

USB Switches and $\overline{F1}$/$\overline{F2}$ Outputs

The MAX14984 features two switches that provide power for up to two USB connectors. One enable input, $\overline{ENU}$, controls both switches simultaneously. Each switch can provide up to 500mA while only dropping 250mV from V_{CC}.

Two active-low fault outputs, $\overline{F1}$ and $\overline{F2}$, assert when a fault is detected on USB1 or USB2, respectively. Two fault conditions can be detected: short circuit to GND and overcurrent draw from the USB port. The switches are protected against reverse current into VCC while $\overline{ENU}$ is high, but this condition is not detected by $\overline{F1}$ and $\overline{F2}$. Current-limiting and thermal-shutdown circuitry protects the device in the presence of any fault.

A blanking period is built in to $\overline{F1}$ and $\overline{F2}$ that delays assertion until the current limit has been reached for at least t_{BLANK}. In addition, an internal 1kΩ pulldown resistor is connected on each USB output when it is disabled.

The $\overline{F1}$ and $\overline{F2}$ outputs are tolerant to external voltages of up to 6V. The MAX14984 limits the current into them to 600µA.

RGB Switches

The MAX14984 provides three single-pole/single-throw (SPST) high-bandwidth switches to connect the standard VGA R, G, and B signals from the graphics controller to the VGA port. The R, G, B analog switches are identical, and any of the three switches can be used to route red, green, or blue video signals.

The RGB switches are connected when $\overline{ENV}$ is low.

Horizontal/Vertical Sync Buffer

The H/V signals are buffered to provide level shifting and drive capability to meet the VESA specification.

H1 and V1 are enabled when $\overline{ENV}$ is low and high impedance when $\overline{ENV}$ is high. The H and V channels are not interchangeable.

Display Data Channel Switches (SDA_, SCL_)

The MAX14984 provides two voltage-limited SPST switches to connect DDC signals (SDA_, SCL_). These switches limit the voltage that can be passed through to the graphics controller to less than 2.5V. Internal pullup resistors on the monitor side of the switches translate the graphics controller signals to 5V compatible logic. Connect pullup resistors on SCL0 and SDA0 to define the logic level of the graphics controller.

The SDA_ and SCL_ switches are connected when $\overline{ENV}$ is low and are identical; either switch can be used to route SDA or SCL I²C signals.

Monitor Detection and Automatic Switching

The MAX14984 detects monitor insertion/removal events by measuring the voltage on B1. The monitor detection circuitry always correctly indicates the presence of a monitor as long as V0 is not high impedance. The voltage measurement is only sampled between synchronization pulses on V0 from the controller when a monitor is inserted to ensure that the video signal is not interrupted while promptly detecting a removal.

The device automatically connects the graphics controller to the monitor when it is plugged in if configured in automatic mode. To configure automatic mode, connect $\overline{MD}$ to $\overline{ENV}$ and add a pullup resistor.

Applications Information

Compatibility with Low-Voltage Graphics Controllers

The MAX14984 provides the level shifting necessary to drive a standard VGA port using any graphics controller. Internal buffers drive the H and V signals to VGA standard TTL levels. The DDC switches provide level shifting by limiting signal levels that can be passed through the DDC switches to less than 2.5V. Add pullup resistors from the DDC lines to the graphics controller supply to set the logic level on the SDA0/SCL0 side.

Power-Supply Decoupling

Bypass V_{CC} to ground with a 1µF or larger ceramic capacitor as close to the device as possible.

PC Board Layout

High-speed switches such as the MAX14984 require proper PCB layout for optimum performance. Ensure that impedance-controlled PCB traces for high-speed signals are matched in length and as short as possible. Connect the exposed pad to a solid ground plane.

High ESD Protection

Electrostatic Discharge (ESD) protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV Human Body Model (HBM) encountered during handling and assembly. All VGA and USB outputs are further protected against ESD up to ±8kV (HBM) without damage (see the *Pin Description*). The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the MAX14984 continues to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 3 shows the Human Body Model. Figure 4 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

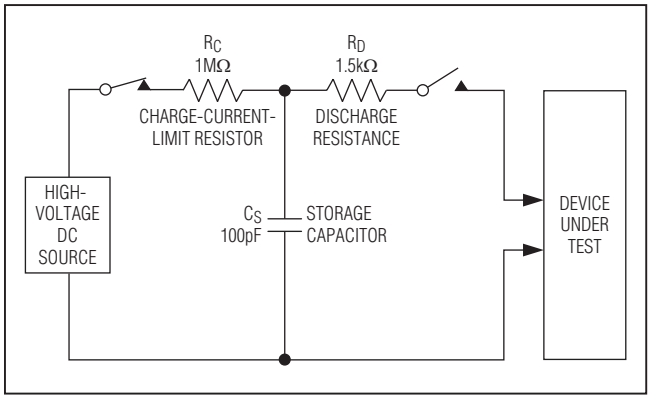


Figure 3. Human Body ESD Test Model

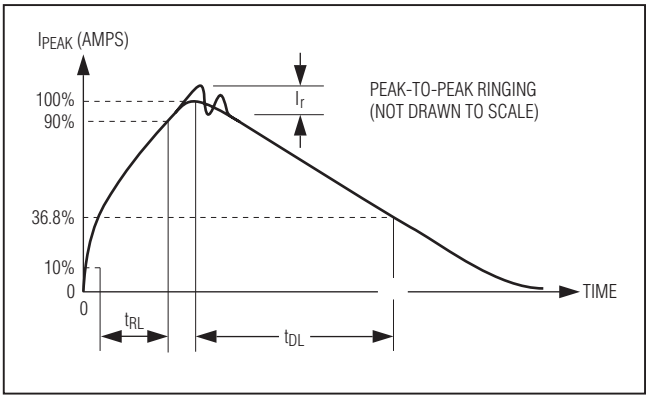


Figure 4. Human Body Current Waveform

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14984ETG+	-40°C to +85°C	24 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed paddle.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T2444+3	21-0139	90-0021

Enhanced VGA Port Protector with Monitor Detection and Dual USB Power Switches

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/12	Initial release	—