Multichannel, True-Differential, Serial, 14-Bit ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND, DGND .....-0.3V to +6.0V
AGND to DGND.....-0.3V to +0.3V
CH0–CH7, COM to AGND.....-0.3V to (V_{DD} + 0.3V)
REF, REFADJ to AGND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND.....-0.3V to (V_{DD} + 0.3V)
Digital Outputs to DGND .....-0.3V to (V_{DD} + 0.3V)
Digital Output Sink Current 25mA

Continuous Power Dissipation (T_A = +70°C)
20 TSSOP (derate 10.9mW/°C above +70°C) 879mW
Operating Temperature Ranges
MAX114_ BC_ _ .....0°C to +70°C
MAX114_ BE_ _ .....-40°C to +85°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V (MAX1146/MAX1148), V_{DD} = 3.3V (MAX1147/MAX1149), $\overline{SHDN}$ = V_{DD}, V_{COM} = 0, f_{SCLK} = 2.1MHz, external clock (50% duty cycle), 18 clocks/conversion (116ksps), V_{REFADJ} = V_{DD}, C_{REF} = 2.2µF, external +4.096V reference at REF (MAX1146/MAX1148), external 2.500V reference at REF (MAX1147/MAX1149), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			14			Bits
Relative Accuracy (Note 2)	INL			±0.7	±2	LSB
Differential Nonlinearity	DNL	No missing codes over temperature	-1.0	±0.5	+1.5	LSB
Offset Error					±10	LSB
Offset Temperature Coefficient				0.3		ppm/°C
Gain Error		(Note 3)			±20	LSB
Gain Temperature Coefficient				±0.8		ppm/°C
Channel-to-Channel Offset Matching				±1		LSB
Channel-to-Channel Gain Matching				±1		LSB
DYNAMIC SPECIFICATIONS (1kHz sine-wave input, 2.5V_{P-P}, full-scale analog input, 116ksps, 2.1MHz external clock)						
Signal-to-Noise Plus Distortion Ratio	SINAD		77	81		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-96	-88	dB
Spurious-Free Dynamic Range	SFDR		84	98		dB
Channel-to-Channel Crosstalk		(Note 4)		-85		dB
Small-Signal Bandwidth	SSBW	-3dB point		3.0		MHz
Full-Power Bandwidth	FPBW	SINAD > 68dB		2.0		MHz
CONVERSION RATE						
Conversion Time (Note 5)	tCONV	External clock, 2.1MHz 15 SCLK cycles	7.2			µs
		Internal clock	6		8	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V (MAX1146/MAX1148), V_{DD} = 3.3V (MAX1147/MAX1149), $\overline{SHDN}$ = V_{DD}, V_{COM} = 0, f_{SCLK} = 2.1MHz, external clock (50% duty cycle), 18 clocks/conversion (116ksps), V_{REFADJ} = V_{DD}, C_{REF} = 2.2µF, external +4.096V reference at REF (MAX1146/MAX1148), external 2.500V reference at REF (MAX1147/MAX1149), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Throughput Rate	fSAMPLE	Internal clock mode, fSCLK = 2.1MHz	18 clocks/conversion			60.3	ksps
			24 clocks/conversion			51.5	
		External clock mode, fSCLK = 2.1MHz	18 clocks/conversion			116.66	
			24 clocks/conversion			87.50	
T/H Acquisition Time	tACQ			1.4			µs
Aperture Delay	tAD				20		ns
Aperture Jitter	tAJ				<50		ps
Serial Clock Frequency	fSCLK	External clock mode		0.1		2.1	MHz
		Internal clock mode		0		2.1	
Internal Clock Frequency					2.1		MHz
ANALOG INPUTS (CH0–CH7, COM)							
Input Voltage Range, Single-Ended and Differential (Note 6)		Unipolar, COM = 0		0		V_{REF}	V
		Bipolar, COM = V_{REF} / 2, single-ended				±V_{REF} / 2	
Multiplexer Leakage Current		On/off-leakage current, $V_{CH\_}$ = 0 to V_{DD}			±0.01	±1	µA
Input Capacitance					18		pF
INTERNAL REFERENCE (C_{REF} = 2.2µF, C_{REFADJ} = 0.01µF)							
REF Output Voltage	V_{REF}	MAX1147/MAX1149, T_A = +25°C		2.480	2.500	2.520	V
		MAX1146/MAX1148, T_A = +25°C		4.076	4.096	4.116	
REF Short-Circuit Current	I_{REFSC}	REF = DGND				20	mA
V_{REF} Tempco (Note 7)		MAX114_ BC _ _			±30	±50	ppm/°C
		MAX114_ BE _ _			±40	±60	
Load Regulation		0 to 0.2mA output load (Note 8)			2.0		mV
Capacitive Bypass at REF				2			µF
Capacitive Bypass at REFADJ				0.01			µF
REFADJ Output Voltage					1.250		V
REFADJ Input Range					±18		mV
REFADJ Logic High		Pull REFADJ high to disable the internal bandgap reference and reference buffer		V_{DD} - 0.25V			V
Reference Buffer Voltage Gain		MAX1147/MAX1149			2.000		V/V
		MAX1146/MAX1148			3.277		

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V (MAX1146/MAX1148), V_{DD} = 3.3V (MAX1147/MAX1149), $\overline{SHDN}$ = V_{DD}, V_{COM} = 0, f_{SCLK} = 2.1MHz, external clock (50% duty cycle), 18 clocks/conversion (116ksps), V_{REFADJ} = V_{DD}, C_{REF} = 2.2µF, external +4.096V reference at REF (MAX1146/MAX1148), external 2.500V reference at REF (MAX1147/MAX1149), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE AT REF						
REF Input Voltage Range	V_{REF}		1.5		V_{DD} + 50mV	V
REF Input Current	I_{REF}			125	450	µA
		Shutdown		0.01	10	
REF Input Resistance			6	8		kΩ
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)						
Input High Voltage	V_{IH}	V_{DD} < 3.6V	2.0			V
		V_{DD} > 3.6V	3.0			
Input Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYST}			0.2		V
Input Leakage	I_{IN}				±1	µA
Input Capacitance	C_{IN}			10		pF
DIGITAL OUTPUT (DOUT, SSTRB)						
Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
Output-Voltage High	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Tri-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}			±10	µA
Tri-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD}		10		pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}	MAX1147/MAX1149	2.7		3.6	V
		MAX1146/MAX1148	4.75		5.25	
Supply Current (Note 8)	I_{DD}	Normal operation, full-scale input, External reference, 116ksps		1.1	1.5	mA
		Normal operation, full-scale input, External reference, 10ksps		0.12		
		Normal operation, full-scale input, External reference, 1ksps		0.012		
		Normal operation, full-scale input, Internal reference at 116ksps		1.9	2.4	mA
Shutdown Supply Current (Note 8)		Fast power-down		120		µA
		Full power-down		0.3		
		$\overline{SHDN}$ = DGND		0.3	10	
Power-Supply Rejection (Note 9)	PSR	External reference		±0.2		mV

TIMING CHARACTERISTICS

(V_{DD} = 4.75V to 5.25V (MAX1146/MAX1148), V_{DD} = 2.7V to 3.6V (MAX1147/MAX1149), $\overline{SHDN}$ = V_{DD}, V_{COM} = 0, f_{SCLK} = 2.1MHz, external clock (50% duty cycle), 18 clocks/conversion (116ksps), V_{REFADJ} = V_{DD}, C_{REF} = 2.2µF, external +4.096V reference at REF for the MAX1146/MAX1148, external 2.500V reference at REF for the MAX1147/MAX1149, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Figures 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIN to SCLK Setup Time	t_{DS}		50			ns
DIN to SCLK Hold Time	t_{DH}		0			ns
SCLK Fall to Output Data Valid	t_{DOV}	C_{LOAD} = 50pF	10		80	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DOE}	C_{LOAD} = 50pF			120	ns
$\overline{CS}$ Rise to DOUT Disable	t_{DOD}	C_{LOAD} = 50pF			120	ns
$\overline{SHDN}$ Rise $\overline{CS}$ Fall to SCLK Rise Time	t_{CSS}		50			ns
$\overline{SHDN}$ Rise $\overline{CS}$ Fall to SCLK Rise Hold Time	t_{CSH}		50			ns
SCLK Clock Frequency	f_{SCLK}	External clock mode	0.1		2.1	MHz
		Internal clock mode	0		2.1	
SCLK Pulse-Width High	t_{CH}	Internal clock mode	100			ns
SCLK Pulse-Width Low	t_{CL}	Internal clock mode	100			ns
$\overline{CS}$ Fall to SSTRB Output Enable	t_{STE}	External clock mode only			120	ns
$\overline{CS}$ Rise to SSTRB Output Disable	t_{STD}	External clock mode only			120	ns
SSTRB Rise to SCLK Rise	t_{SCK}	Internal clock mode only		0		ns
SCLK Fall to SSTRB Edge	t_{SCST}				80	ns
$\overline{CS}$ Pulse Width	t_{CSW}		100			ns

Note 1: Tested at V_{DD} = 3.0V (MAX1147/MAX1149) or 5.0V(MAX1146/MAX1148); V_{COM} = 0; unipolar single-ended input mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: Offset nulled. Measured with external reference.
Note 4: "On" channel grounded; full-scale 1kHz sine wave applied to all "off" channels.
Note 5: Conversion time defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle. (See Figures 8–11.)
Note 6: The common-mode range for the analog inputs is from AGND to V_{DD}.
Note 7: Digital inputs equal V_{DD} or DGND.
Note 8: External load should not change during conversion for specified accuracy.
Note 9: Measured as (V_{FS} x 3.6V) - (V_{FS} x 2.7V) for the MAX1147/MAX1149 and (V_{FS} x 5.25V) - (V_{FS} x 4.75V) for the MAX1146/MAX1148. V_{DD} = 3.6V to 2.7V for MAX1147/MAX1149 and V_{DD} = 5.25V to 4.75V for the MAX1146/MAX1148.

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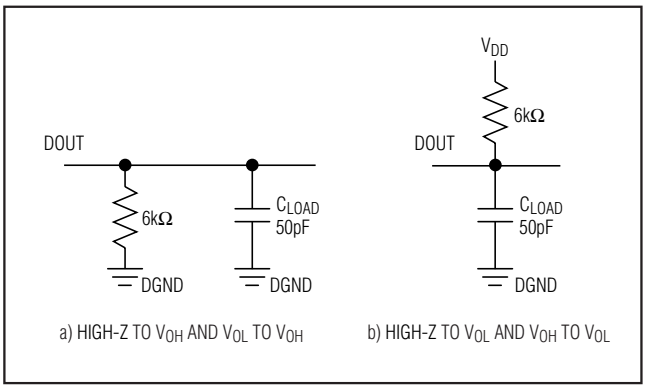


Figure 1. Load Circuits for Enable Time

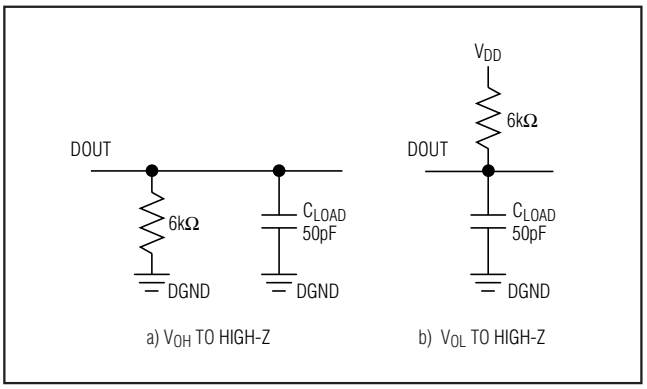


Figure 2. Load Circuits for Disable Time

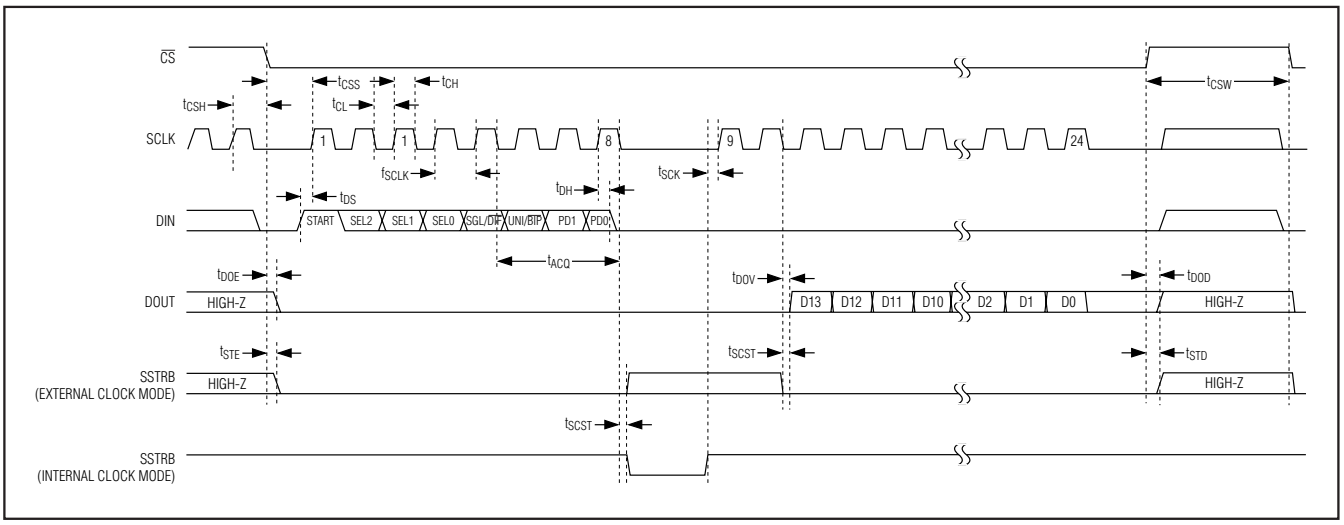
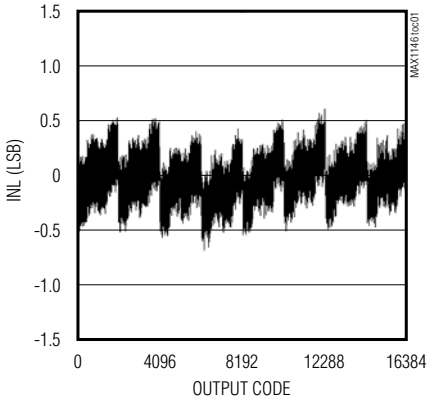


Figure 3. Detailed Operating Characteristics

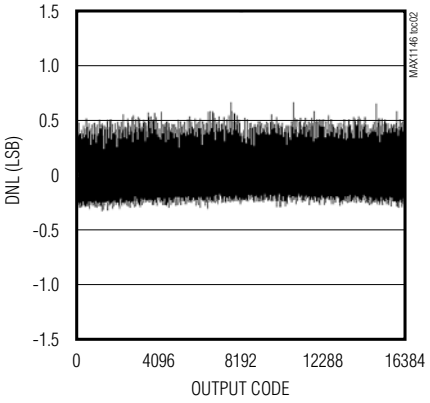
Typical Operating Characteristics

(V_{DD} = +5.0V (MAX1146/MAX1148), V_{DD} = +3.3V (MAX1147/MAX1149), $\overline{SHDN}$ = V_{DD}, V_{COM} = 0, f_{SCLK} = 2.1MHz, external clock (50% duty cycle), 18 clocks/conversion (116ksps), V_{REFADJ} = V_{DD}, external +4.096V reference at REF (MAX1146/MAX1148), external +2.500V reference at REF (MAX1147/MAX1149), C_{REF} = 2.2µF, C_{LOAD} = 50pF, T_A = +25°C, unless otherwise noted.)

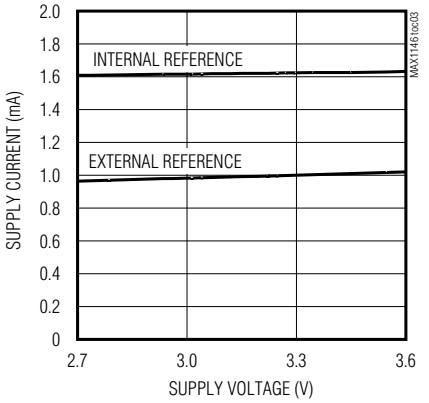
INL vs. OUTPUT CODE



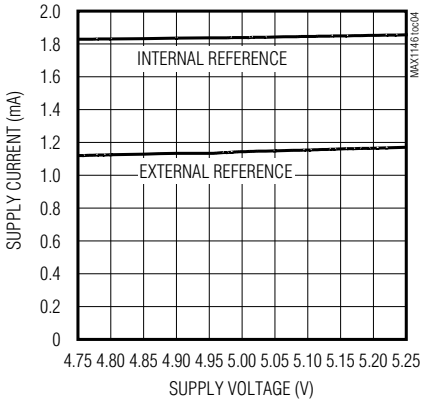
DNL vs. OUTPUT CODE



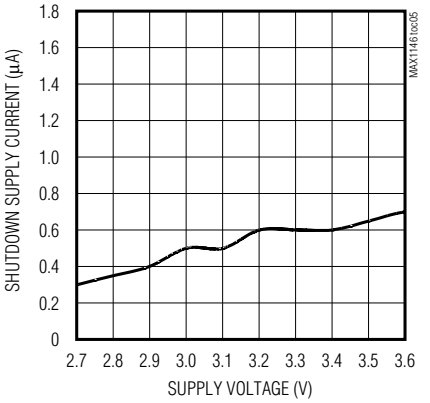
SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX1147/MAX1149)



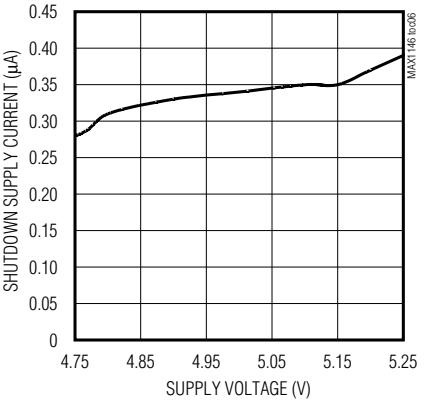
SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX1146/MAX1148)



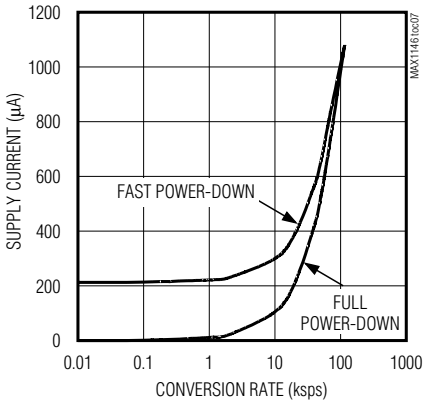
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX1147/MAX1149)



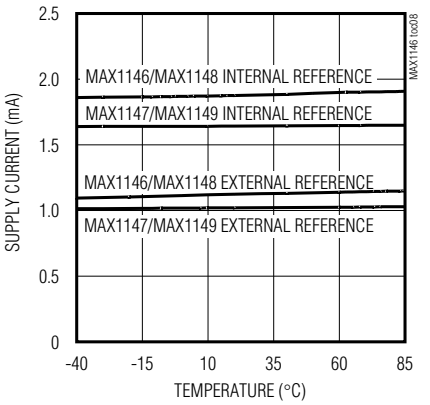
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX1146/MAX1148)



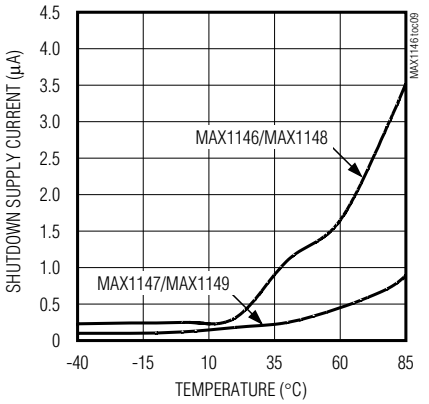
SUPPLY CURRENT vs. CONVERSION RATE



SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



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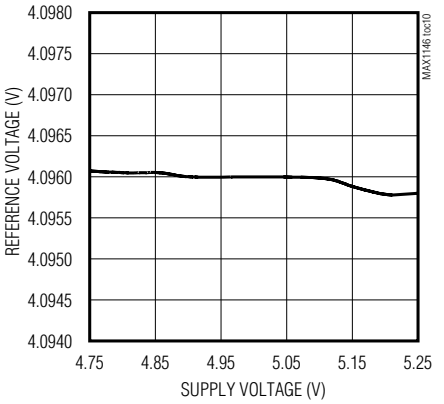
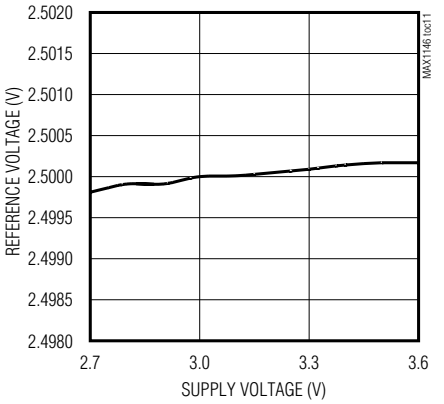
Typical Operating Characteristics (continued)

(V_{DD} = +5.0V (MAX1146/MAX1148), V_{DD} = +3.3V (MAX1147/MAX1149), $\overline{SHDN}$ = V_{DD}, V_{COM} = 0, f_{SCLK} = 2.1MHz, external clock (50% duty cycle), 18 clocks/conversion (116ksps), V_{REFADJ} = V_{DD}, external +4.096V reference at REF (MAX1146/MAX1148), external +2.500V reference at REF (MAX1147/MAX1149), C_{REF} = 2.2µF, C_{LOAD} = 50pF, T_A = +25°C, unless otherwise noted.)

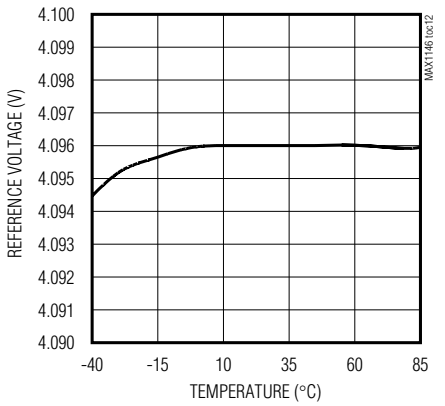
REFERENCE VOLTAGE vs. SUPPLY VOLTAGE (MAX1146/MAX1148)



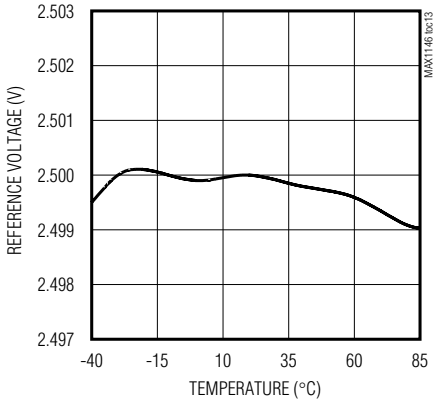
REFERENCE VOLTAGE vs. SUPPLY VOLTAGE (MAX1147/MAX1149)



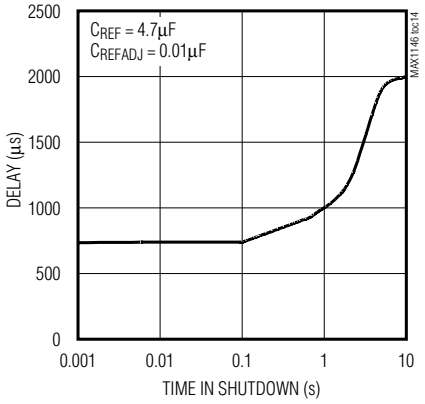
REFERENCE VOLTAGE vs. TEMPERATURE (MAX1146/MAX1148)



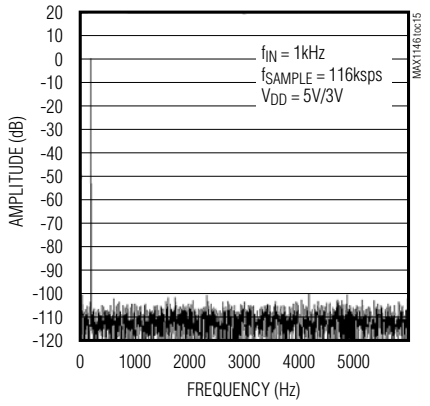
REFERENCE VOLTAGE vs. TEMPERATURE (MAX1147/MAX1149)



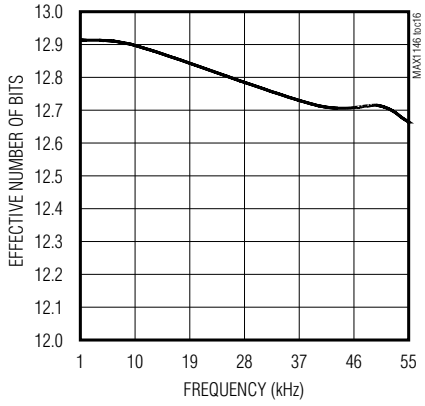
REFERENCE BUFFER POWER-UP DELAY vs. TIME IN SHUTDOWN



FFT PLOT



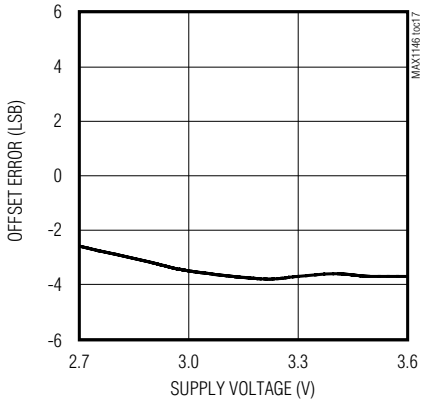
EFFECTIVE NUMBER OF BITS vs. FREQUENCY



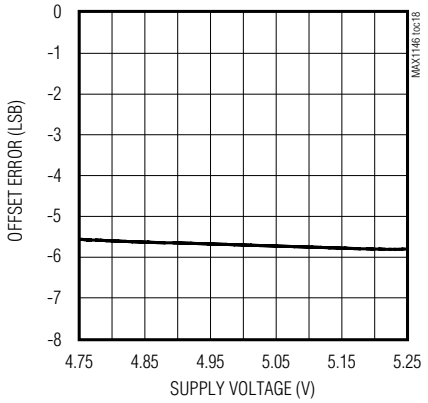
Typical Operating Characteristics (continued)

(V_{DD} = +5.0V (MAX1146/MAX1148), V_{DD} = +3.3V (MAX1147/MAX1149), $\overline{SHDN}$ = V_{DD}, V_{COM} = 0, f_{SCLK} = 2.1MHz, external clock (50% duty cycle), 18 clocks/conversion (116ksps), V_{REFADJ} = V_{DD}, external +4.096V reference at REF (MAX1146/MAX1148), external +2.500V reference at REF (MAX1147/MAX1149), C_{REF} = 2.2µF, C_{LOAD} = 50pF, T_A = +25°C, unless otherwise noted.)

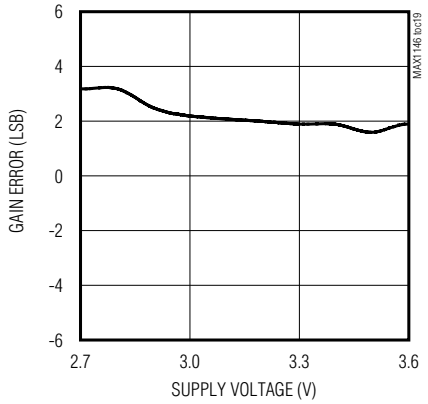
OFFSET ERROR vs. SUPPLY VOLTAGE (MAX1147/MAX1149)



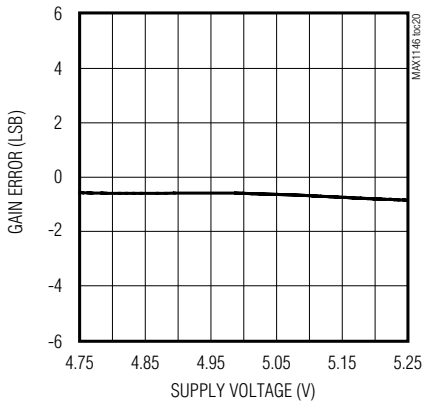
OFFSET ERROR vs. SUPPLY VOLTAGE (MAX1146/MAX1148)



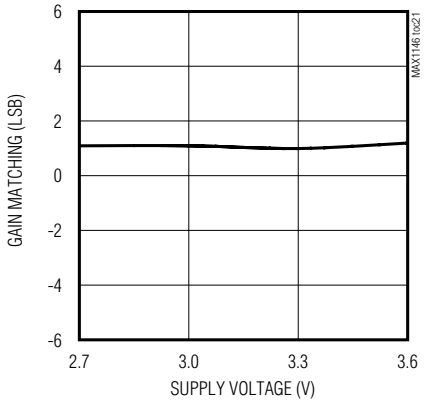
GAIN ERROR vs. SUPPLY VOLTAGE (MAX1147/MAX1149)



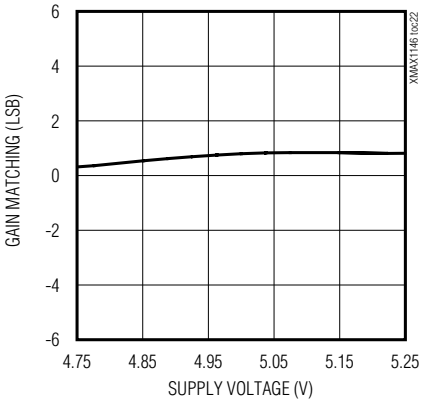
GAIN ERROR vs. SUPPLY VOLTAGE (MAX1146/MAX1148)



CHANNEL-TO-CHANNEL GAIN MATCHING vs. SUPPLY VOLTAGE (MAX1147/MAX1149)



CHANNEL-TO-CHANNEL GAIN MATCHING vs. SUPPLY VOLTAGE (MAX1146/MAX1148)

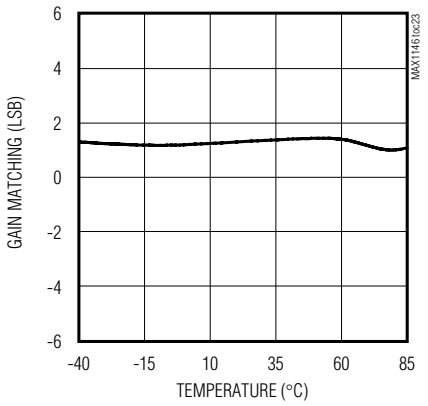


Multichannel, True-Differential, Serial, 14-Bit ADCs

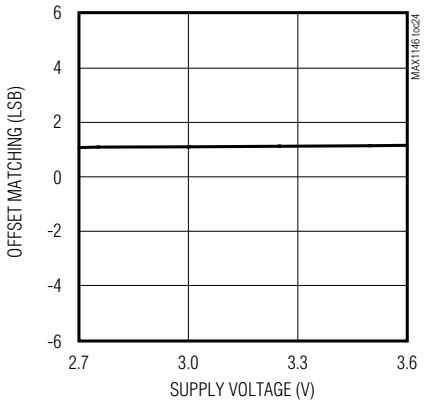
Typical Operating Characteristics (continued)

(V_{DD} = +5.0V (MAX1146/MAX1148), V_{DD} = +3.3V (MAX1147/MAX1149), $\overline{SHDN}$ = V_{DD}, V_{COM} = 0, f_{SCLK} = 2.1MHz, external clock (50% duty cycle), 18 clocks/conversion (116ksps), V_{REFADJ} = V_{DD}, external +4.096V reference at REF (MAX1146/MAX1148), external +2.500V reference at REF (MAX1147/MAX1149), C_{REF} = 2.2µF, C_{LOAD} = 50pF, T_A = +25°C, unless otherwise noted.)

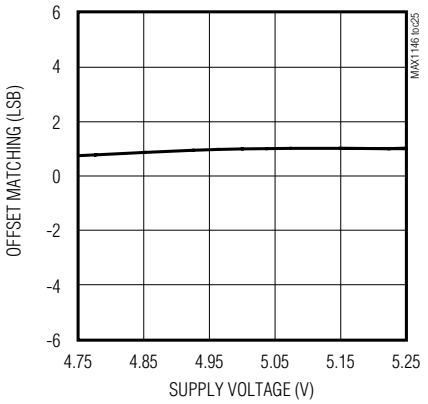
CHANNEL-TO-CHANNEL GAIN MATCHING vs. TEMPERATURE



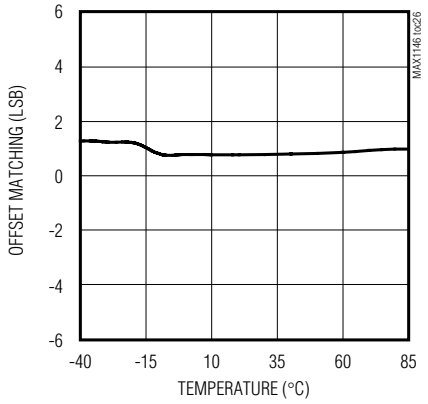
CHANNEL-TO-CHANNEL OFFSET MATCHING vs. SUPPLY VOLTAGE (MAX1147/MAX1149)



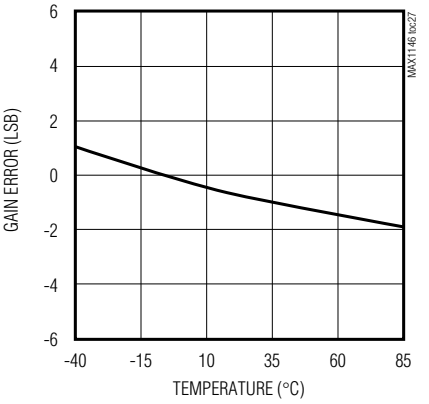
CHANNEL-TO-CHANNEL OFFSET MATCHING vs. SUPPLY VOLTAGE (MAX1146/MAX1148)



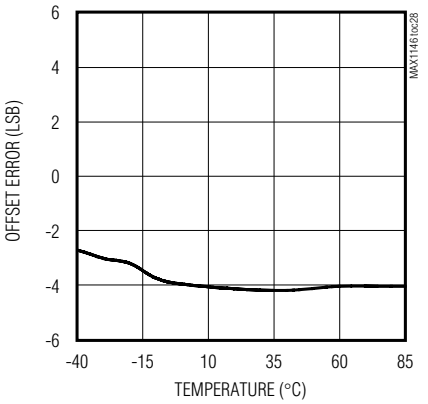
CHANNEL-TO-CHANNEL OFFSET MATCHING vs. TEMPERATURE



GAIN ERROR vs. TEMPERATURE



OFFSET ERROR vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
MAX1148 MAX1149	MAX1146 MAX1147		
1	1	CH0	Analog Inputs
2	2	CH1	
3	3	CH2	
4	4	CH3	
5	—	CH4	
6	—	CH5	
7	—	CH6	
8	—	CH7	
9	9	COM	Common Input. Negative analog input in single-ended mode. COM sets zero-code voltage in unipolar and bipolar mode.
10	10	$\overline{SHDN}$	Active-Low Shutdown Input. Pulling $\overline{SHDN}$ low shuts down the device reducing supply current to 0.2µA. Driving shutdown high enables the devices.
11	11	REF	Reference-Buffer Output/ADC Reference Input. Reference voltage for analog-to-digital conversion. In internal reference mode, the MAX1146/MAX1148 V_{REF} is +4.096V, and the MAX1147/MAX1149 V_{REF} is +2.500V.
12	12	REFADJ	Bandgap Reference Output and Reference Buffer Input. Bypass to AGND with a 0.01µF capacitor. Connect REFADJ to V_{DD} to disable the internal bandgap reference and reference-buffer amplifier.
13	13	AGND	Analog Ground
14	14	DGND	Digital Ground
15	15	DOUT	Serial Data Output. Data is clocked out at the falling edge of SCLK when $\overline{CS}$ is low. DOUT is high impedance when $\overline{CS}$ is high.
16	16	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the ADC conversion begins, and goes high when the conversion is finished. In external clock mode, SSTRB pulses high for two clock periods before the MSB decision. SSTRB is high impedance when $\overline{CS}$ is high (external clock mode).
17	17	DIN	Serial Data Input. Data is clocked in at the rising edge of SCLK when $\overline{CS}$ is low. DIN is high impedance when $\overline{CS}$ is high.
18	18	$\overline{CS}$	Active-Low Chip Select. Data is not clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
19	19	SCLK	Serial Clock Input. Clocks data in and out of the serial interface and sets the conversion speed in external clock mode. (Duty cycle must be 40% to 60%.)
20	20	V_{DD}	Positive Supply Voltage. Bypass to AGND with a 0.1µF capacitor.
—	5–8	N.C.	No Connection. Not internally connected.

Multichannel, True-Differential, Serial, 14-Bit ADCs

Detailed Description

The MAX1146–MAX1149 ADCs use a successive-approximation conversion technique and input T/H circuitry to convert an analog signal to a 14-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). Figure 4 shows the typical application circuit and Figure 5 shows a functional diagram of the MAX1148/MAX1149.

True-Differential Analog Input and Track/Hold

The MAX1146–MAX1149 analog input architecture contains an analog input multiplexer (MUX), two T/H capacitors, T/H switches, a comparator, and two switched capacitor digital-to-analog converters (DACs) (Figure 6).

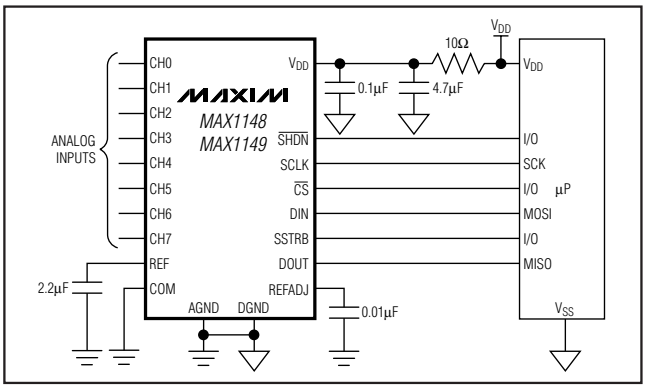


Figure 4. Typical Application Circuit

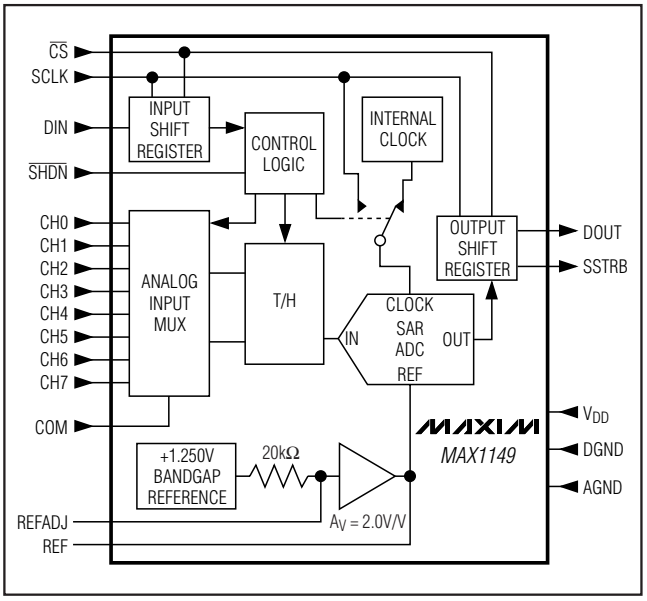


Figure 5. Functional Diagram

In single-ended mode, the analog input MUX connects IN+ to the selected input channel and IN- to COM. In differential mode, IN+ and IN- are connected to the selected analog input pairs such as CH0/CH1. Select the analog input channels according to Tables 1–5.

The analog input multiplexer switches to the selected channel on the control byte's fifth SCLK falling edge. At this time, the T/H switches are in the track position and $C_{T/H+}$ and $C_{T/H-}$ track the analog input signal. At the control byte's eighth SCLK falling edge, the MUX opens and the T/H switches move to the hold position, retaining the charge on $C_{T/H+}$ and $C_{T/H-}$ as a sample of the input signal. See Figures 8–11 for input MUX and T/H switch positioning.

During the conversion interval, the switched capacitive DAC adjusts to restore the comparator-input voltage to 0 within the limits of 14-bit resolution. This action requires 15 conversion clock cycles and is equivalent to transferring a charge of 18pF × (V_{IN+} - V_{IN-}) from $C_{T/H+}$ and $C_{T/H-}$ to the binary-weighted capacitive DAC, forming a digital representation of the analog input signal.

After conversion, the T/H switches move from the hold position to the track position and the MUX switches back to the last specified position. In internal clock mode, the conversion is complete on the rising edge of SSTRB. In external clock mode, the conversion is complete on the eighteenth SCLK falling edge.

The time required for the T/H to acquire an input signal is a function of the analog input source impedance. If the input signal source impedance is high, the acquisition time lengthens. The MAX1146–MAX1149 provide three SCLK cycles (t_{ACQ}) in which the T/H capacitance must acquire a charge representing the input signal, typically the last three SCLKs of the control word. The input source impedance (R_{SOURCE}) should be minimized to allow the T/H capacitance to charge within this allotted time.

$$t_{ACQ} = 11.5 \times (R_{SOURCE} + R_{IN}) \times C_{IN}$$

where R_{SOURCE} is the analog input source impedance, R_{IN} is 2.6kΩ (which is the sum of the analog input MUX and T/H switch resistances), and C_{IN} is 18pF (which is the sum of $C_{T/H+}$, $C_{T/H-}$, and input stray capacitance).

To minimize sampling errors with higher source impedances, connect a 100pF capacitor from the analog input to AGND. This input capacitor reduces the input's AC impedance but forms an RC filter with the source impedance, limiting the analog input bandwidth. For larger source impedance, use a buffer amplifier such as the MAX4430 to maintain analog input signal integrity.

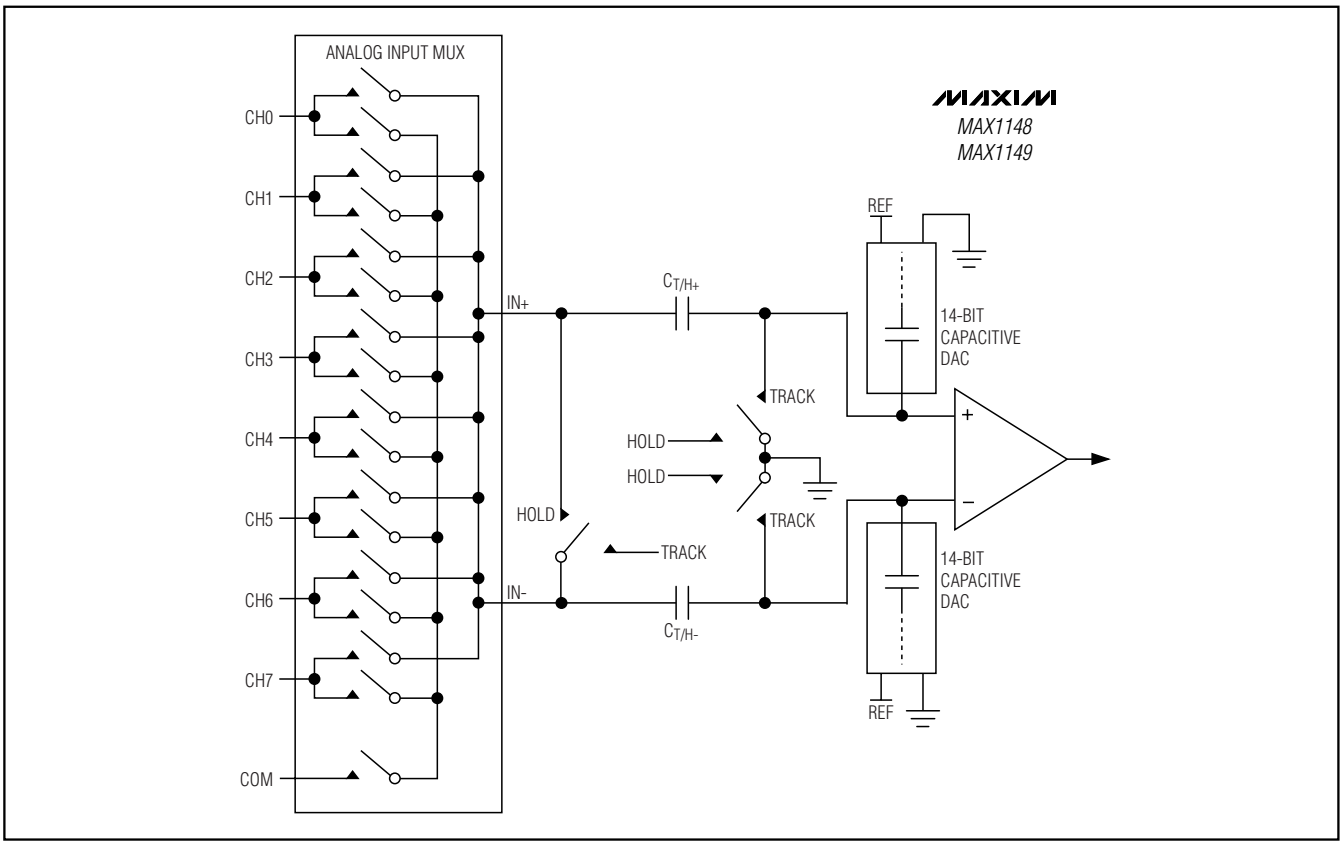


Figure 6. Equivalent Input Circuit

Input Bandwidth

The MAX1146–MAX1149 feature input tracking circuitry with a 3.0MHz small-signal bandwidth. The 3.0MHz input bandwidth makes it possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes clamp the analog input to V_{DD} and AGND. These diodes allow the analog inputs to swing from (AGND - 0.3V) to (V_{DD} + 0.3V) without causing damage to the device. For accurate conversions, the inputs must not go more than 50mV below AGND or above V_{DD}.

Note: If the analog input exceeds 50mV beyond the supply rails, limit the current to 2mA.

Quick Look

Use the circuit of Figure 7 to quickly evaluate the MAX1148/MAX1149. The MAX1148/MAX1149 require a control byte to be written to DIN using SCLK before each conversion. Connecting DIN to V_{DD} and clocking SCLK feeds in a control byte of $FF HEX (see Table 1). Trigger single-ended unipolar conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for two clock periods before the MSB of the 14-bit conversion result is shifted out of DOUT. Varying the analog input to CH7 alters the sequence of bits from DOUT. A total of 18 clock cycles are required per conversion (Figure 10). All transitions of the SSTRB and DOUT outputs occur on the falling edge of SCLK.

Multichannel, True-Differential, Serial, 14-Bit ADCs

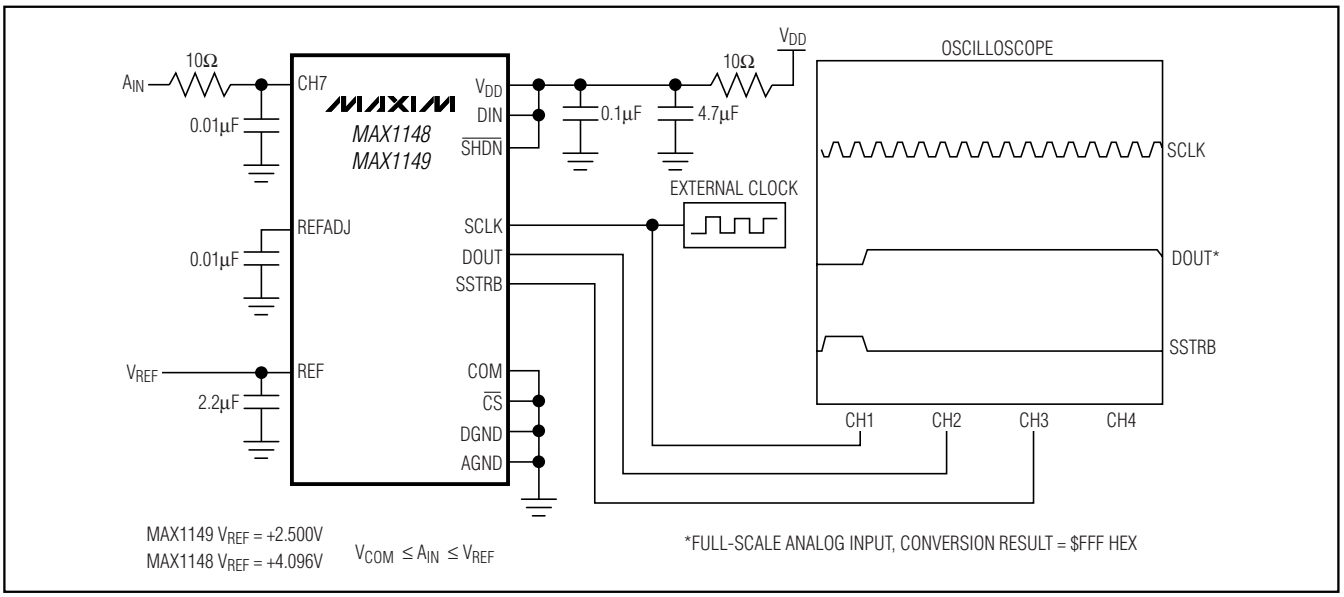


Figure 7. Quick-Look Circuit

Table 1. Control Byte Format

BIT	NAME	DESCRIPTION
7 (MSB)	START	Start bit. The first logic 1 bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6	SEL2	Channel-select bits. The channel-select bits select which of the eight channels are used for the conversion (Tables 2, 3, 4, and 5).
5	SEL1	
4	SEL0	
3	SGL/$\overline{DIF}$	1 = single ended, 0 = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured.
2	UNI/$\overline{BIP}$	1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, connect COM to AGND to perform conversion from 0 to V_{REF}. In bipolar mode, connect COM to $V_{REF}/2$ to perform conversion from 0 to V_{REF}. See Table 7.
1	PD1	Selects clock and power-down modes. PD1 = 0 and PD0 = 0 selects full power-down mode*. PD1 = 0 and PD0 = 1 selects fast power-down mode*. PD1 = 1 and PD0 = 0 selects internal clock mode. PD1 = 1 and PD0 = 1 selects external clock mode.
0 (LSB)	PD0	

**The start bit resets power-down modes.*

Table 2. MAX1148/MAX1149 Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	+								-
1	0	0		+							-
0	0	1			+						-
1	0	1				+					-
0	1	0					+				-
1	1	0						+			-
0	1	1							+		-
1	1	1								+	-

Table 3. MAX1148/MAX1149 Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	-						
0	0	1			+	-				
0	1	0					+	-		
0	1	1							+	-
1	0	0	-	+						
1	0	1			-	+				
1	1	0					-	+		
1	1	1							-	+

Table 4. MAX1146/MAX1147 Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	COM
0	0	0	+				-
1	0	0		+			-
0	0	1			+		-
1	0	1				+	-

Table 5. MAX1146/MAX1147 Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3
0	0	0	+	-		
0	0	1			+	-
1	0	0	-	+		
1	0	1			-	+

Power-On Reset

When power is first applied, internal power-on reset circuitry activates the MAX1146–MAX1149 in internal clock mode, making the MAX1146–MAX1149 ready to convert with SSTRB high. No conversions should be performed until the power supply is stable. The first logical 1 on DIN with $\overline{CS}$ low is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros.

Starting a Conversion

Start a conversion by clocking a control byte into DIN. With $\overline{CS}$ low, a rising edge on SCLK latches a bit from DIN into the MAX1146–MAX1149 internal shift register. After $\overline{CS}$ falls, the first logic 1 bit defines the control byte's MSB. Until this start bit arrives, any number of logic 0 bits can be clocked into DIN with no effect. Table 1 shows the control-byte format.

The MAX1146–MAX1149 are compatible with SPI/QSPI and MICROWIRE devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers. Set CPOL = 0 and CPHA = 0. MICROWIRE, SPI, and QSPI transmit a byte and receive a byte at the same time. Using the *Typical Application Circuit* (Figure 4), the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 14-bit conversion result).

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Digital Output

In unipolar input mode, the digital output is straight binary (Figure 14). For bipolar input mode, the digital output is two's complement binary (Figure 15). Data is clocked out on the falling edge of SCLK in MSB-first format.

Clock Modes

The MAX1146–MAX1149 can use either the external serial clock or the internal clock to drive the successive-approximation conversion. The external clock shifts data in and out of the MAX1146–MAX1149.

External clock mode allows the fastest throughput rate (116ksps) and serial clock frequencies from 0.1MHz to 2.1MHz. Internal clock mode provides the best noise performance because the digital interface can be idle during conversion. The internal clock mode serial clock frequency can range from 0 to 2.1MHz. Internal clock mode allows the CPU to request a conversion and clock back the results.

Bits PD1 and PD0 of the control byte program the clock and power-down modes. The MAX1146–MAX1149 power up in internal clock mode with all circuits activated. Figures 8–11 illustrate the available clocking modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, but it also drives the analog-to-digital conversion. SSTRB pulses high for two clock periods after the last bit of the control byte. Successive-approximation bit decisions are made and the results appear at DOUT on each of the next 14 SCLK falling edges (Figures 8 and10). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ is high.

Use internal clock mode if the serial clock frequency is less than 100kHz or if serial clock interruptions could cause the conversion interval to exceed 140µs. The conversion must complete in 140µs, or droop on the T/H capacitors can degrade conversion results.

Internal Clock

When configured for internal clock mode, the MAX1146–MAX1149 generate an internal conversion clock. This frees the µP from the burden of running the SAR conversion clock and allows the conversion results to be read back at the processor's convenience, at any clock rate up to 2.1MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB is low for a maximum of 8.0µs, during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the second falling SCLK clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figures 9 and 11).

For the most accurate conversion, the MAX1146–MAX1149 digital I/O should remain inactive during the internal clock conversion interval (t_{CONV}). Do not pull $\overline{CS}$ high during conversion. Pulling $\overline{CS}$ high aborts the current conversion. To ensure that the next start bit is recognized, clock in 18 zeros at DIN. When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high. A rising edge on SSTRB indicates that the MAX1146–MAX1149 have finished the conversion. The µP can then read the conversion results at its convenience.

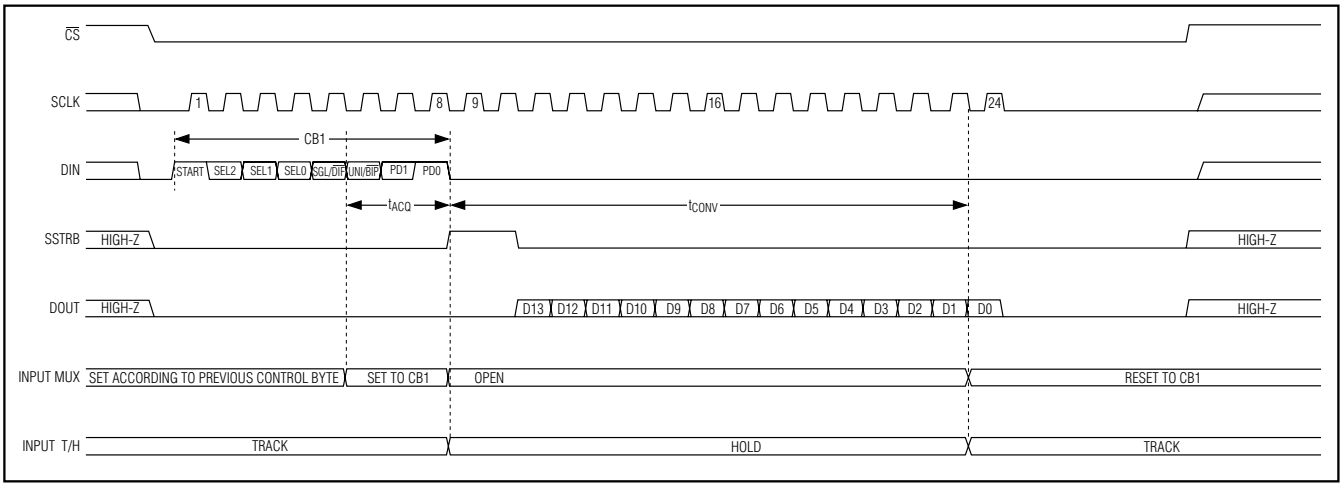

Figure 8. External Clock Mode—24 Clocks/Conversion Timing

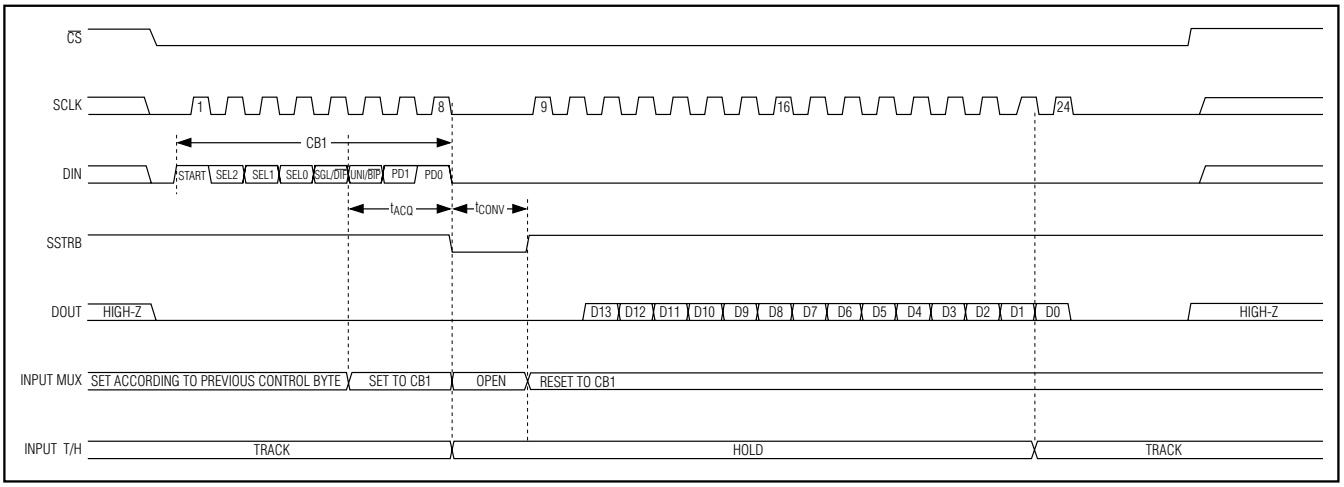

Figure 9. Internal Clock Mode Timing—24 Clocks/Conversion Timing

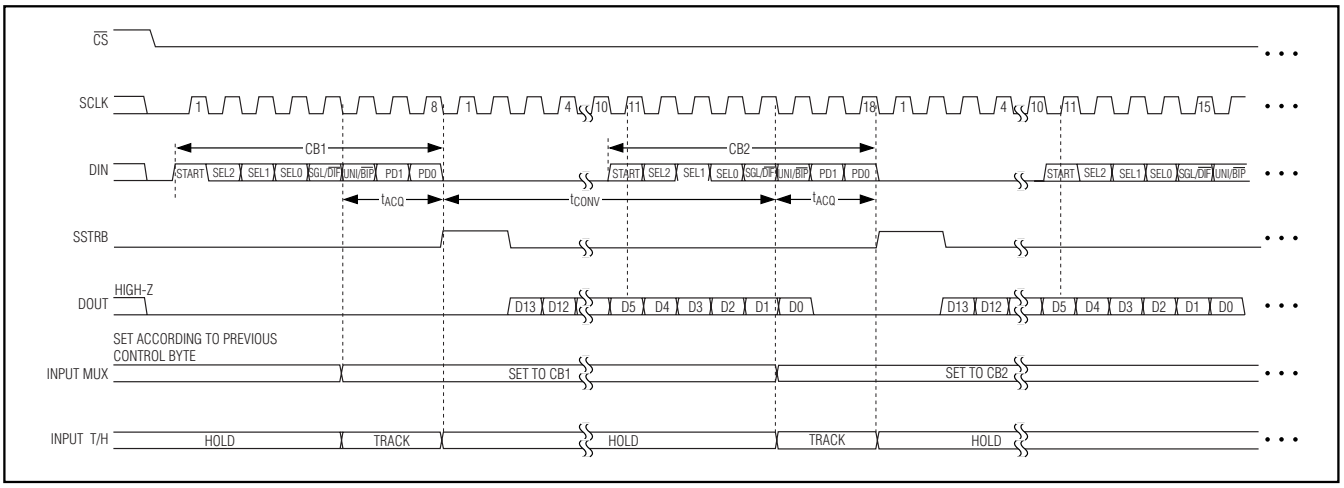

Figure 10. External Clock Mode—18 Clocks/Conversion Timing

Applications Information

Idle Mode

The device is considered idle when all the bits have been clocked out or 18 zeros have been clocked in on DIN.

Start Bit

The falling edge of $\overline{CS}$ alone does not start a conversion. The first logic high clocked into DIN with $\overline{CS}$ low is interpreted as a start bit and defines the first bit of the control byte. The device begins to track on the fifth falling edge of SCLK after a start bit has been recognized. A conversion starts on the eighth falling edge of SCLK as the last bit of the control byte is being clocked in. The start bit is defined as follows:

1) The first high bit clocked into DIN with $\overline{CS}$ low any time the converter is idle.

or

2) The first high bit clocked into DIN after bit 5 of a conversion in progress is clocked onto DOUT (Figures 10 and 11).

Toggling $\overline{CS}$ before the current conversion is complete aborts the conversion and clears the output register.

The fastest the MAX1146–MAX1149 can run with $\overline{CS}$ held low between conversions is 18 clocks per conversion. Figures 10 and 11 show the serial-interface timing necessary to perform a conversion every 18 SCLK cycles.

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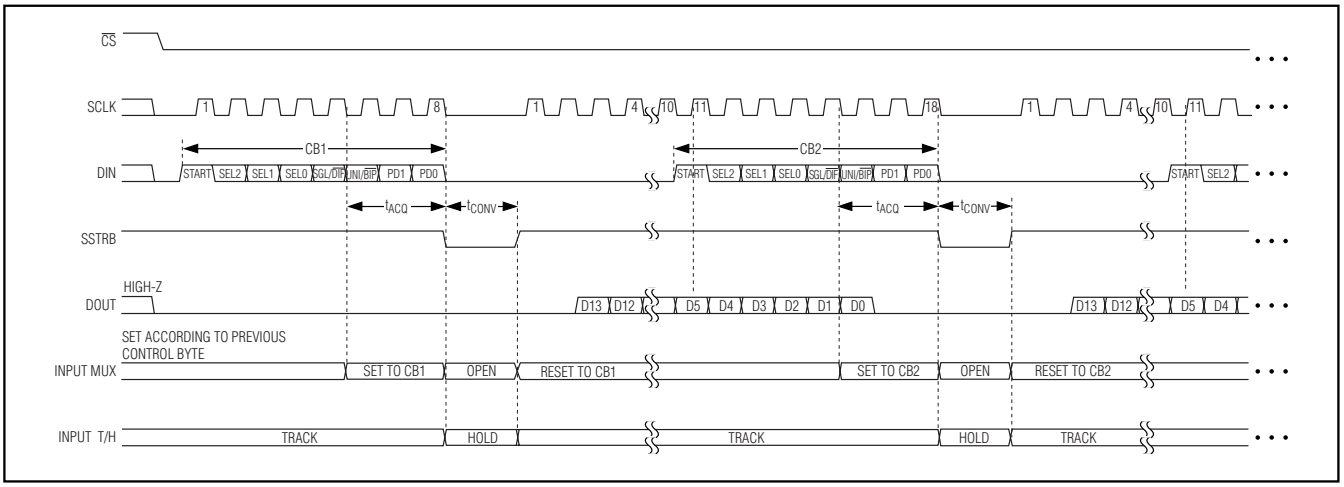


Figure 11. Internal Clock Mode—18 Clocks/Conversion Timing

Shutdown and Power-Down Modes

The MAX1146–MAX1149 provide a hardware shutdown and two software power-down modes.

Pulling $\overline{SHDN}$ low places the converter in hardware shutdown. The conversion is immediately terminated and the supply current is reduced to 300nA. Allow 2ms for the device to power-up when the internal reference buffer is used with C_{REFADJ} = 0.01µF and C_{REF} = 2.2µF. Larger capacitors on C_{REFADJ} and C_{REF} increase the power-up time (Table 6). No wake-up time is needed for the device to power-up from fast power-down when using an external reference.

Select a software power-down mode through the PD1 and PD0 bits of the control byte (Table 1). When the conversion in progress is complete, software power-down is initiated. The serial interface remains active and the last conversion result can be clocked out. In full power-down mode, only the serial interface remains operational and the supply current is reduced to 300nA. In fast power-down mode, only the bandgap reference and the serial interface remain operational, and the supply current is reduced to 600µA.

Table 6. Internal Reference Buffer Power-Up Times vs. Bypass Capacitors

C_{REFADJ}*	C_{REF}	POWER-UP TIMES FROM AN EXTENDED POWER-DOWN
0.01µF	4.7µF	2ms
0.1µF	10µF	25ms

**Power-up times are dominated by C_{REFADJ}.*

The MAX1146–MAX1149 automatically wake up from software power-down when they receive the control byte's start bit (Table 1). Allow 2ms for the device to power-up when the internal reference buffer is used with C_{REFADJ} = 0.01µF and C_{REF} = 2.2µF. Larger capacitors on C_{REFADJ} and C_{REF} increase the power-up time (Table 6). No wake-up time is needed for the device to power-up from fast power-down when using an external reference.

Reference Voltage

The MAX1146–MAX1149 can be used with an internal or external reference voltage. The reference voltage determines the ADC input range. The reference determines the full-scale output value (Table 7).

Internal Reference

The MAX1146–MAX1149 contain an internal 1.250V bandgap reference. This bandgap reference is connected to REFADJ through a 20kΩ resistor. Bypass REFADJ with a 0.01µF capacitor to AGND. The MAX1146/MAX1148 reference buffer has a 3.277V/V gain to provide +4.096V at REF. The MAX1147/MAX1149 reference buffer has a 2.000V/V gain to provide +2.500V at REF. Bypass REF with a minimum 2.2µF capacitor to AGND when using the internal reference.

External Reference

An external reference can be applied to the MAX1146–MAX1149 in two ways:

1) Disable the internal reference buffer by connecting REFADJ to V_{DD} and apply the external reference to REF (Figure 12).
2) Utilize the internal reference buffer by applying an external reference to REFADJ (Figure 13).

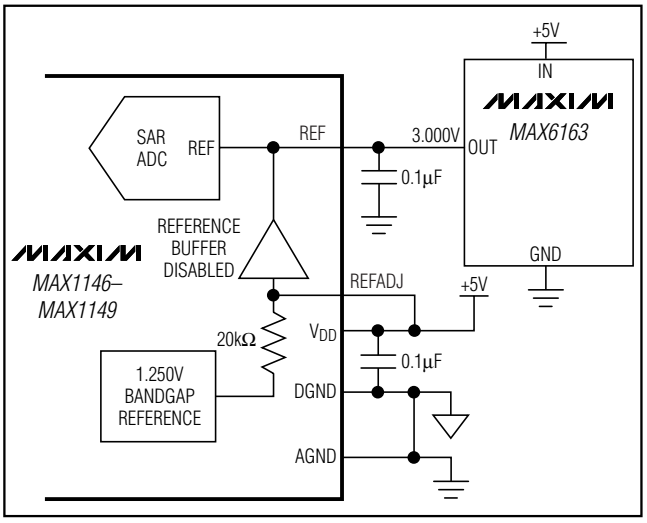


Figure 12. External Reference Applied to REF

Method 1 allows the direct application of an external reference from 1.5V to V_{DD} + 50mV. The REF input impedance is typically 10kΩ. During conversion, an external reference at REF must deliver up to 210µA and have an output impedance less than 10Ω. Bypass REF with a 0.1µF capacitor to AGND to improve its output impedance.

Method 2 utilizes the internal reference buffer to reduce the external reference load. The REFADJ input impedance is typically 20kΩ. During a conversion, an external reference at REFADJ must deliver at least 100µA and have an output impedance less than 100Ω. The MAX1146/MAX1148 reference buffer has a 3.277V/V gain and the MAX1147/MAX1149 has a gain of 2.000V/V. The external reference voltage at REFADJ multiplied by the reference buffer gain is the SAR ADC reference voltage. This reference appears at REF and must be from 1.5V to V_{DD} + 50mV. Bypass REFADJ with a 0.01µF capacitor and bypass REF with a 2.2µF capacitor to AGND.

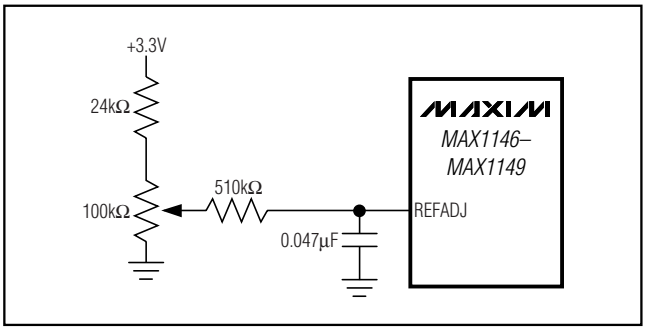


Figure 13. Reference Adjust Circuit

Transfer Function

Table 7 shows the full-scale voltage ranges for unipolar and bipolar modes.

Output data coding for the MAX1146–MAX1149 is binary in unipolar mode and two's complement binary in bipolar mode with 1 LSB = ($V_{REF}/2^N$), where N is the number of bits (14). Code transitions occur halfway between successive-integer LSB values. Figure 14 and Figure 15 show the input/output (I/O) transfer functions for unipolar and bipolar operations, respectively.

Serial Interfaces

The MAX1146–MAX1149 feature a serial interface that is fully compatible with SPI, QSPI, and MICROWIRE. If a serial interface is available, establish the CPU's serial interface as a master, so that the CPU generates the serial clock for the ADCs. Select a clock frequency up to 2.1MHz.

SPI and MICROWIRE Interface

When using an SPI (Figure 16a) or MICROWIRE interface (Figure 16b), set CPOL = CPHA = 0. Two 8-bit readings are necessary to obtain the entire 14-bit result from the ADC. DOUT data transitions on the serial clock's falling

Table 7. Full Scale and Zero Scale

INPUT AND OUTPUT MODES	UNIPOLAR MODE		BIPOLAR MODE		
	ZERO SCALE	FULL SCALE	NEGATIVE FULL SCALE	ZERO SCALE	POSITIVE FULL SCALE
Single-Ended Mode	V_{COM}	$V_{REF} + V_{COM}$	$\frac{-V_{REF}}{2} + V_{COM}$	V_{COM}	$\frac{+V_{REF}}{2} + V_{COM}$
Differential Mode	V_{IN-}	$V_{REF} + V_{IN-}$	$\frac{-V_{REF}}{2} + V_{IN-}$	V_{IN-}	$\frac{+V_{REF}}{2} + V_{IN-}$

Note: *The common mode range for the analog inputs is from AGND to V_{DD}.*

Multichannel, True-Differential, Serial, 14-Bit ADCs

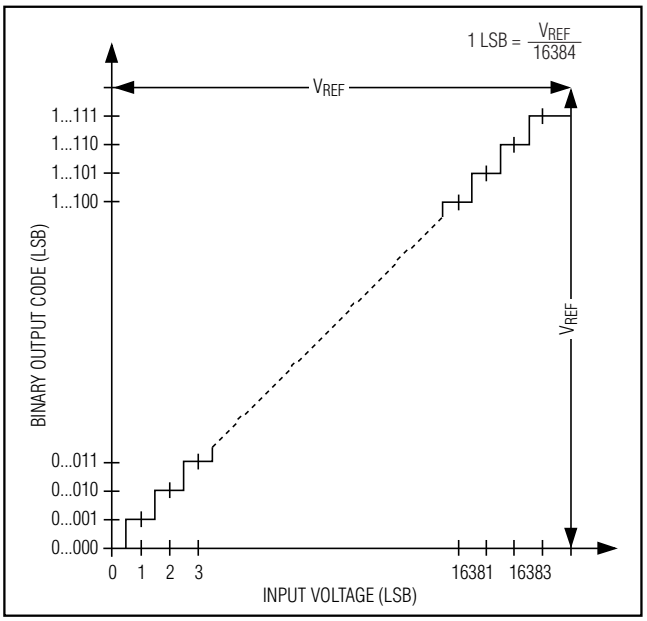


Figure 14. Unipolar Transfer Function

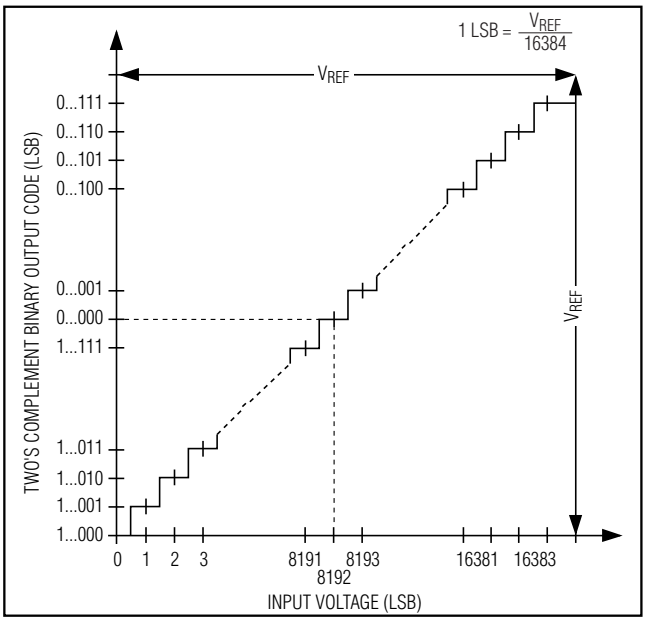


Figure 15. Bipolar Transfer Function

edge and is clocked into the µP on SCLK's rising edge. The first 8-bit data stream contains the first 8-bits of DOUT starting with the MSB. The second 8-bit data stream contains the remaining 6 result bits.

QSPI Interface

Using the high-speed QSPI interface (Figure 17) with CPOL = 0 and CPHA = 0, the MAX1146–MAX1149 support a maximum f_{SCLK} of 2.1MHz. One 16-bit reading is necessary to obtain the entire 14-bit result from the ADC. DOUT data transitions on the serial clock's falling edge and is clocked into the µP on SCLK's rising edge. The first 14 bits are the data.

PIC16/PIC17 SSP Module Interface

The MAX1146–MAX1149 are compatible with a PIC16/PIC17 microcontroller (µC), using the synchronous serial-port (SSP) module. To establish SPI communication, connect the controller as shown in Figure 18 and configure the PIC16/PIC17 as system master. Initialize the synchronous serial-port control register (SSPCON) and synchronous serial-port status register (SSPSTAT) to the bit patterns shown in Tables 8 and 9. In SPI mode, the PIC16/PIC17 µCs allow 8 bits of data to be synchronously transmitted and received simultaneously. Two consecutive 8-bit readings are necessary to obtain the entire 14-bit result from the ADC. DOUT data transitions on the serial clock's falling edge and is clocked into the µC on SCLK's rising edge. The first 8-bit data stream contains the first 8 data bits starting with the MSB. The second data stream contains the remaining bits, D5 through D0.

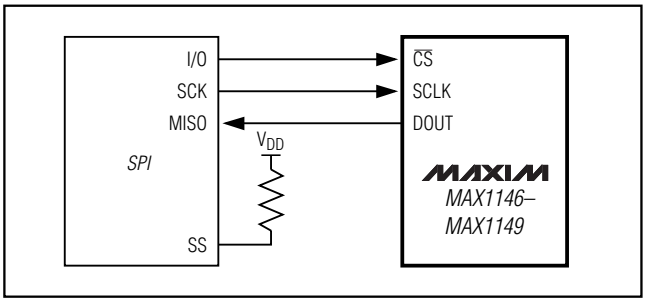


Figure 16a. SPI Connections

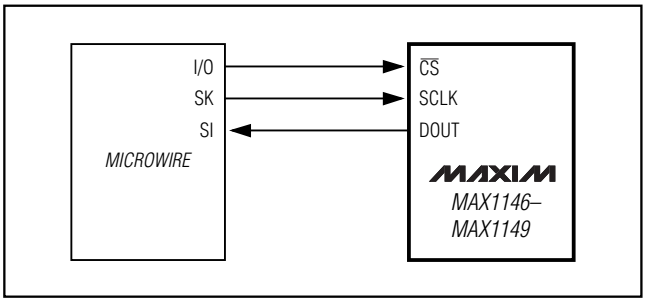


Figure 16b. MICROWIRE Connections

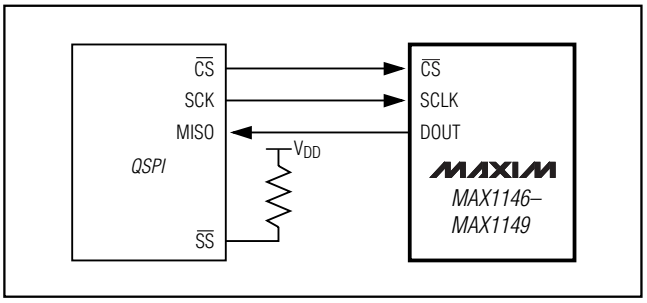


Figure 17. QSPI Connections

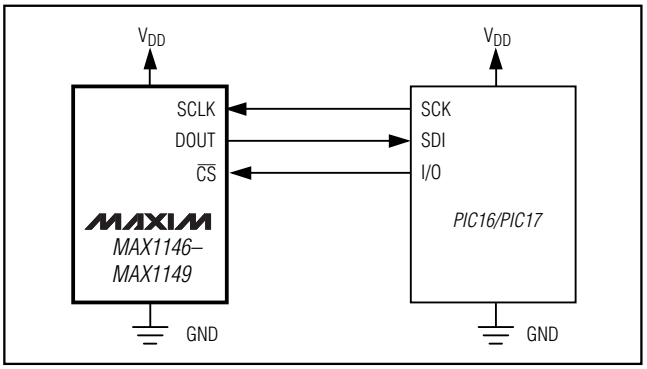


Figure 18. SPI Interface Connection for a PIC16/PIC17 Controller

Table 8. Detailed SSPCON Register Content

CONTROL BIT		PICI6/PICI7 SETTINGS	SYNCHRONOUS SERIAL-PORT CONTROL REGISTER (SSPCON)
WCOL	Bit 7	X	Write collision detection bit.
SSPOV	Bit 6	X	Receive overflow detect bit.
SSPEN	Bit 5	1	Synchronous serial port enable bit: 0: Disables serial port and configures these pins as I/O port pins. 1: Enables serial port and configures SCK, SDO, and SCI pins as serial-port pins.
CKP	Bit 4	0	Clock polarity select bit. CKP = 0 for SPI master mode selection.
SSPM3	Bit 3	0	Synchronous serial port mode select bit. Sets SPI master mode and selects $F_{CLK} = f_{OSC} / 16$.
SSPM2	Bit 2	0	
SSPM1	Bit 1	0	
SSPM0	Bit 0	1	

Table 9. Detailed SSPSTAT Register Content

CONTROL BIT		MAX1146–MAX1149 SETTINGS	SYNCHRONOUS SERIAL-PORT STATUS REGISTER (SSPSTAT)
SMP	Bit 7	0	SPI data input sample phase. Input data is sampled at the middle of the data output time.
CKE	Bit 6	1	SPI clock edge select bit. Data is transmitted on the rising edge of the serial clock.
D/A	Bit 5	X	Data address bit.
P	Bit 4	X	Stop bit.
S	Bit 3	X	Start bit.
R/W	Bit 2	X	Read/write bit information.
UA	Bit 1	X	Update address.
BF	Bit 0	X	Buffer full status bit.

Multichannel, True-Differential, Serial, 14-Bit ADCs

TMS32OLC3x Interface

Figure 19 shows an application circuit to interface the MAX1146–MAX1149 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 20. Use the following steps to initiate a conversion in the MAX1146–MAX1149 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR on the TMS320 are connected together with the MAX1146–MAX1149 SCLK input.
2) Drive the $\overline{CS}$ of the MAX1146–MAX1149 low through the XF_ I/O port of the TMS320 to clock data into the MAX1146–MAX1149 DIN.
3) Write an 8-bit word (1XXXXX11) to the MAX1146–MAX1149 to initiate a conversion and place the device into external clock mode. Refer to Table 1 to select the proper XXXXX bit values for your specific application.
4) The MAX1146–MAX1149 SSTRB output is monitored by the FSR input of the TMS320. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX1146–MAX1149.
5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 14-bit conversion result followed by 2 trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX1146–MAX1149 until the next conversion is initiated.

Layout, Grounding, and Bypassing

Careful PC board layout is essential for best system performance. Boards should have separate analog and digital ground planes. Ensure that digital and analog signals are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the device package.

Figure 4 shows the recommended system ground connections. Establish an analog ground point at AGND and a digital ground point at DGND. Connect all analog grounds to the star analog ground. Connect the digital grounds to the star digital ground. Connect the digital ground point to the analog ground point directly at the device. For lowest noise operation, the ground return to the star ground's power supply should be low impedance and as short as possible.

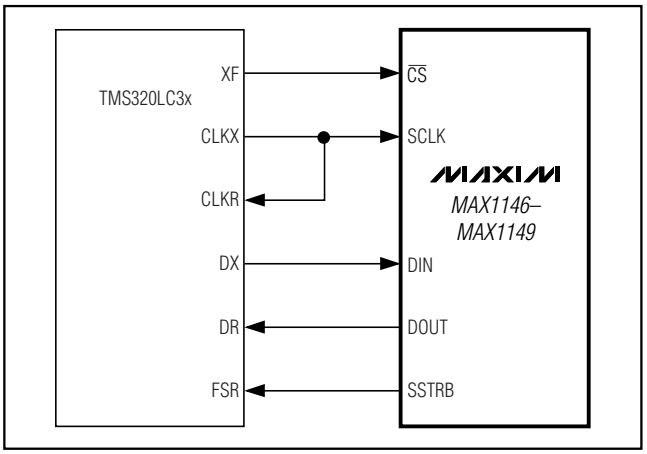


Figure 19. MAX1146–MAX1149-to-TMS320 Serial Interface

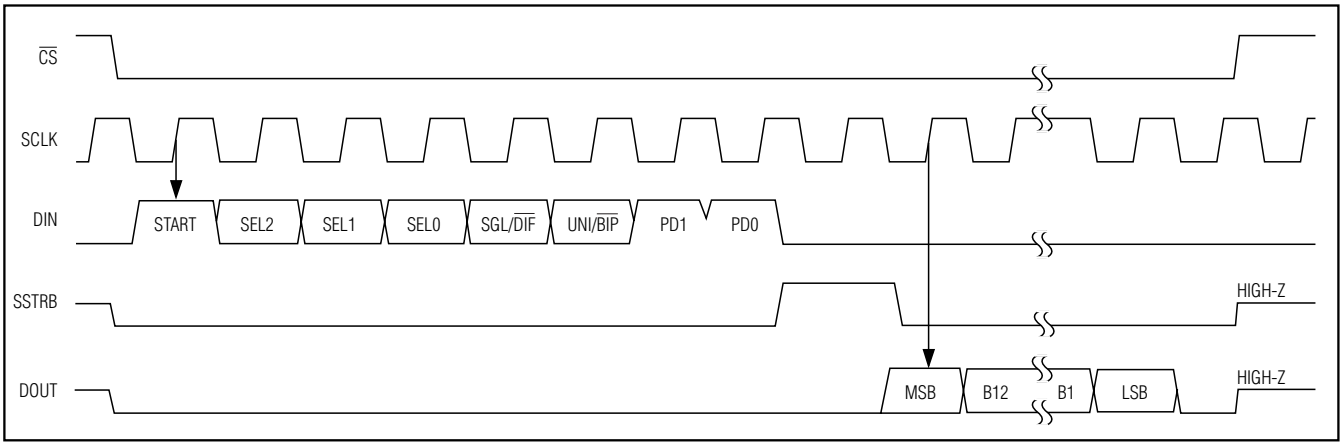


Figure 20. TMS320 Serial-Interface Timing Diagram

High-frequency noise in the V_{DD} power supply degrades the device's high-speed performance. Bypass the supply to the digital ground with 0.1µF and 4.7µF capacitors. Minimize capacitor lead lengths for best supply-noise rejection. Connect a 10Ω resistor in series with the 0.1µF capacitor to form a lowpass filter when the power supply is noisy.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1146–MAX1149 are measured using the end-point method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function.

Aperture Definitions

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between the samples. Aperture delay (t_{AD}) is the time between the rising edge of the sampling clock and the instant when an actual sample is taken.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to RMS equivalent of all other ADC output signals.

$$SINAD(dB) = 20 \times \log (SignalRMS / NoiseRMS)$$

Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the ENOB as follows:

$$ENOB = (SINAD - 1.76) / 6.02$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \left(\sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + V_5^2}{V_1}} \right)$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest distortion component.

Chip Information

TRANSISTOR COUNT: 5589

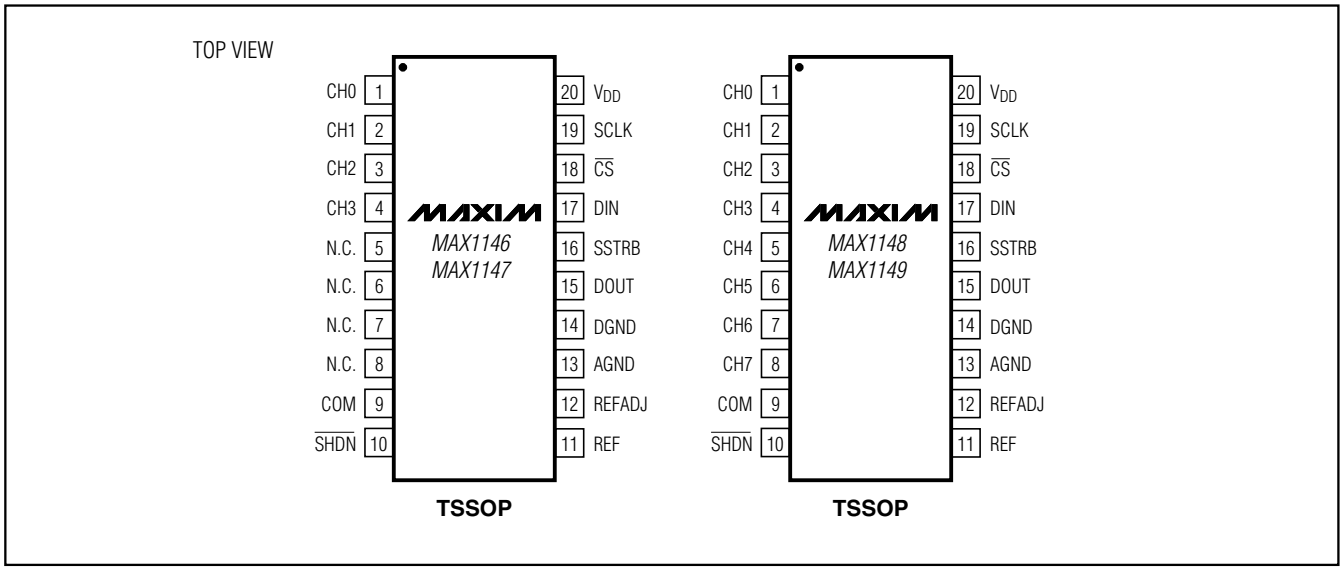
PROCESS: BiCMOS

Revision History

Pages changed at Rev 2: 1, 20, 23, 25.

Multichannel, True-Differential, Serial, 14-Bit ADCs

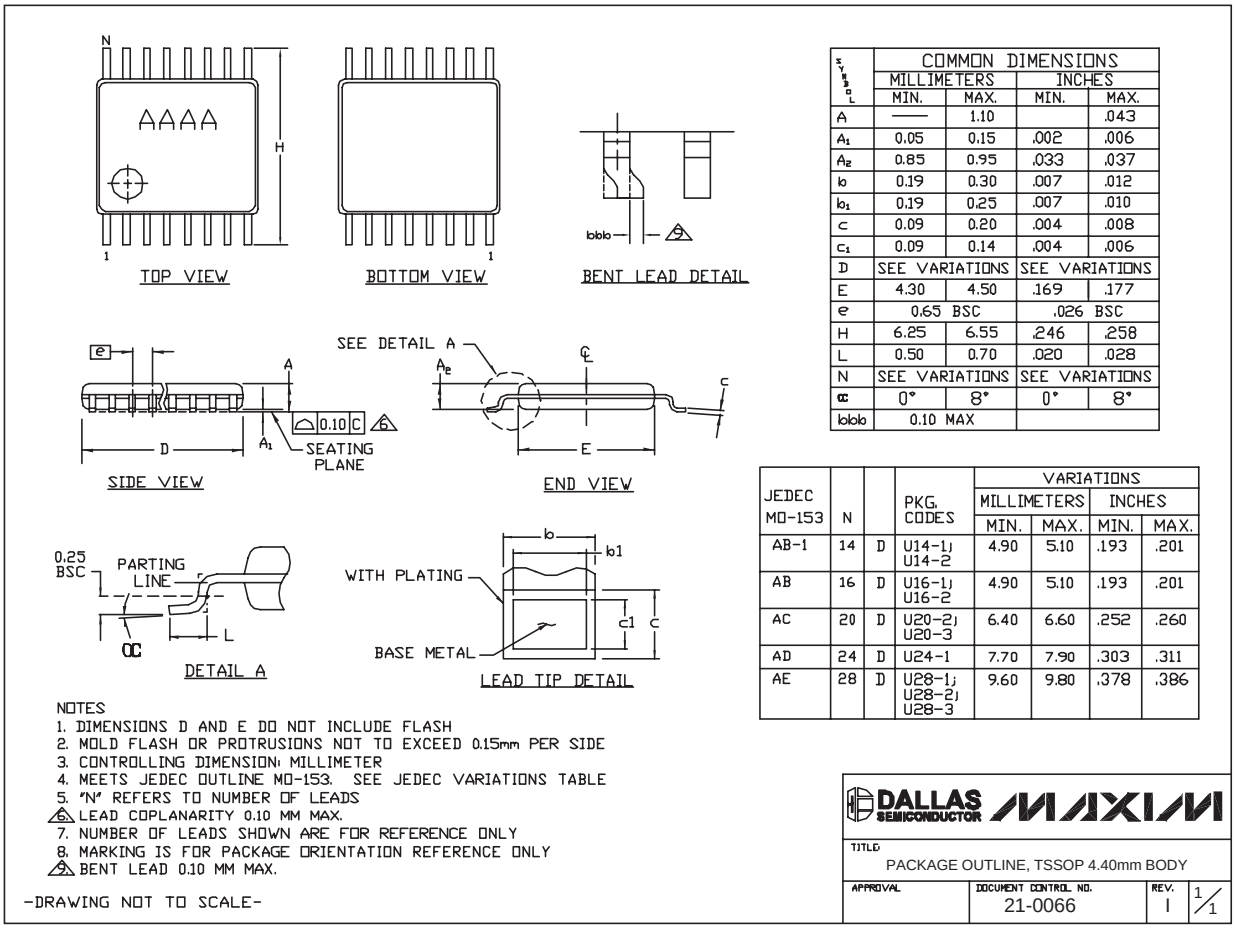
Pin Configurations



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	0.10 MAX			

JEDEC MO-153	N		PKG. CODES	VARIATIONS			
				MILLIMETERS		INCHES	
				MIN.	MAX.	MIN.	MAX.
AB-1	14	D	U14-1; U14-2	4.90	5.10	.193	.201
AB	16	D	U16-1; U16-2	4.90	5.10	.193	.201
AC	20	D	U20-2; U20-3	6.40	6.60	.252	.260
AD	24	D	U24-1	7.70	7.90	.303	.311
AE	28	D	U28-1; U28-2; U28-3	9.60	9.80	.378	.386

NOTES
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. LEAD COPLANARITY 0.10 MM MAX.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
9. BENT LEAD 0.10 MM MAX.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	I	1/1