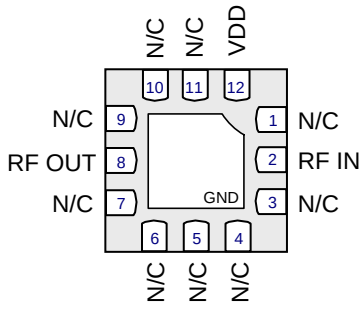
ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage, RF Off ..... 4 V
Drain Current ..... 40 mA
Total Power Dissipation ..... 0.15 W
RF Input Power ..... +10 dBm
Operation Ambient Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to 150°C
Package Peak Temp. for Solder Reflow (40 seconds maximum exposure) ... 260°C (+0 -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

PACKAGE PIN OUT



LL PACKAGE
(Bottom View)

RoHS / Pb-free NiPdAu Lead Finish

FUNCTIONAL PIN DESCRIPTION

Name	Pin #	Description
RF IN	2	RF Input for the low noise amplifier. This pin is DC-shorted to GND but AC-coupled to the transistor gate.
RF OUT	8	RF Output for the low noise amplifier. This pin is AC-coupled and does not require a DC-blocking capacitor.
VDD	12	Supply Voltage.
GND	Center Metal	The center metal base of the MLP package provides both DC and RF ground.
N/C	1,3,4,5,6,7, 9,10,11	Not Used. They may be treated either as open pins or connected to the ground.

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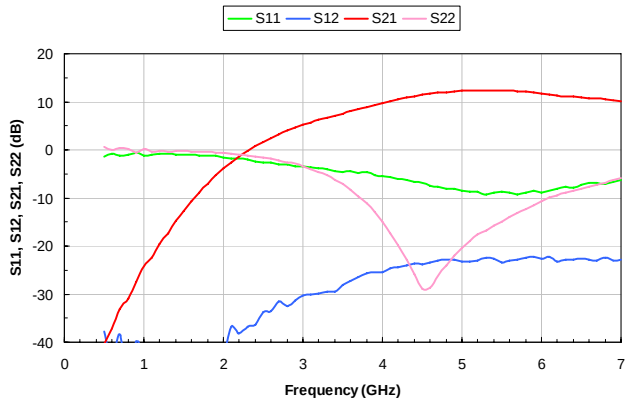
ELECTRICAL CHARACTERISTICS

Nominal test conditions: V_{DD} = 3.3V, I_{DD} = 9.5mA, T_A = 25°C (Room Temperature)

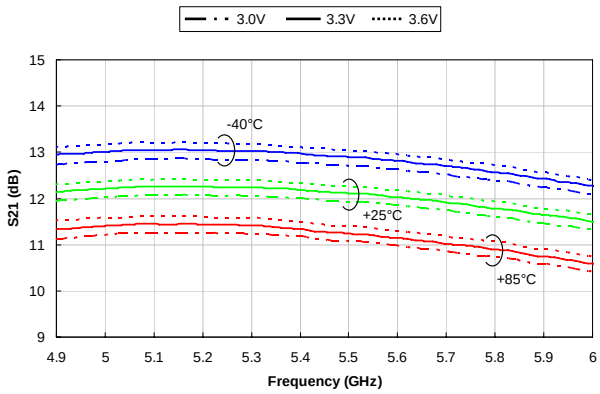
Parameter	Symbol	Test Conditions	LX5560			Units
			Min	Typ	Max	
Application Frequency Range	f		4.9		6	GHz
Small-Signal Gain	S21			12		dB
Noise Figure	NF	Room Temperature		1.7	2.1	dB
Input 3rd Order Intercept Point	IIP3	Freq. 1 = 5.25 GHz, Freq. 2 = 5.27 GHz		6		dBm
Input P1dB	IP1dB	Freq. = 5.5 GHz		2		dBm
Input Return Loss	S11			9		dB
Output Return Loss	S22			10		dB
Supply Voltage	V_{DD}			3.3		V
Supply Current	I_{DD}			9.5		mA

S-PARAMETER

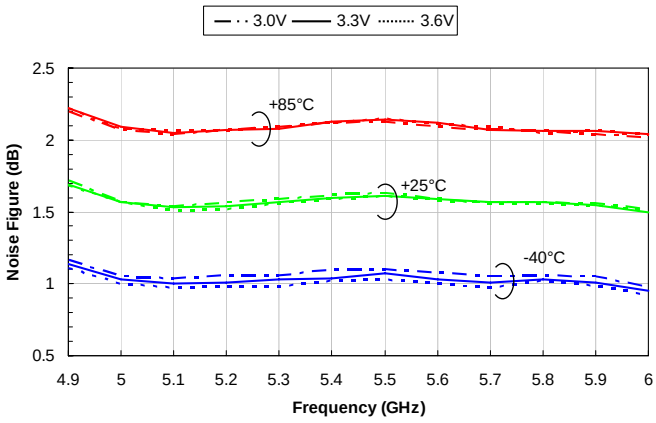


Typical S-Parameter Data at Room Temperature
(Vdd = 3.3V, Idd = 9.5mA at Room Temperature)

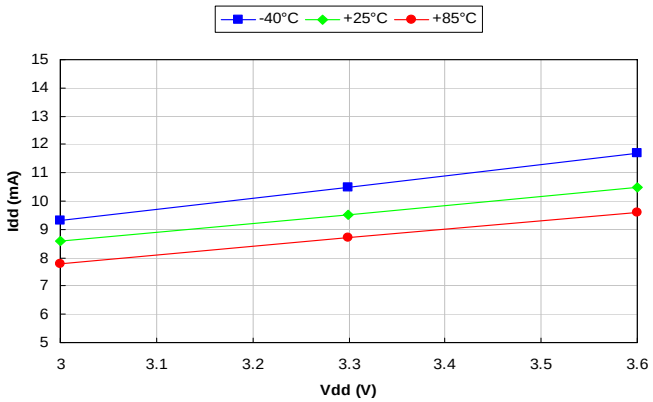
GAIN OVER TEMP



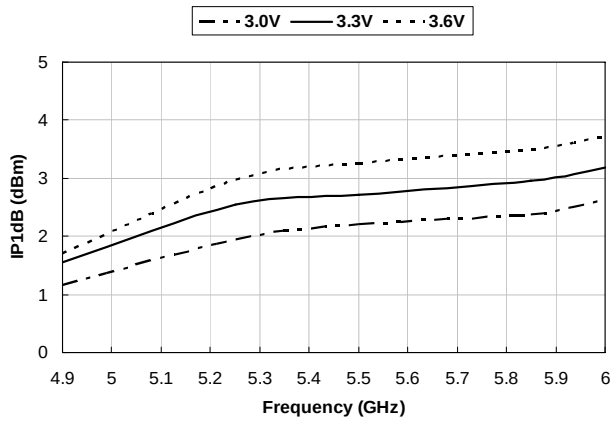
NOISE FIGURE OVER TEMP



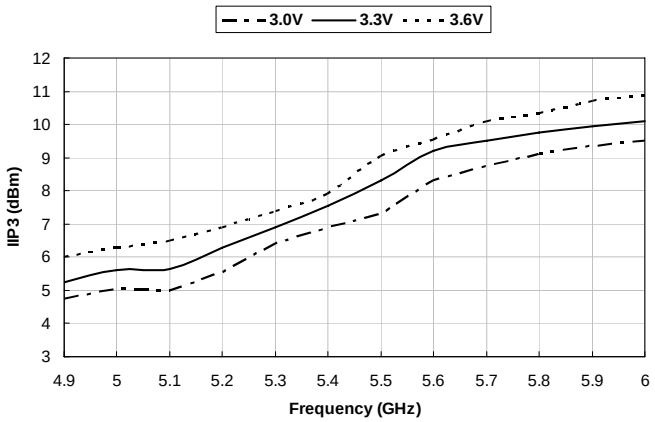
CURRENT OVER TEMP



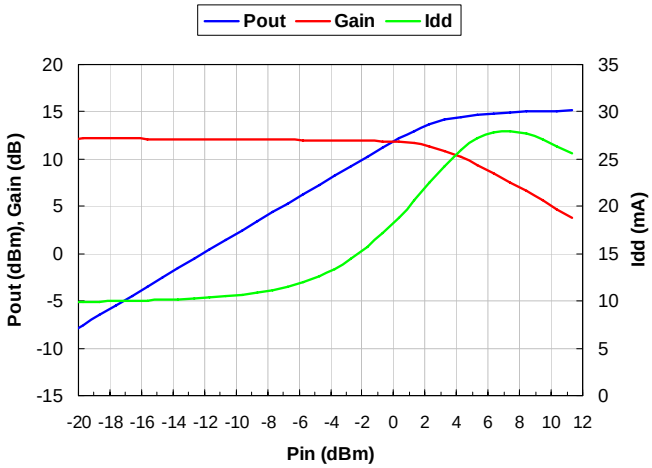
INPUT P1DB (+25°C)



INPUT IP3 (+25°C)

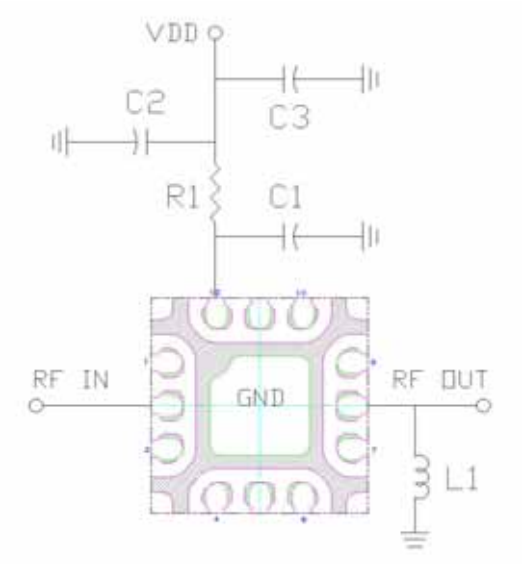


POWER SWEEP @ 5.5GHz



(Vdd=3.3V, Idq=9.5mA at Room Temperature)

APPLICATION SCHEMATIC



BOM LIST

Reference Designator	Part Description	Case
C1	Capacitor, 1 pF	0402
C2	Capacitor,1 µF	0603
C3	Capacitor,10 µF	0805
L1	Inductor, 1.5 nH (TOKO : LL1005-FH1N5S)	0402
R1	Resistor, 30 Ohm	0402

NOTES

- It is recommended to place C1 at ~30mil from MLP package outline.
- It is recommended to place L1 at ~30mil from MLP package outline.
- C2 and C3 are used for standalone evaluation board test only. They can be replaced with a 1nF(0402) in final applications.

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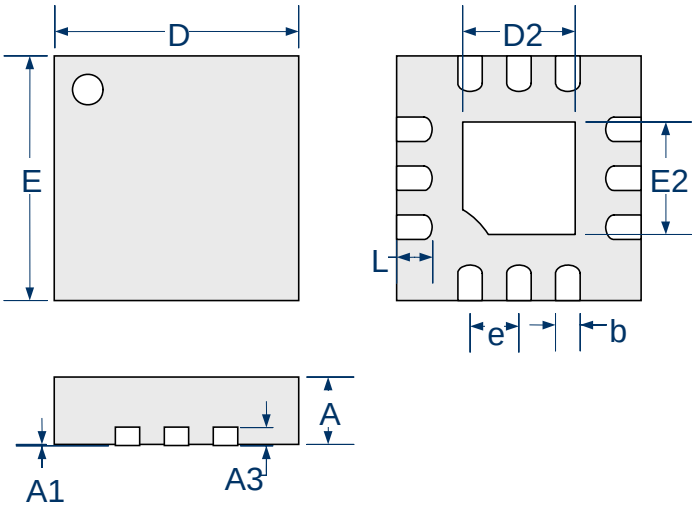
PACKAGE DIMENSIONS

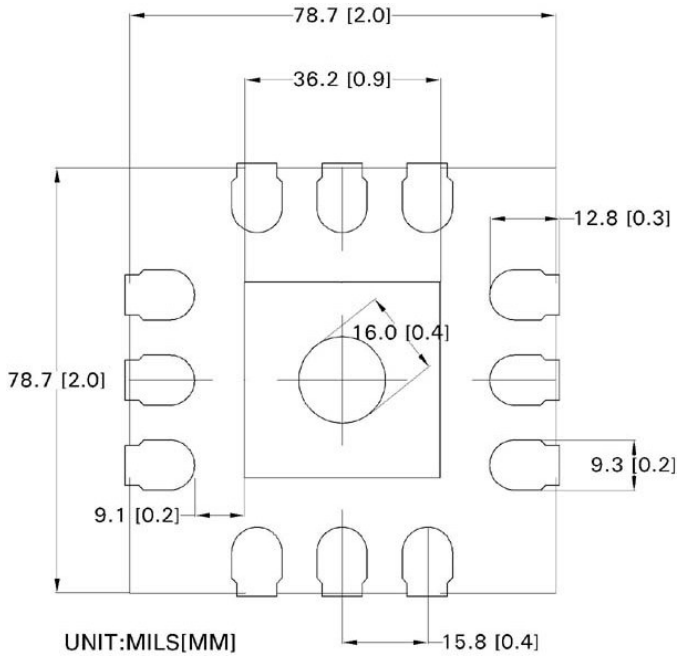
LL 12-Pin MLPQ Plastic (2x2mm)



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.40	0.50	0.016	0.020
A1	0.00	0.05	0.000	0.002
A3	0.15 REF		0.006 REF	
b	0.15	0.25	0.006	0.010
D	2.00 BSC		0.079 BSC	
D2	0.77	1.02	0.030	0.040
E	2.00 BSC		0.079 BSC	
E2	0.77	1.02	0.030	0.040
e	0.40 BSC		0.016 BSC	
L	0.19	0.39	0.007	0.015

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.



Recommended Land Pattern

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NOTES

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