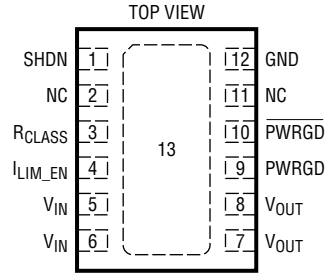
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{IN} Voltage ..... 0.3V to –90V
V_{OUT} Voltage ..... V_{IN} + 90V (and ≤ GND) to V_{IN} – 0.3V
SHDN Voltage ..... V_{IN} + 90V to V_{IN} – 0.3V
R_{CLASS}, I_{LIM_EN} Voltage ..... V_{IN} + 7V to V_{IN} – 0.3V
PWRGD Voltage (Note 3)
  Low Impedance Source .... V_{OUT} + 11V to V_{OUT} – 0.3V
  Current Fed 5mA
$\overline{PWRGD}$ Voltage ..... V_{IN} + 80V to V_{IN} – 0.3V
PWRGD Current 10mA
R_{CLASS} Current 100mA
Operating Ambient Temperature Range
  LTC4264C ..... 0°C to 70°C
  LTC4264I ..... –40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PACKAGE/ORDER INFORMATION



DE12 PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W, θ_{JC} = 4.3°C/W
EXPOSED PAD (PIN 13) MUST BE SOLDERED TO AN ELECTRICALLY ISOLATED HEAT SINK

ORDER PART NUMBER	DE PART MARKING*
LTC4264CDE LTC4264IDE	4264 4264

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.
*The temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Supply Voltage	Voltage with Respect to GND Pin					
	IEEE 802.3af System	(Notes 5, 6, 7, 8)	●			–57	V
	Signature Range		●	–1.5		–10.1	V
	Classification Range		●	–12.5		–21	V
	UVLO Turn-On Voltage		●	–37.7	–38.9	–40.2	V
	UVLO Turn-Off Voltage		●	–29.8	–30.6	–31.5	V
I_{IN_ON}	IC Supply Current when On	V_{IN} = –54V	●			3	mA
I_{IN_CLASS}	IC Supply Current During Classification	V_{IN} = –17.5V (Note 9)	●	0.55	0.62	0.70	mA
ΔI_{CLASS}	Current Accuracy During Classification	10mA < I_{CLASS} < 75mA, –12.5V ≤ V_{IN} ≤ –21V (Notes 10,11)	●			±3.5	%
$t_{CLASSRDY}$	Classification Stability Time	V_{IN} Stepped 0V to –17.5V, I_{IN_CLASS} ≤3.5% of Ideal, 10mA < I_{CLASS} < 75mA (Notes 10, 11)	●			1	ms
$R_{SIGNATURE}$	Signature Resistance	–1.5V ≤ V_{IN} ≤ –10.1V, IEEE 802.3af 2-Point Measurement, SHDN Tied to V_{IN} (Notes 6, 7)	●	23.25		26.00	kΩ
$R_{INVALID}$	Invalid Signature Resistance	–1.5V ≤ V_{IN} ≤ –10.1V, IEEE 802.3af 2-Point Measurement, SHDN Tied to GND (Notes 6, 7)	●		10	11.8	kΩ
V_{IH_SHDN}	SHDN High Level Input Voltage	With Respect to V_{IN}, High Level = Shutdown (Note 12)	●	3		57	V
V_{IL_SHDN}	SHDN Low Level Input Voltage	With Respect to V_{IN}	●			0.45	V
R_{INPUT_SHDN}	SHDN Input Resistance	With Respect to V_{IN}	●	100			kΩ
V_{IH_ILIM}	I_{LIM_EN} High Level Input Voltage	With Repect to V_{IN}, High Level Enables Current Limit (Note 13)	●	4			V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IL_ILIM}	I_{LIM_EN} Low Level Input Voltage	With Respect to V_{IN} (Note 13)	●			1	V
$V_{\overline{PWRGD}\_OUT}$	Active Low Power Good Output Low Voltage	$I_{\overline{PWRGD}}$ = 1mA, V_{IN} = –54V, $\overline{PWRGD}$ Referenced to V_{IN}	●			0.5	V
$I_{\overline{PWRGD}\_LEAK}$	Active Low Power Good Leakage	V_{IN} = 0V, $V_{\overline{PWRGD}}$ = 57V	●			1	µA
V_{PWRGD_OUT}	Active High Power Good Output Low Voltage	I_{PWRGD} = 0.5mA, V_{IN} = –52V, V_{OUT} = –4V, PWRGD Referenced to V_{OUT} (Note 14)	●			0.35	V
V_{PWRGD_VCLAMP}	Active High Power Good Voltage-Limiting Clamp	I_{PWRGD} = 2mA, V_{OUT} = 0V, With Respect to V_{OUT} (Note 3)	●	12.0	14.0	16.5	V
I_{PWRGD_LEAK}	Active High Power Good Leakage	V_{PWRGD} = 11V, with Respect to V_{OUT}, V_{OUT} = V_{IN} = –54V	●			1	µA
R_{ON}	On Resistance	I = 700mA, V_{IN} = –54V Measured from V_{IN} to V_{OUT} (Note 11)	 ●		0.5	0.6 0.8	Ω Ω
I_{OUT_LEAK}	V_{OUT} Leakage	V_{IN} = –57V, GND = SHDN = V_{OUT} = 0V	●			1	µA
I_{LIMIT_HIGH}	Input Current Limit During Normal Operation	V_{IN} = –54V, V_{OUT} = –53V, I_{LIM_EN} Floating (Notes 15, 16)	●	700	750	800	mA
I_{LIMIT_LOW}	Inrush Current Limit	V_{IN} = –54V, V_{OUT} = –53V (Notes 15, 16)	●	250	300	350	mA
I_{LIMIT_DISA}	Safeguard Current Limit when I_{LIMIT_HIGH} Disabled	V_{IN} = –54V, V_{OUT} = –52.5V, I_{LIM_EN} Tied to V_{IN} (Notes 15, 16, 17)		1.20	1.45	1.65	A

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are with respect to GND pin unless otherwise noted.

Note 3: Active high PWRGD pin internal clamp circuit self-regulates to 14V with respect to V_{OUT}.

Note 4: The LTC4264 operates with a negative supply voltage in the range of –1.5V to –57V. To avoid confusion, voltages in this data sheet are referred to in terms of absolute magnitude.

Note 5: In IEEE 802.3af systems, the maximum voltage at the PD jack is defined to be –57V. See Applications Information.

Note 6: The LTC4264 is designed to work with two polarity protection diodes in series with the input. Parameter ranges specified in the Electrical Characteristics are with respect to LTC4264 pins and are designed to meet IEEE 802.3af specifications when the drop from the two diodes is included. See Applications Information.

Note 7: Signature resistance is measured via the two-point ΔV/ΔI method as defined by IEEE 802.3af. The LTC4264 signature resistance is offset from 25k to account for diode resistance. With two series diodes, the total PD resistance will be between 23.75k and 26.25k and meet IEEE 802.3af specifications. The minimum probe voltages measured at the LTC4264 pins are – 1.5V and – 2.5V. The maximum probe voltages are –9.1V and –10.1V.

Note 8: The LTC4264 includes hysteresis in the UVLO voltages to preclude any start-up oscillation. Per IEEE 802.3af requirements, the LTC4264 will power up from a voltage source with 20Ω series resistance on the first trial.

Note 9: I_{IN_CLASS} does not include classification current programmed at Pin 3. Total supply current in classification mode will be I_{IN_CLASS} + I_{CLASS} (see Note 10).

Note 10: I_{CLASS} is the measured current flowing through R_{CLASS}. ΔI_{CLASS} accuracy is with respect to the ideal current defined as I_{CLASS} = 1.237/R_{CLASS}. $t_{CLASSRDY}$ is the time for I_{CLASS} to settle to within ±3.5% of ideal. The current accuracy specification does not include variations in R_{CLASS} resistance. The total classification current for a PD also includes the IC quiescent current (I_{IN_CLASS}). See Applications Information.

Note 11: This parameter is assured by design and wafer level testing.

Note 12: To disable the 25k signature, tie SHDN to GND (±0.1V) or hold SHDN pin high with respect to V_{IN}. See Applications Information.

Note13: I_{LIM_EN} pin is pulled high internally and for normal operation should be left floating. To disable high level current limit, tie I_{LIM_EN} to V_{IN}. See Applications Information.

Note 14: Active high power good is referenced to V_{OUT} and is valid for GND-V_{OUT} ≥ 4V. Measured at –52V due to test hardware limitations.

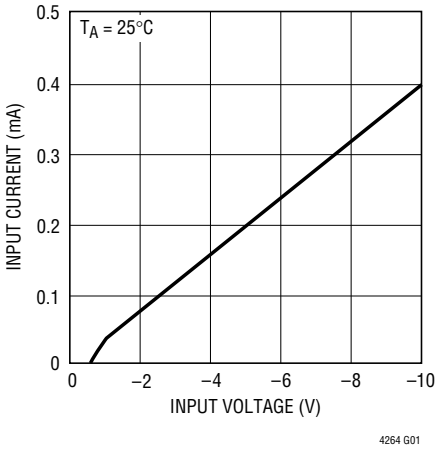
Note 15: The LTC4264 includes a dual current limit. At turn-on, before C1 is charged, the LTC4264 current level is set to I_{LIMIT_LOW}. After C1 is charged and with I_{LIM_EN} floating, the LTC4264 switches to I_{LIMIT_HIGH}. With I_{LIM_EN} pin tied low, the LTC4264 switches to I_{LIMIT_DISA}. The LTC4264 stays in I_{LIMIT_HIGH} or I_{LIMIT_DISA} until the input voltage drops below the UVLO turn-off threshold or a thermal overload occurs.

Note 16: The LTC4264 features thermal overload protection. In the event of an overtemperature condition, the LTC4264 will turn off the power MOSFET, disable the classification load current and present an invalid power good signal. Once the LTC4264 cools below the overtemperature limit, the LTC4264 current limit switches to I_{LIMIT_LOW} and normal operation resumes. Thermal overload protection is intended to protect the device during momentary fault conditions and continuous operation in thermal overload should be avoided as it may impair device reliability.

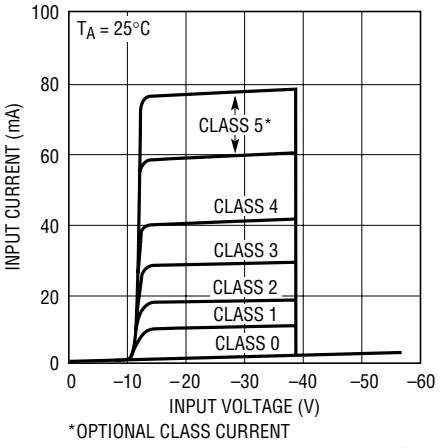
Note 17: I_{LIMIT_DISA} is a safeguard current limit that is activated when the normal input current limit (I_{LIMIT_HIGH}) is defeated using the I_{LIM_EN} pin. Currents at or near I_{LIMIT_DISA} will cause significant package heating and may require a reduced maximum ambient operating temperature in order to avoid tripping the thermal overload protection. See Applications Information.

TYPICAL PERFORMANCE CHARACTERISTICS

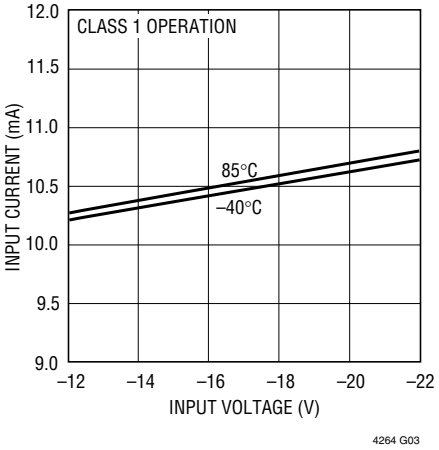
Input Current vs Input Voltage 25k Detection Range



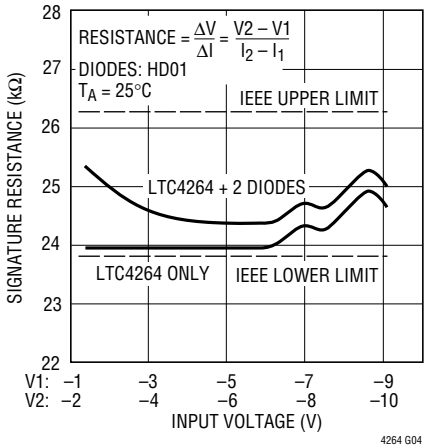
Input Current vs Input Voltage



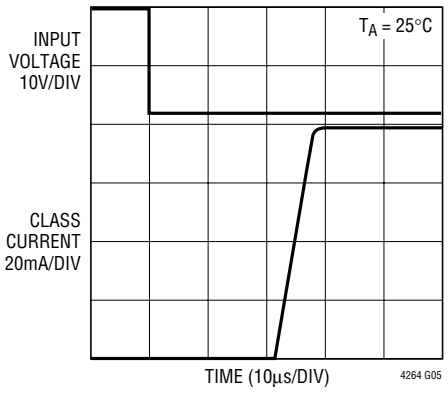
Input Current vs Input Voltage



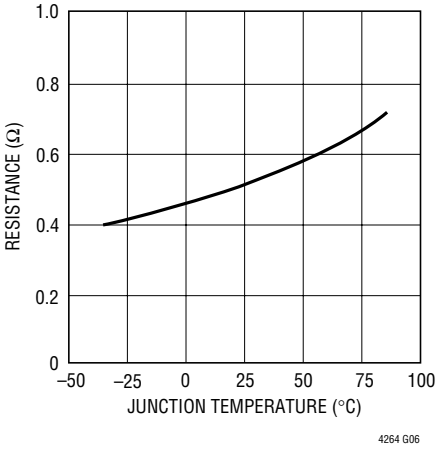
Signature Resistance vs Input Voltage



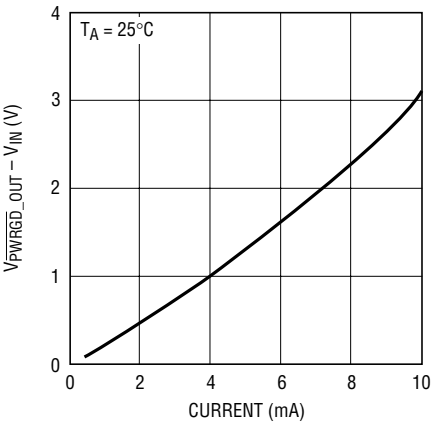
Class Operation vs Time



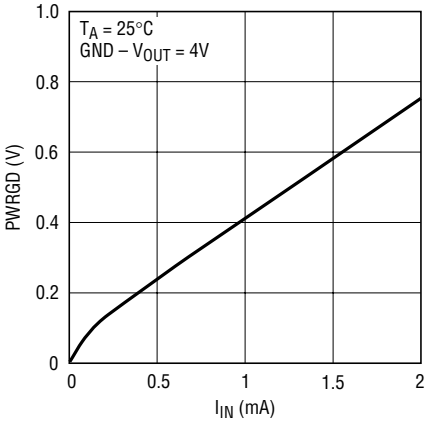
On Resistance vs Temperature



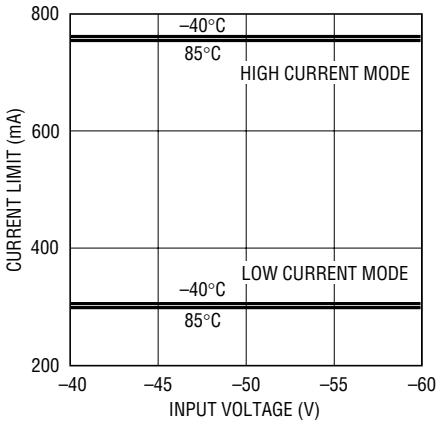
Active Low $\overline{\text{PWRGD}}$ Output Low Voltage vs Current



Active High PWRGD Output Low Voltage vs Current



Current Limit vs Input Voltage



PIN FUNCTIONS

SHDN (Pin 1): Shutdown Input. Used to command the LTC4264 to present an invalid signature. Connecting SHDN to GND lowers the signature resistance to an invalid value and disables other LTC4264 operations. If unused, tie SHDN to V_{IN}.

NC (Pin 2): No Internal Connection.

R_{CLASS} (Pin 3): Class Select Input. Used to set the current the LTC4264 maintains during classification. Connect a resistor between R_{CLASS} and V_{IN}. (See Table 2.)

I_{LIM_EN} (Pin 4): Input Current Limit Enable. Used to control LTC4264 current limit behavior during powered operation. For normal operation, float I_{LIM_EN} to enable I_{LIMIT_HIGH} current. Tie I_{LIM_EN} to V_{IN} to disable input current limit. Note that the inrush current limit does not change with I_{LIM_EN} selection. See Applications Information.

V_{IN} (Pins 5, 6): Power Input. Tie to the PD input through the diode bridge. Pins 5 and 6 must be electrically tied together.

V_{OUT} (Pins 7, 8): Power Output. Supplies power to the PD load through the internal power MOSFET. V_{OUT} is high impedance until the input voltage rises above the UVLO turn-on threshold. The output is then connected to V_{IN} through a current-limited internal MOSFET switch. Pins 7 and 8 must be electrically tied together.

PWRGD (Pin 9): Active High Power Good Output, Open Collector. Signals to the DC/DC converter that the LTC4264 MOSFET is on and that the converter can start operation. High impedance indicates power is good. PWRGD is referenced to V_{OUT} and is low impedance during inrush and in the event of a thermal overload. PWRGD is clamped 14V above V_{OUT}.

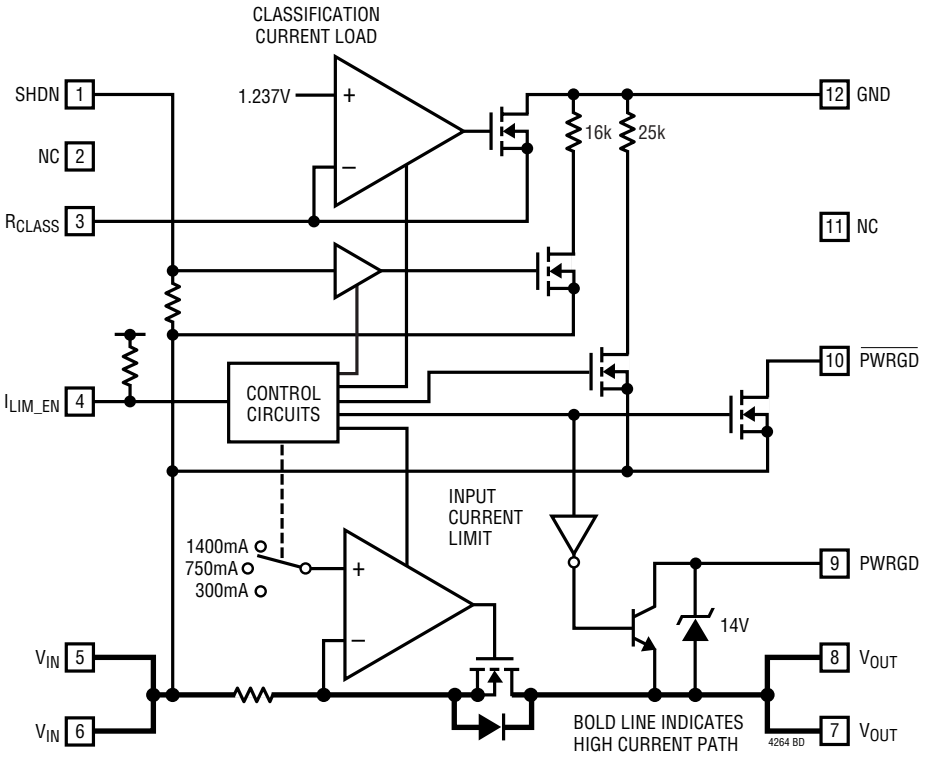
$\overline{\text{PWRGD}}$ (Pin 10): Active Low Power Good Output, Open-Drain. Signals to the DC/DC converter that the LTC4264 MOSFET is on and that the converter can start operation. Low impedance indicates power is good. PWRGD is referenced to V_{IN} and is high impedance during detection, classification and in the event of a thermal overload. $\overline{\text{PWRGD}}$ has no internal clamps.

NC (Pin11): No Internal Connection.

GND (Pin 12): Ground. Tie to system ground and power return through the input diode bridge.

Exposed Pad (Pin 13): Must be soldered to electrically isolated heat sink.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

OVERVIEW

Power over Ethernet (PoE) continues to gain popularity as more products are taking advantage of having DC power and high speed data available from a single RJ45 connector. As PoE is becoming established in the marketplace, Powered Device (PD) equipment vendors are running into the 12.95W power limit established by the IEEE 802.3af standard. To solve this problem and expand the application of PoE, the LTC4264 breaks the power barrier by allowing custom PoE applications to deliver up to 35W for power-hungry PoE applications such as dual band and 802.11n access points, RFID readers and PTZ security cameras.

The LTC4264 is designed to interface with custom Power Sourcing Equipment (PSE) to deliver higher power levels to the PD load. Off-the-shelf high power PSEs are available today from a variety of vendors for use with the LTC4264 to allow quick implementation of a custom system. Alternately, the system vendor can choose to build their own high power PSE. Linear Technology provides complete application information for high power PSE solutions delivering up to 35W for 2-pair systems and as much as 70W when used in 4-pair systems.

One of the basic architectural decisions associated with a high power PoE system is whether to deliver power using four conductors (2-pair) or all eight conductors (4-pair). Each method provides advantages and the system vendor needs to decide which method best suits their application.

2-pair power is used today in 802.3af systems (see Figure 1). One pair of conductors is used to deliver the current and a second pair is used for the return while two conductor pairs are not powered. This architecture offers the simplest implementation method but suffers from higher cable loss than an equivalent 4-pair system.

4-pair power delivers current to the PD via two conductor pairs in parallel (Figure 2). This lowers the cable resistance but raises the issue of current balance between each conductor pair. Differences in resistance of the transformer, cable and connectors along with differences in diode bridge forward voltage in the PD can cause an imbalance in the currents flowing through each pair. The 4-pair system in Figure 2 solves this problem by using two independent DC/DC converters in the PD. Using this architecture solves the balancing issue and allows the PD to be driven by two independent PSEs, for example an Endpoint PSE and a Midspan PSE. Contact Linear Technology applications support for detailed information on implementing 2-pair and 4-pair PoE systems.

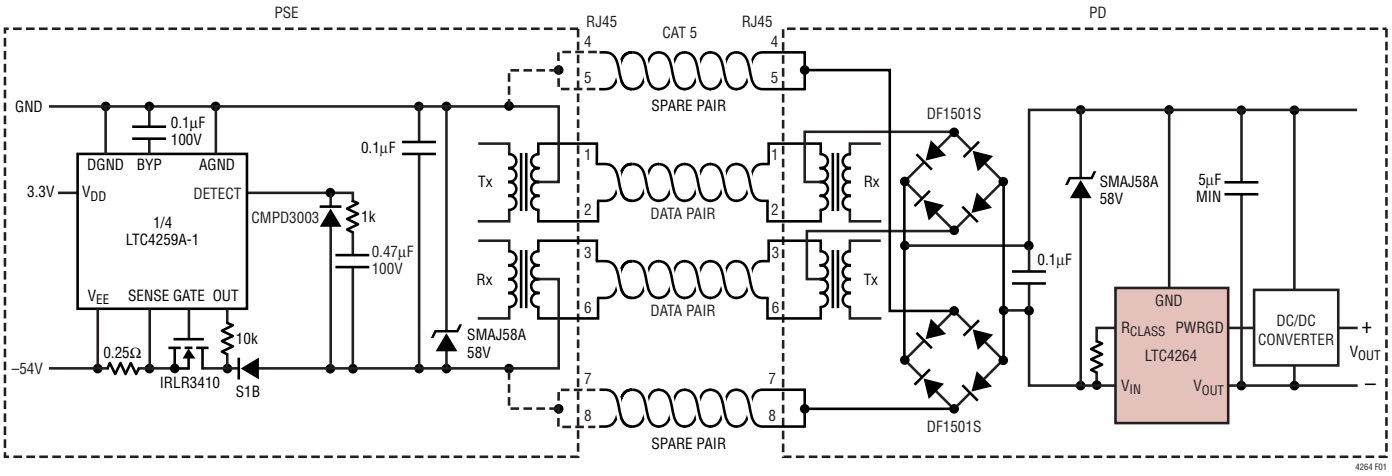


Figure 1. 2-Pair High Power PoE System Diagram

APPLICATIONS INFORMATION

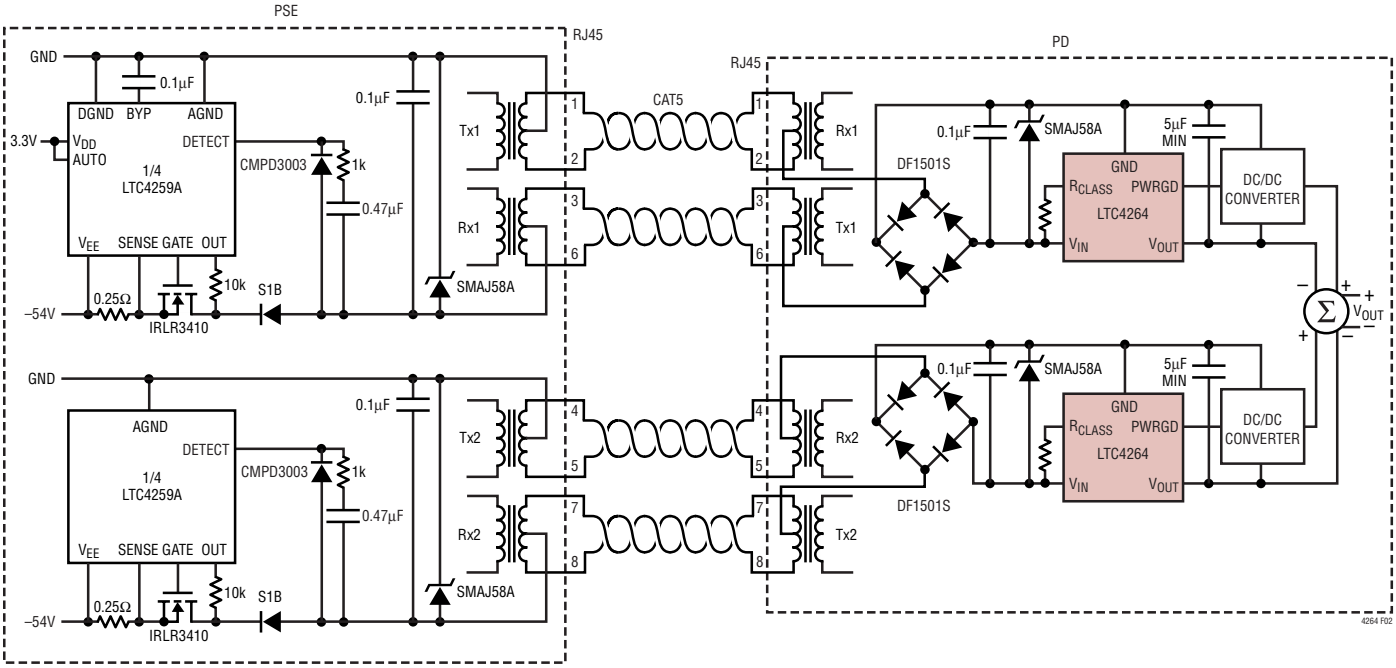


Figure 2. 4-Pair High Power PoE Gigabit Ethernet System Diagram

The LTC4264 is specifically designed to implement the front end of a high power PD for power-hungry PoE applications that must operate beyond the power limits of IEEE 802.3af. LTC4264 uses a precision, dual current limit that keeps inrush below IEEE 803.2af levels to ensure interoperability with any PSE. After inrush is complete, the LTC4264 input current limit switches to the I_{LIMIT_HIGH} level, using an onboard, 750mA power MOSFET. This allows a PD (supplied by a custom PSE) to deliver power above the IEEE 802.3af 12.95W maximum, sending up to 35W to the PD load. The LTC4264 uses established IEEE 802.3af detection and classification methods to maintain compliance and includes an extended programmable Class 5 range for use in custom PoE applications. The LTC4264 features both active-high and active-low power good signaling for simplified interface to any DC/DC converter. The SHDN pin on the LTC4264 can be used to provide a seamless interface for external wall adapter or other auxiliary power options. The I_{LIM_EN} pin provides the option to remove the high current limit, I_{LIMIT_HIGH}. The LTC4264 includes an onboard signature resistor, precision UVLO, thermal overload protection and is available in a thermally-enhanced 12-lead 4mm × 3mm DFN package for superior high current performance.

OPERATION

The LTC4264 high power PD interface controller has several modes of operation depending on the applied input voltage as shown in Figure 3 and summarized in Table 1. These various modes satisfy the requirements defined in the IEEE 802.3af specification. The input voltage is applied to the V_{IN} pin with reference to the GND pin and is always negative.

Table 1. LTC4264 Operational Mode as a Function of Input Voltage

INPUT VOLTAGE	LTC4264 MODE OF OPERATION
0V to –1.4V	Inactive
–1.5V to –10.1V	25k Signature Resistor Detection
–10.3V to –12.4V	Classification Load Current Ramps Up from 0% to 100%
–12.5V to UVLO*	Classification Load Current Active
UVLO* to –57V	Power Applied to PD Load

*UVLO includes hysteresis.
Rising input threshold ≅ –38.9V
Falling input threshold ≅ –30.6V

APPLICATIONS INFORMATION

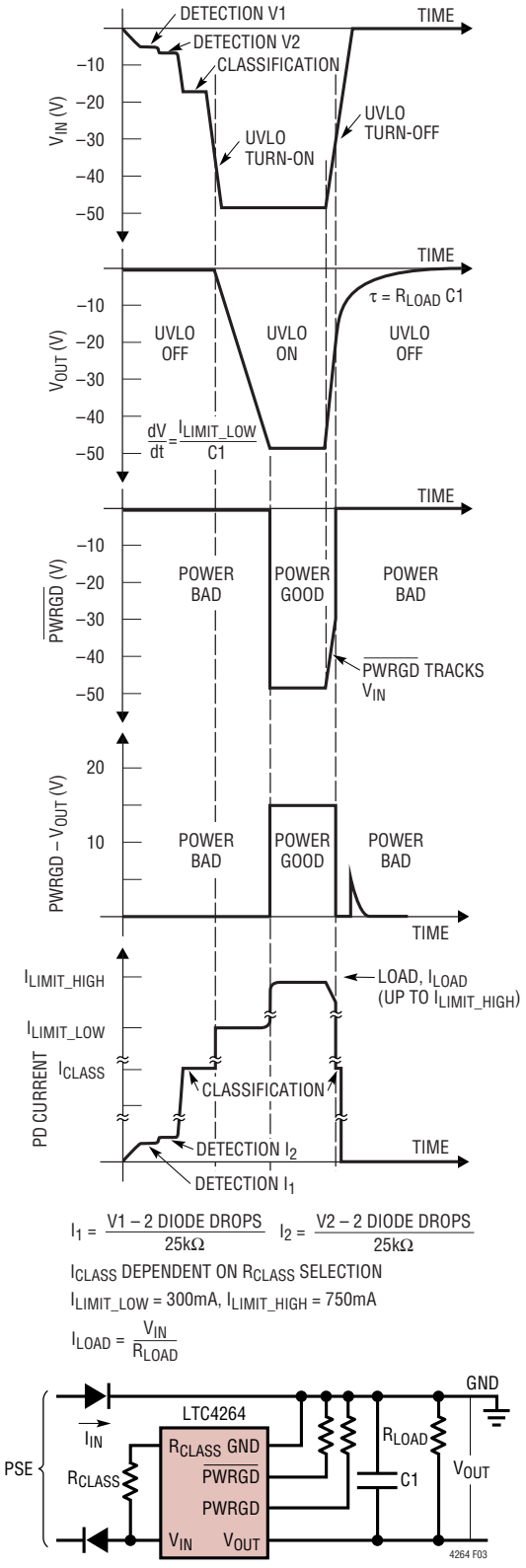


Figure 3. Output Voltage, $\overline{\text{PWRGD}}$, PWRGD and PD Current as a Function of Input Voltage

SERIES DIODES

The IEEE 802.3af-defined operating modes for a PD reference the input voltage at the RJ45 connector on the PD. The PD must be able to handle power received in either polarity. For this reason, it is common to install diode bridges BR1 and BR2 between the RJ45 connector and the LTC4264 (Figure 4). The diode bridges introduce an offset that affects the threshold points for each range of operation. The LTC4264 meets the IEEE 802.3af-defined operating modes by compensating for the diode drops in the threshold points. For the signature, classification, and the UVLO thresholds, the LTC4264 extends two diode drops below the IEEE 802.3af specifications. Note that the voltage ranges specified in the LTC4264 Electrical Specifications are referenced with respect to the IC pins. The LTC4264 threshold points support the use of either traditional or Schottky diode bridges.

DETECTION

During detection, the PSE will apply a voltage in the range of –2.8V to –10V on the cable and look for a 25k signature resistor. This identifies the device at the end of the cable as a PD. With the PSE voltage in the detection range, the LTC4264 presents an internal 25k resistor between the GND and V_{IN} pins. This precision, temperature-compensated resistor provides the proper characteristics to alert the PSE that a PD is present and requests power to be applied.

The IEEE 802.3af specification requires the PSE to use a $\Delta V/\Delta I$ measurement technique to keep the DC offset voltage of the diode bridge from affecting the signature resistance measurement. However, the diode resistance appears in series with the signature resistor and must be included in the overall signature resistance of the PD. The LTC4264 compensates for the two series diodes in the signature path by offsetting the internal resistance so that a PD built with the LTC4264 meets the IEEE 802.3af specification.

In some designs that include an auxiliary power option, such as an external wall adapter, it is necessary to control whether or not the PD is detected by a PSE. With the LTC4264, the 25k signature resistor can be enabled or disabled with the SHDN pin (Figure 5). Taking the SHDN

APPLICATIONS INFORMATION

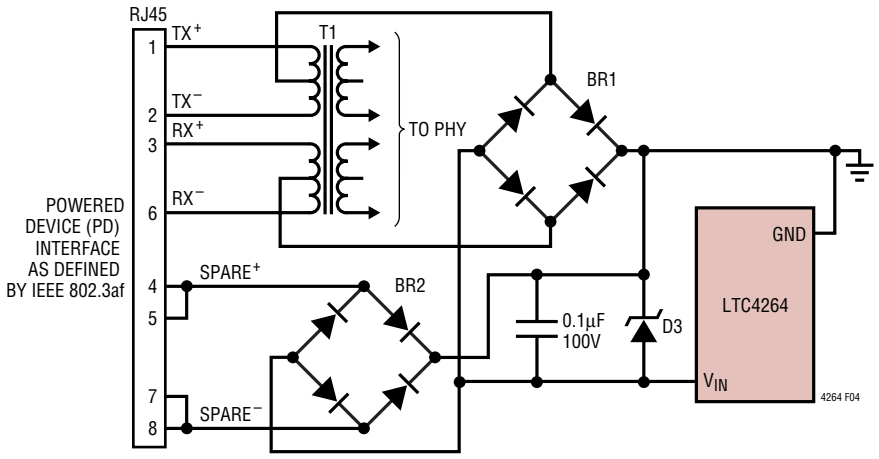


Figure 4. PD Front End Using Diode Bridges on Main and Spare Inputs

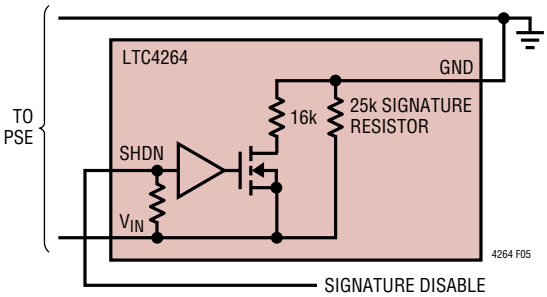


Figure 5. 25k Signature Resistor with Disable

pin high will reduce the signature resistor to 10k which is an invalid signature per the IEEE 802.3af specifications. This will prevent a PSE from detecting and powering the PD. This invalid signature is present in the PSE probing range of –2.8V to –10V. When the input rises above –10V, the signature resistor reverts to 25k to minimize power dissipation in the LTC4264. To disable the signature, tie SHDN to GND. Alternately, the SHDN pin can be driven high with respect to V_{IN}. When SHDN is high, all functions are disabled. For normal operation tie SHDN to V_{IN}.

CLASSIFICATION

Once the PSE has detected a PD, the PSE may optionally classify the PD. Classification provides a method for more efficient allocation of power by allowing the PSE to identify lower-power PDs and assign the appropriate power level to these devices. For each class, there is an associated load current that the PD asserts onto the line during classification probing. The PSE measures the PD load current in order to assign the proper PD classification. Class 0 is included in the IEEE 802.3af specification to cover PDs that do not support classification. Class 1-3 partition PDs into three distinct power ranges as shown in Table 2. Class 4 is reserved by the IEEE 802.3af committee for future use. The new Class 5 defined here is available for system vendors to implement a unique classification for use in closed systems and is not defined or supported by the IEEE 802.3af. With the extended classification range available in the LTC4264, it is possible for system designers to define multiple classes using load currents between 40mA and 75mA.

APPLICATIONS INFORMATION

During classification, the PSE presents a fixed voltage between –15.5V and –20.5V to the PD (Figure 6). With the input voltage in this range, the LTC4264 asserts a load current from the GND pin through the R_{CLASS} resistor. The magnitude of the load current is set with the selection of the R_{CLASS} resistor. The resistor value associated with each class is shown in Table 2.

Table 2. Summary of IEEE 802.3af Power Classifications and LTC4264 R_{CLASS} Resistor Selection

CLASS	USAGE	MAXIMUM POWER LEVELS AT INPUT OF PD (W)	NOMINAL CLASSIFICATION LOAD CURRENT (mA)	LTC4264 RCLASS RESISTOR (Ω, 1%)
0	Default	0.44 to 12.95	<5	Open
1	Optional	0.44 to 3.84	10.5	124
2	Optional	3.84 to 6.49	18.5	69.8
3	Optional	6.49 to 12.95	28	45.3
4	Reserved by IEEE. See Apps		40	30.9
5	Undefined IEEE. See Apps		56	22.1

A substantial amount of power is dissipated in the LTC4264 during classification. The IEEE 802.3af specification limits the classification time to 75ms in order avoid excessive heating. The LTC4264 is designed to handle the power dissipation during the probe period. If the PSE probing exceeds 75ms, the LTC4264 may overheat. In this situation, the thermal protection circuit will engage and disable the classification current source, protecting the LTC4264 from damage. When the die cools, classification is automatically resumed.

Classification presents a challenging stability problem for the PSE due to the wide range of loads possible. The LTC4264 has been designed to avoid PSE interoperability problems by maintaining a positive I-V slope throughout the signature and classification ranges up to UVLO turn-on as shown in Figure 6b. The positive I-V slope avoids areas of negative resistance and helps prevent the PSE from power cycling or getting "stuck" during signature or classification probing. In the event a PSE overshoots beyond the classification voltage range, the available load current aids in returning the PD back into the classification voltage range. (The PD input may otherwise be "trapped" by a reverse-biased diode bridge and the voltage held by the 0.1µF capacitor.) By gently ramping the classification current on and maintaining a positive I-V slope until UVLO turn-on, the LTC4264 provides a well behaved load, assuring interoperability with any PSE.

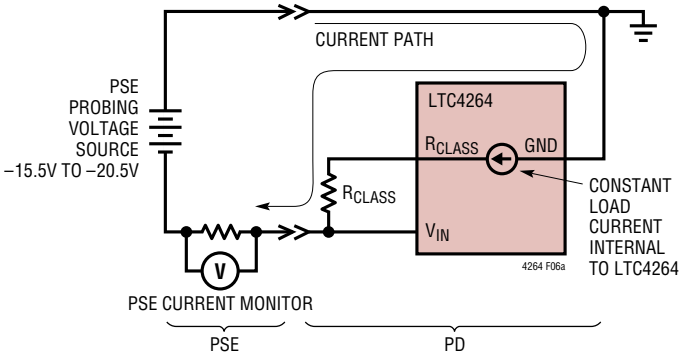


Figure 6a. PSE Probing PD During Classification

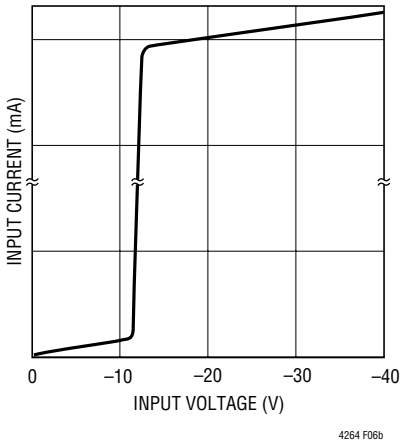


Figure 6b. LTC4264 Positive I-V Slope

APPLICATIONS INFORMATION

UNDERVOLTAGE LOCKOUT

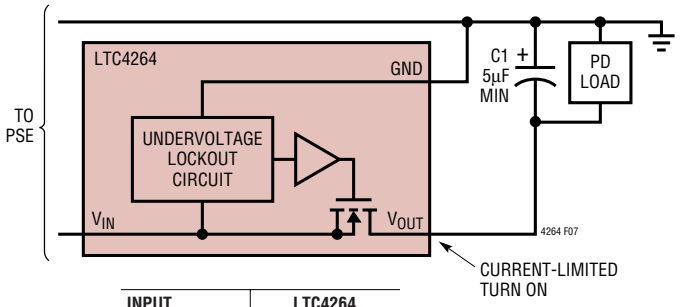
The IEEE 802.3af specification dictates a maximum turn-on voltage of 42V and a minimum turn-off voltage of 30V for the PD. In addition, the PD must maintain large on-off hysteresis to prevent current-resistance (I-R) drops in the wiring between the PSE and the PD from causing start-up oscillation. The LTC4264 incorporates an undervoltage lockout (UVLO) circuit that monitors line voltage at V_{IN} to determine when to apply power to the PD load (Figure 7). Before power is applied to the load, the V_{OUT} pin is high impedance and there is no charge on capacitor C1. When the input voltage rises above the UVLO turn-on threshold, the LTC4264 removes the classification load current and turns on the internal power MOSFET. C1 charges up under LTC4264 inrush current limit control and the V_{OUT} pin transitions from 0V to V_{IN} as shown in Figure 3. The LTC4264 includes a hysteretic UVLO circuit on V_{IN} that keeps power applied to the load until the magnitude of the input voltage falls below the UVLO turn-off threshold. Once V_{IN} falls below UVLO turn-off, the internal power MOSFET disconnects V_{OUT} from V_{IN} and the classification current is re-enabled. C1 will discharge through the PD circuitry and the V_{OUT} pin will go to a high impedance state.

INPUT CURRENT LIMIT

IEEE 802.3af specifies a maximum inrush current and also specifies a minimum load capacitor between the GND and V_{OUT} pins. To control turn-on surge currents in the system the LTC4264 integrates a dual current limit circuit using an onboard power MOSFET and sense resistor to provide a complete inrush control circuit without additional external components.

At turn-on, the LTC4264 will limit the inrush current to I_{LIMIT_LOW}, allowing the load capacitor to ramp up to the line voltage in a controlled manner without interference from the PSE current limit. By keeping the PD current limit below the PSE current limit, PD power up characteristics are well controlled and independent of PSE behavior. This ensures interoperability regardless of PSE output characteristics.

After load capacitor C1 is charged up, the LTC4264 switches to the high input current limit, I_{LIMIT_HIGH}. This allows the LTC4264 to deliver up to 35W to the PD load for high power applications. To maintain compatibility with IEEE 802.3af power levels, it is necessary for the PD designer to ensure the PD steady-state power consumption remains below the limits shown in Table 2. The LTC4264 maintains the high input current limit until the port voltage drops below the UVLO turn-off threshold.



INPUT VOLTAGE	LTC4264 POWER MOSFET
0V TO UVLO*	OFF
>UVLO*	ON

*UVLO INCLUDES HYSTERESIS
RISING INPUT THRESHOLD ≅ –38.9V
FALLING INPUT THRESHOLD ≅ –30.6V

Figure 7. LTC4264 Undervoltage Lockout

APPLICATIONS INFORMATION

During the inrush event as C1 is being charged, a large amount of power is dissipated in the MOSFET. The LTC4264 is designed to accept this load and is thermally protected to avoid damage to the onboard power MOSFET. If a thermal overload does occur, the power MOSFET turns off, allowing the die to cool. Once the die has returned to a safe temperature, the LTC4264 automatically switches to I_{LIMIT_LOW}, and load capacitor C1 charging resumes.

The LTC4264 has the option of disabling the normal operating input current limit, I_{LIMIT_HIGH}, for custom high power PoE applications. To disable the current limit, connect I_{LIM_EN} to V_{IN}. To protect the LTC4264 from damage when the normal current limit is disabled, a safeguard current limit, I_{LIMIT_DISA} keeps the current below destructive levels, typically 1.4A. Note that continuous operation at or near the safeguard current limit will rapidly overheat the LTC4264, engaging the thermal protection circuit. For normal operations, float the I_{LIM_EN} pin. The LTC4264 maintains the I_{LIMIT_LOW} inrush current limit for charging the load capacitor regardless of the state of I_{LIM_EN}. The operation of the I_{LIM_EN} pin is summarized in Table 3.

Table 3. Current Limit as a Function of I_{LIM_EN}

STATE OF I_{LIM_EN}	INRUSH CURRENT LIMT	OPERATING INPUT CURRENT LIMIT
Floating	I_{LIMIT_LOW}	I_{LIMT_HIGH}
Tied to V_{IN}	I_{LIMIT_LOW}	I_{LIMIT_DISA}

POWER GOOD

The LTC4264 includes complementary power good outputs (Figure 8) to simplify connection to any DC/DC converter. Power Good is asserted at the end of the inrush event when load capacitor C1 is fully charged and the DC/DC converter can safely begin operation. The power good signal stays active during normal operation and is de-asserted at power off when the port drops below the UVLO threshold or in the case of a thermal overload event.

For PD designs that use a large load capacitor and also consume a lot of power, it is important to delay activation of the DC/DC converter with the power good signal. If the converter is not disabled during the current-limited turn-on sequence, the DC/DC converter will rob current intended for charging up the load capacitor and create a slow rising input, possibly causing the LTC4264 to go into thermal shutdown.

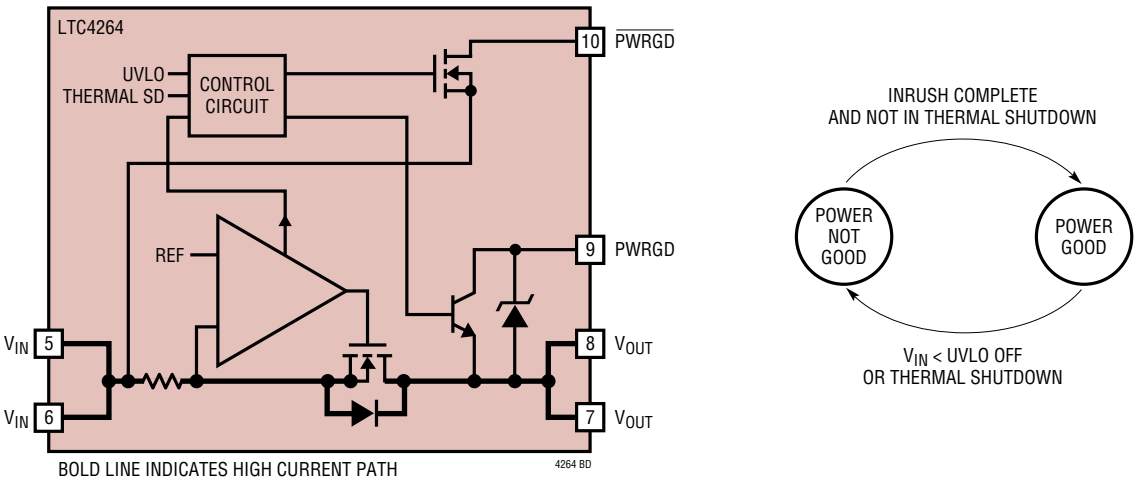


Figure 8. LTC4264 Power Good Functional and State Diagram

APPLICATIONS INFORMATION

The active high PWRGD pin features an internal, open-collector output referenced to V_{OUT}. During inrush, the active high PWRGD pin pulls low until the load capacitor is fully charged. At that point, PWRGD becomes high impedance, indicating the converter may begin running. The active high PWRGD pin can interface directly with the "Run" pin of converter products. The PWRGD pin features an internal 14V clamp to V_{OUT} which protects the DC/DC converter from excessive voltage. During a power supply ramp down event, PWRGD becomes low impedance when V_{IN} drops below the UVLO turn-off threshold, then goes high impedance when the V_{IN} voltages fall to within the detection voltage range.

The active low $\overline{\text{PWRGD}}$ pin connects to an internal, open drain MOSFET referenced to V_{IN} which can sink 1mA. During inrush, $\overline{\text{PWRGD}}$ is high impedance. Once the load capacitor is fully charged, $\overline{\text{PWRGD}}$ is pulled low and DC/DC converter operation can begin. The active low PWRGD pin can connect directly to the shutdown pin of converter products. $\overline{\text{PWRGD}}$ is referenced to the V_{IN} pin and when active will be near the V_{IN} potential. The converter will typically be referenced to V_{OUT} and care must be taken to ensure that the difference in potential of the $\overline{\text{PWRGD}}$ pin does not cause a problem for the DC/DC converter. The use of diode clamp D9 and R_S, as shown in Figure 11, alleviates any problems.

THERMAL PROTECTION

The LTC4264 includes thermal overload protection in order to provide full device functionality in a miniature package while maintaining safe operating temperatures. At turn-on, before load capacitor C1 has charged up, the instantaneous power dissipated by the LTC4264 can be as high as 20W. As the load capacitor charges, the power dissipation in the LTC4264 will decrease until it reaches a steady-state value dependent on the DC load current. The LTC4264 can also experience device heating after turn-on if the PD experiences a fast input voltage rise. For example, if the PD input voltage steps from –37V to –57V, the instantaneous power dissipated by the LTC4264 can be as high as 16W.

The LTC4264 protects itself from damage by monitoring die temperature. If the die exceeds the overtemperature trip point, the power MOSFET and classification transistors are disabled until the part cools down. Once the die cools below the overtemperature trip point, all functions are enabled automatically.

During classification, excessive heating of the LTC4264 can occur if the PSE violates the 75ms probing time limit. In addition, the IEEE 802.3af specification requires a PD to withstand application of any voltage from 0V to 57V indefinitely. To protect the LTC4264 in these situations, the thermal protection circuitry disables the classification circuit if the die temperature exceeds the overtemperature trip point. When the die cools down, classification current is enabled.

Once the LTC4264 has charged up the load capacitor and the PD is powered and running, there will be some residual heating due to the DC load current of the PD flowing through the internal MOSFET. In some high current applications, the LTC4264 power dissipation may be significant. The LTC4264 uses a thermally enhanced DFN12 package that includes an Exposed Pad which should be soldered to an electrically isolated heat sink on the printed circuit board.

MAXIMUM AMBIENT TEMPERATURE

The LTC4264 I_{LIM_EN} pin allows the PD designer to disable the normal operating current limit. With the normal current limit disabled, it is possible to pass currents as high as 1.4A through the LTC4264. In this mode, significant package heating may occur. Depending on the current, voltage, ambient temperature, and waveform characteristics, the LTC4264 may shut down. To avoid nuisance trips of the thermal shutdown, it may be necessary to limit the maximum ambient temperature. Limiting the die temperature to 125°C will keep the LTC4264 from hitting

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thermal shutdown. For DC loads the maximum ambient temperature can be calculated as:

$$T_{MAX} = 125 – \theta_{JA} \bullet PWR\ (°C)$$

where T_{MAX} is the maximum ambient operating temperature, θ_{JA} is the junction-to-ambient thermal resistance (43°C/W), and PWR is the power dissipation for the LTC4264 in Watts ($I_{PD}^2R_{ON}$).

EXTERNAL INTERFACE AND COMPONENT SELECTION

Transformer

Nodes on an Ethernet network commonly interface to the outside world via an isolation transformer (Figure 9). For powered devices, the isolation transformer must include a center tap on the media (cable) side. Proper termination is required around the transformer to provide correct impedance matching and to avoid radiated and conducted emissions. For high power applications beyond IEEE 802.3af limits, the increased current levels increase the current imbalance in the magnetics. This imbalance reduces the perceived inductance and can interfere with data transmission. Transformers specifically designed for high current applications are required. Transformer vendors such as Bel Fuse, Coilcraft, Halo, Pulse, and Tyco (Table 4) can provide assistance with selection of an appropriate isolation transformer and proper termination methods. These vendors have transformers specifically designed for use in high power PD applications.

Table 4. Power over Ethernet Transformer Vendors

VENDOR	CONTACT INFORMATION
Bel Fuse Inc.	206 Van Vorst Street Jersey City, NJ 07302 Tel: 201-432-0463 www.belfuse.com
Coilcraft Inc.	1102 Silver Lake Road Gary, IL 60013 Tel: 847-639-6400 www.coilcraft.com
Halo Electronics	1861 Landings Drive Mountain View, CA 94043 Tel: 650-903-3800 www.haloelectronics.com
Pulse Engineering	12220 World Trade Drive San Diego, CA 92128 Tel: 858-674-8100 www.pulseeng.com
Tyco Electronics	308 Constitution Drive Menlo Park, CA 94025-1164 Tel: 800-227-7040 www.circuitprotection.com

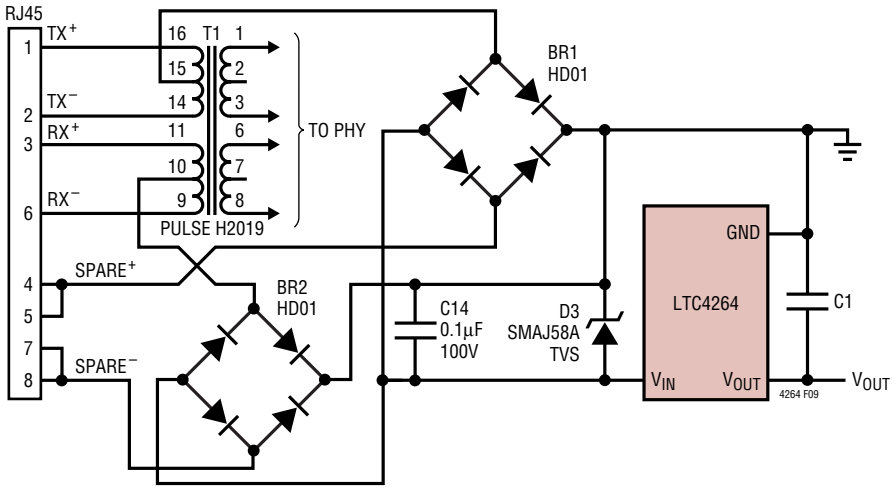

Figure 9. PD Front-End with Isolation Transformer, Diode Bridges, Capacitors and TVS

APPLICATIONS INFORMATION

Diode Bridge

IEEE 802.3af allows power wiring in either of two configurations on the TX/RX wires, and power can be applied to the PD via the spare wire pair in the RJ45 connector. The PD is required to accept power in either polarity on both the data and spare inputs; therefore it is common to install diode bridges on both inputs in order to accommodate the different wiring configurations. Figure 9 demonstrates an implementation of the diode bridges. The IEEE 802.3af specification also mandates that the leakage back through the unused bridge be less than 28µA when the PD is powered with 57V.

The PD may be configured to handle 2-pair or 4-pair power delivery over the Ethernet cable. In a 2-pair power delivery system, one of the two pairs is delivering power to the PD—either the main pair or the spare pair, but not both. In a 4-pair system, both the main and spare pairs deliver power to the PD simultaneously (see Figures 1 and 2). In either case, a diode bridge is needed on the front end to accept power in either polarity. Contact LTC applications for more information about implementing a 4-pair PoE system.

The IEEE standard includes an AC impedance requirement in order to implement the AC disconnect function. Capacitor C14 in Figure 9 is used to meet this AC impedance requirement. A 0.1µF capacitor is recommended for this application.

The LTC4264 has several different modes of operation based on the voltage present between the V_{IN} and GND pins. The forward voltage drop of the input diodes in a PD design subtracts from the input voltage and will affect the transition point between modes. When using the LTC4264, it is necessary to pay close attention to this forward voltage drop. Selection of oversized diodes will help keep the PD thresholds from exceeding IEEE 802.3af specifications.

The input diode bridge of a PD can consume over 4% of the available power in some applications. Schottky diodes can be used in order to reduce power loss. The LTC4264 is designed to work with both standard and Schottky diode bridges while maintaining proper threshold points for IEEE 802.3af compliance.

Figure 4 shows how two diode bridges are typically connected in a PD application. One bridge is dedicated to the data pair while the second bridge is dedicated to the spare pair. For high power applications, a diode bridge typically used in an IEEE 802.3af system cannot handle the higher currents because the operating current is derated at the upper temperature range. To solve this problem, the PD application can utilize larger diode bridges, use discrete diodes or consider the following alternative option.

Realizing that the two diode bridges do not need to be exclusive to the data and spare pairs, the bridges may be reconnected so that current is shared between them. The new configuration extends the maximum operating current while maintaining the smaller package profiles. Figure 9 shows an example of how the two diode bridges may be reconnected. Consult the diode bridge vendors for operating current derating curves when only one of four diodes is in operation.

Auxiliary Power Source

In some applications, it may be necessary to power the PD from an auxiliary power source such as a wall adapter. The auxiliary power can be injected into the PD at several locations and various trade-offs exist. Figure 10 demonstrates four methods of connecting external power to a PD.

Option 1 in Figure 10 inserts power before the LTC4264 interface controller. In this configuration, it is necessary for the wall adapter to exceed the LTC4264 UVLO turn-on requirement. This option provides input current limit for the adapter, provides a valid power good signal and simplifies power priority issues. As long as the adapter applies power to the PD before the PSE, it will take priority and the PSE will not power up the PD because the external power source will corrupt the 25k signature. If the PSE is already powering the PD, the adapter power will be in parallel with the PSE. In this case, priority will be given to the higher supply voltage. If the adapter voltage is higher, the PSE should remove the port voltage since no current

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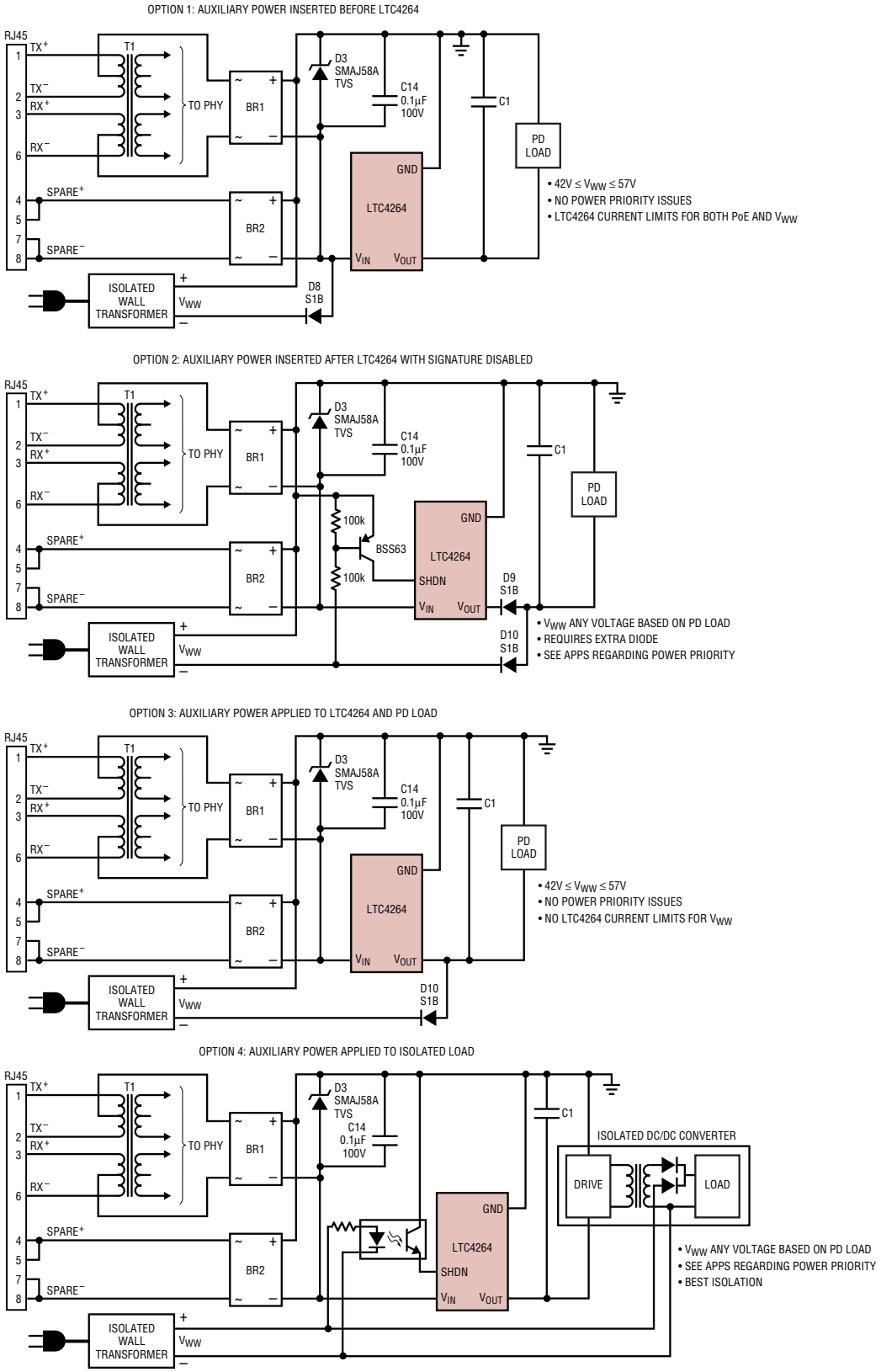

Figure 10. Interfacing Auxiliary Power Source to the PD

APPLICATIONS INFORMATION

will be drawn from the PSE. On the other hand, if the adapter voltage is lower, the PSE will continue to supply power to the PD and the adapter will not be used. Proper operation will occur in either scenario.

Option 2 applies power directly to the DC/DC converter. In this configuration the adapter voltage does not need to exceed the LTC4264 turn-on UVLO requirement and can be selected based solely on the PD load requirements. It is necessary to include diode D9 to prevent the adapter from applying power to the LTC4264. Power priority issues require more intervention. If the adapter voltage is below the PSE voltage, then the priority will be given to the PSE power. The PD will draw power from the PSE while the adapter will remain unused. This configuration is acceptable in a typical PoE system. However, if the adapter voltage is higher than the PSE voltage, the PD will draw power from the adapter. In this situation, it is necessary to address the issue of power cycling that may occur if a PSE is present. The PSE will detect the PD and apply power. If the PD is being powered by the adapter, then the PD will not meet the minimum load requirement and the PSE may subsequently remove power. The PSE will again detect the PD and power cycling will start. With an adapter voltage above the PSE voltage, it is necessary to either disable the signature as shown in option 2, or install a minimum load on the output of the LTC4264 to prevent power cycling. A 3k, 1W resistor connected between GND and V_{OUT} will present the required minimum load.

Option 3 applies power directly to the DC/DC converter bypassing the LTC4264 and omitting diode D9. With the diode omitted, the adapter voltage is applied to the LTC4264 in addition to the DC/DC converter. For this reason, it is necessary to ensure that the adapter maintain the voltage between 42V and 57V to keep the LTC4264 in its normal operating range. The third option has the advantage of corrupting the 25k signature resistance when the external voltage exceeds the PSE voltage and thereby solving the power priority issue.

Option 4 bypasses the entire PD interface and injects power at the output of the low voltage power supply. If the adapter output is below the low voltage output there are no power priority issues. However, if the adapter is above the internal supply, then option 4 suffers from the same power priority issues as option 2 and the signature should be disabled or a minimum load should be installed. Shown in option 4 is one method to disable to the signature while maintaining isolation.

If employing options 1 through 3, it is necessary to ensure that the end-user cannot access the terminals of the auxiliary power jack on the PD since this would compromise IEEE 802.3af isolation requirements and may violate local safety codes. Using option 4 along with an isolated power supply addresses the isolation issue and it is no longer necessary to protect the end-user from the power jack.

The above power cycling scenarios have assumed the PSE is using DC disconnect methods. For a PSE using AC disconnect, a PD with less than minimum load will continue to be powered.

Wall adapters have been known to generate voltage spikes outside their expected operating range. Care should be taken to ensure no damage occurs to the LTC4264 or any support circuitry from extraneous spikes at the auxiliary power interface.

Classification Resistor Selection (R_{CLASS})

The IEEE 802.3af specification allows classifying PDs into four distinct classes with class 4 being reserved for future use (Table 2). The LTC4264 supports all IEEE classes and implements an additional Class 5 for use in custom PoE applications. An external resistor connected from R_{CLASS} to V_{IN} (Figure 6) sets the value of the load current. The designer should determine which class the PD is to advertise and then select the appropriate value of

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R_{CLASS} from Table 2. If a unique load current is required, the value of R_{CLASS} can be calculated as:

$$R_{CLASS} = 1.237V/(I_{LOAD} – I_{IN\_CLASS})$$

I_{IN_CLASS} is the LTC4264 IC supply current during classification given in the electrical specifications. The R_{CLASS} resistor must be 1% or better to avoid degrading the overall accuracy of the classification circuit. Resistor power dissipation will be 100mW maximum and is transient so heating is typically not a concern. In order to maintain loop stability, the layout should minimize capacitance at the R_{CLASS} node. The classification circuit can be disabled by floating the R_{CLASS} pin. The R_{CLASS} pin should not be shorted to V_{IN} as this would force the LTC4264 classification circuit to attempt to source very large currents. In this case, the LTC4264 will quickly go into thermal shutdown.

Power Good Interface

The LTC4264 provides complimentary power good signals to simplify the DC/DC converter interface. Using the power good signal to delay converter operation until the load capacitor is fully charged is recommended as this will help ensure trouble free start up. The active high PWRGD pin is controlled by an open collector transistor referenced to V_{OUT} while the active low $\overline{PWRGD}$ pin is controlled by a high voltage, open-drain MOSFET referenced to V_{IN}. The designer has the option of using either of these signals to enable the DC/DC converter and example interface circuits are shown in Figure 11. When using $\overline{PWRGD}$, diode D9 and resistor R_S protects the converter shutdown pin from excessive reverse voltage.

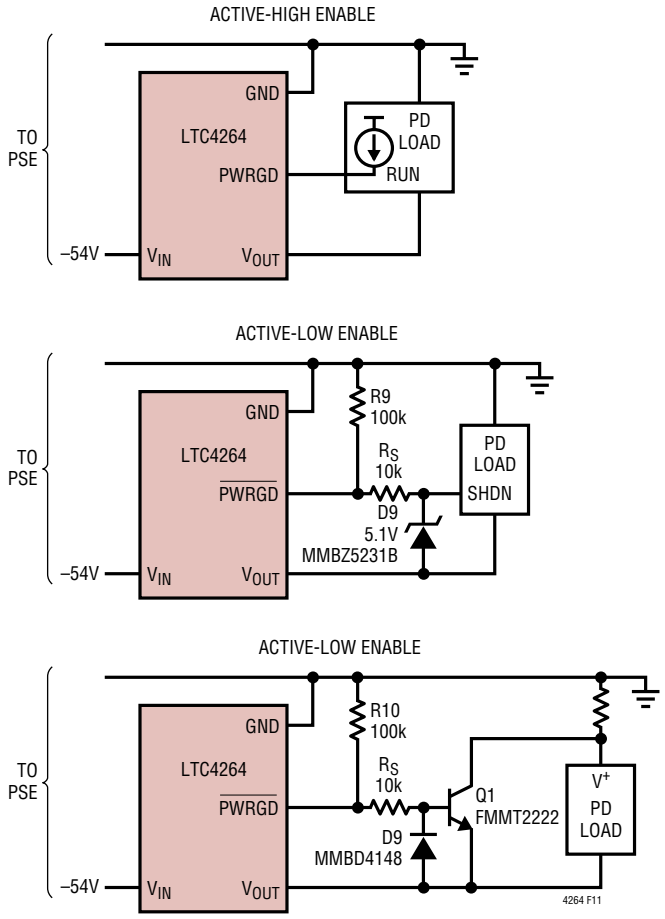

Figure 11. Power Good Interface Examples

APPLICATIONS INFORMATION

Shutdown Interface

To disable the 25k signature resistor, connect SHDN to the GND pin. Alternately, the SHDN pin can be driven high with respect to V_{IN}. Examples of interface circuits that disable the signature and all LTC4264 functions are shown in Figure 10, options 2 and 4. Note that the SHDN input resistance is relatively large and the threshold voltage is fairly low. Because of high voltages present on the printed circuit board, leakage currents from the GND pin could inadvertently pull SHDN high. To ensure trouble-free operation, use high voltage layout techniques in the vicinity of SHDN. If unused, connect SHDN directly to V_{IN}.

Load Capacitor

The IEEE 802.3af specification requires that the PD maintain a minimum load capacitance of 5µF. It is permissible to have a much larger load capacitor and the LTC4264 can charge very large load capacitors before thermal issues become a problem. However, the load capacitor must not be too large or the PD design may violate IEEE 802.3af requirements. The LTC4264 maintains IEEE 802.3af compliance when the load capacitor is 180µF or less. A larger capacitor can be employed in a proprietary, close-system high power application.

If the load capacitor is too large, there can be a problem with inadvertent power shutdown by the PSE. For example, if the PSE is running at –57V (IEEE 802.3af maximum allowed) and the PD is detected and powered up, the load capacitor will be charged to nearly –57V. If for some reason the PSE voltage is suddenly reduced to –44V (IEEE 802.3af minimum allowed), the input bridge will reverse bias and the PD power will be supplied by the load capacitor. Depending on the size of the load capacitor and the DC load of the PD, the PD will not draw any power from the PSE for a period of time. If this period of time exceeds the IEEE 802.3af 300ms disconnect delay, the PSE will remove power from the PD. For this reason, it is necessary to evaluate the load current and capacitance to ensure that inadvertent shutdown cannot occur.

Refer also to Thermal Protection in this data sheet for further discussion on load capacitor selection.

MAINTAIN POWER SIGNATURE

In an IEEE 802.3af system, the PSE uses the maintain power signature (MPS) to determine if a PD continues to require power. The MPS requires the PD to periodically draw at least 10mA and also have an AC impedance less than 26.25kΩ in parallel with 0.05µF. If either the DC current is less than 10mA or the AC impedance is above 26.25kΩ, the PSE may disconnect power. The DC current must be less than 5mA and the AC impedance must be above 2MΩ to guarantee power will be removed. The PD application circuits shown in this data sheet present the required AC impedance necessary to maintain power.

LAYOUT CONSIDERATIONS FOR THE LTC4264

The LTC4264 is relatively immune to layout problems. Excessive parasitic capacitance on the R_{CLASS} pin should be avoided. Include an electrically isolated heat sink to which the exposed pad on the bottom of the package can be soldered. For optimum thermal performance, make the heat sink as large as possible. Voltages in a PD can be as large as –57V for PoE applications, so high voltage layout techniques should be employed. The SHDN pin should be separated from other high voltage pins, like GND and

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V_{OUT}, to avoid the possibility of leakage shutting down the LTC4264. If not used, tie SHDN to V_{IN}.

The load capacitor connected between GND and V_{OUT} of the LTC4264 can store significant energy when fully charged. The design of a PD must ensure that this energy is not inadvertently dissipated in the LTC4264. The polarity-protection diodes prevent an accidental short on the cable from causing damage. However, if the V_{IN} pin is shorted to GND inside the PD while the capacitor is charged, current will flow through the parasitic body diode of the internal MOSFET and may cause permanent damage to the LTC4264.

ELECTRO STATIC DISCHARGE AND SURGE PROTECTION

The LTC4264 is specified to operate with an absolute maximum voltage of –90V and is designed to tolerate brief over-voltage events. However, the pins that interface to the outside world (primarily V_{IN} and GND) can routinely see peak voltages in excess of 10kV. To protect the LTC4264, it is highly recommended that the SMAJ58A unidirectional 58V transient voltage suppressor be installed between the diode bridge and the LTC4264 (D3 in Figure 4).

ISOLATION

The 802.3 standard requires Ethernet ports to be electrically isolated from all other conductors that are user accessible. This includes the metal chassis, other connectors and any auxiliary power connection. For PDs, there are two common methods to meet the isolation requirement. If there will be any user accessible connection to the PD, then an isolated DC/DC converter is necessary to meet the isolation requirements. If user connections can be avoided, then it is possible to meet the safety requirement by completely enclosing the PD in an insulated housing. In all PD applications, there should be no user accessible electrical connections to the LTC4264 or support circuitry other than the RJ-45 port.

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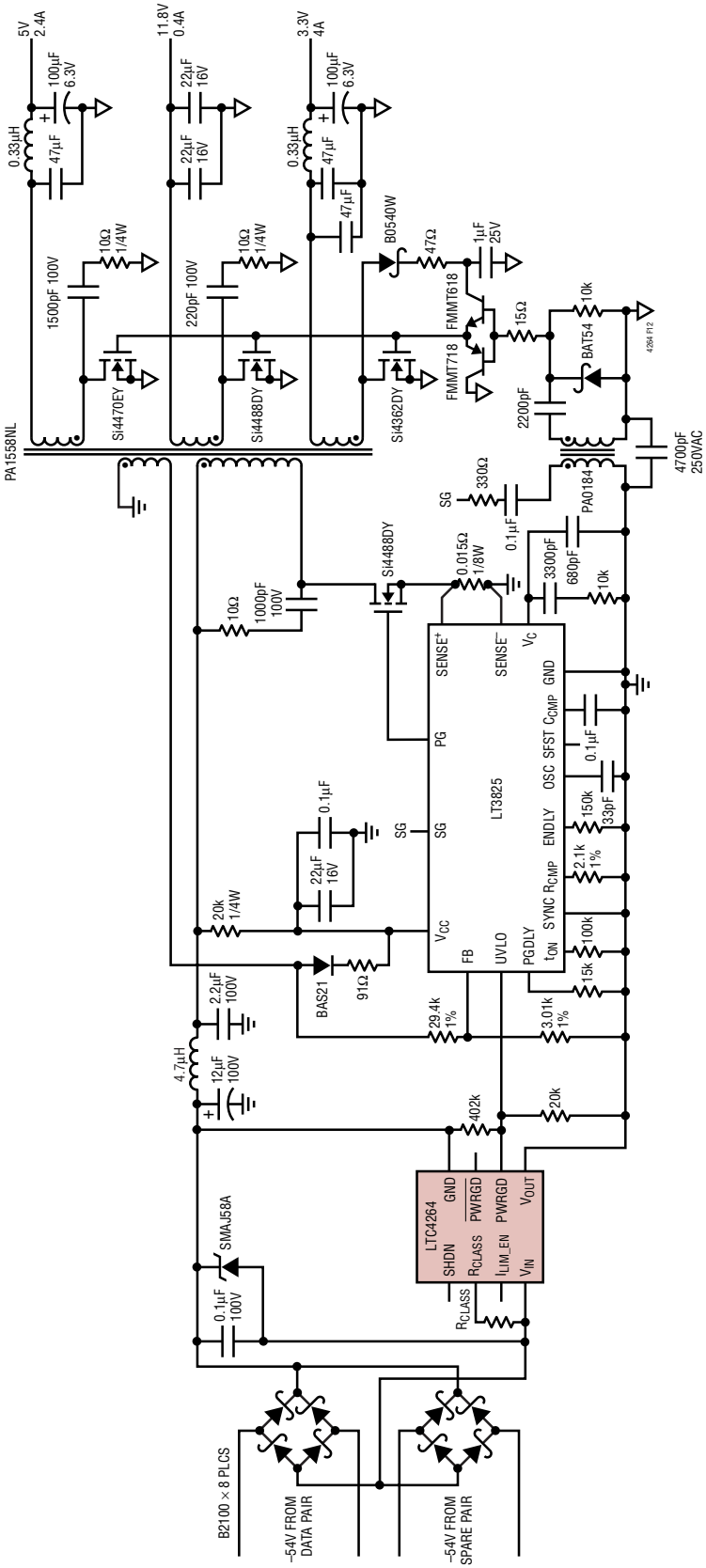
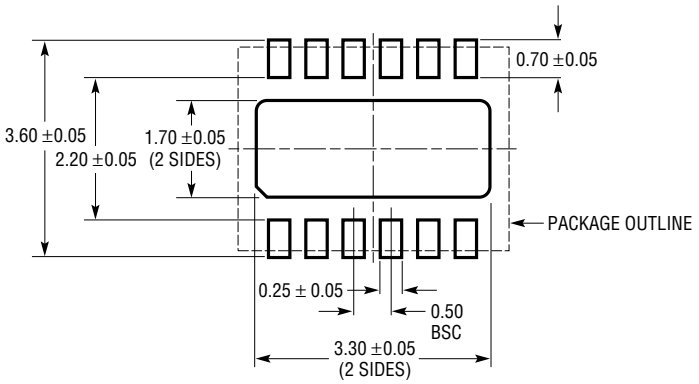


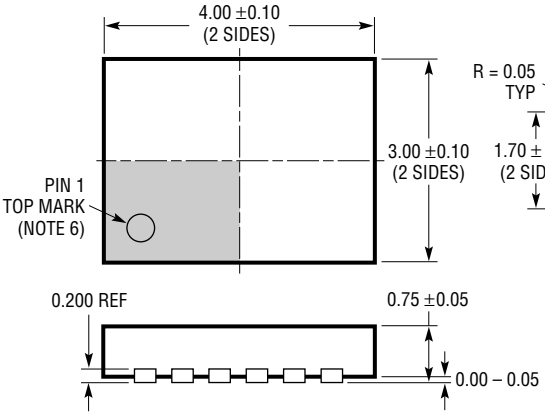
Figure 12. High Efficiency, Triple Output Power Supply

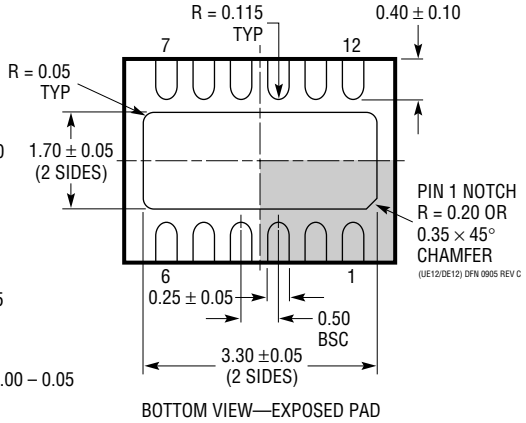
PACKAGE DESCRIPTION

DE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



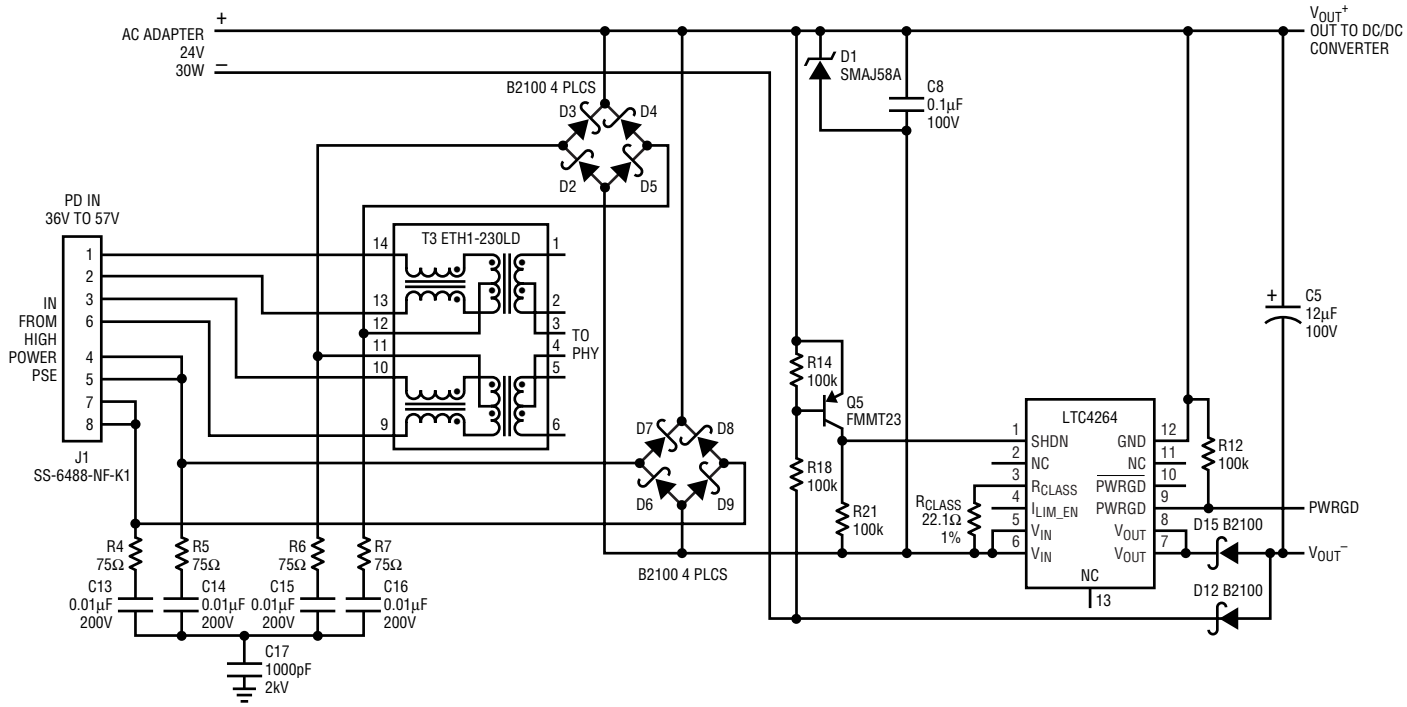


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

LTC4264 with Auxiliary Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1952	Single Switch Synchronous Forward Counter	Synchronous Controller, Programmable Volt-Sec Clamp, Low Start Current
LTC3803	Current Mode Flyback DC/DC Controller in ThinSOT™	200kHz Constant Frequency, Adjustable Slope Compensation, Optimized for High Input Voltage Applications
LTC3805	Adjustable Frequency Current Mode Flyback Controller	Slope Comp Overcurrent Protect, Internal/External Clock
LTC3825	Isolate No-Opto Synchronous Flyback Controller with Wide Input Supply Range	Adjustable Switching Frequency, Programmable Undervoltage Lockout, Accurate Regulation without Trim, Synchronous for High Efficiency
LTC4257-1	IEEE 802.3af PD Interface Controller	100V 400mA Internal Switch, Programmable Classification Dual Current Limit
LTC4258	Quad IEEE 802.3af Power over Ethernet Controller	DC Disconnect Only, IEEE-Compliant PD Detection and Classification, Autonomous Operation or I²C™ Control
LTC4259A-1	Quad IEEE 802.3af Power over Ethernet Controller	AC or DC Disconnect IEEE-Compliant PD Detection and Classification, Autonomous Operation or I²C Control
LTC4263	Single IEEE 802.3af Power over Ethernet Controller	AC or DC Disconnect IEEE-Compliant PD Detection and Classification, Autonomous Operation or I²C Control
LTC4263-1	High Power Single PSE Controller	Internal Switch, Autonomous Operation, 30W
LTC4267	IEEE 802.3af PD Interface with an Integrated Switching Regulator	100V 400mA Internal Switch, Programmable Classification, 200kHz Constant Frequency PWM, Interface and Switcher Optimized for IEEE-Compliant PD System

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