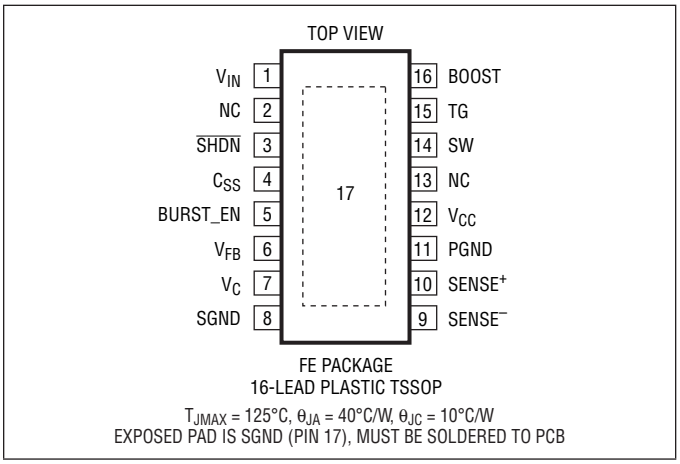
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}) ..... 65V to –0.3V
Boosted Supply Voltage (BOOST) ..... 80V to –0.3V
Switch Voltage (SW)(Note 8) ..... 65V to –1V
Differential Boost Voltage
(BOOST to SW) ..... 24V to –0.3V
Bias Supply Voltage (V_{CC}) ..... 24V to –0.3V
SENSE$^+$ and SENSE$^-$ Voltages ..... 40V to –0.3V

(SENSE$^+$ to SENSE$^-$) ..... 1V to –1V
BURST_EN Voltage ..... 24V to –0.3V
V_C, V_{FB}, C_{SS}, and $\overline{SHDN}$ Voltages ..... 5V to –0.3V
C_{SS} and $\overline{SHDN}$ Pin Currents 1mA
Operating Junction Temperature Range (Notes 2, 3)
LT3724E ..... –40°C to 125°C
LT3724I ..... –40°C to 125°C
LT3724MP ..... –55°C to 125°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



FE PACKAGE
16-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD IS SGND (PIN 17), MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3724EFE#PBF	LT3724EFE#TRPBF	3724EFE	16-Lead Plastic TSSOP	–40°C to 125°C
LT3724IFE#PBF	LT3724IFE#TRPBF	3724IFE	16-Lead Plastic TSSOP	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT3724MPFE	LT3724MPFE#TR	3724MPFE	16-Lead Plastic TSSOP	–55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 20V, V_{CC} = BOOST = BURST_EN = 10V, $\overline{SHDN}$ = 2V, SENSE$^-$ = SENSE$^+$ = 10V, SGND = PGND = SW = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage Range (Note 4)		●	4		60	V
	Minimum Start Voltage		●	7.5			V
	UVLO Threshold (Falling)		●	3.65	3.8	3.95	V
	UVLO Threshold Hysteresis				670		mV
I_{VIN}	V_{IN} Supply Current	V_{CC} > 9V			20		µA
	V_{IN} Burst Mode Current	V_{BURST_EN} = 0V, V_{FB} = 1.35V			20		µA
	V_{IN} Shutdown Current	$V_{\overline{SHDN}}$ = 0V			10	15	µA

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 20V, V_{CC} = BOOST = BURST_EN = 10V, $\overline{SHDN}$ = 2V, $SENSE^-$ = $SENSE^+$ = 10V, SGND = PGND = SW = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{BOOST}	Operating Voltage Range		●			75	V
	Operating Voltage Range (Note 5)	V_{BOOST} - V_{SW}	●			20	V
	UVLO Threshold (Rising)	V_{BOOST} - V_{SW}			5		V
	UVLO Threshold Hysteresis	V_{BOOST} - V_{SW}			400		mV
I_{BOOST}	BOOST Supply Current (Note 6)				1.4		mA
	BOOST Burst Mode Current	V_{BURST_EN} = 0V			0.1		µA
	BOOST Shutdown Current	$V_{\overline{SHDN}}$ = 0V			0.1		µA
V_{CC}	Operating Voltage Range (Note 5)		●			20	V
	Output Voltage	Over Full Line and Load Range	●		8	8.3	V
	UVLO Threshold (Rising)				6.25		V
	UVLO Threshold Hysteresis				500		mV
I_{VCC}	V_{CC} Supply Current (Note 6)		●		1.7	2.1	mA
	V_{CC} Burst Mode Current	V_{BURST_EN} = 0V			80		µA
	V_{CC} Shutdown Current	$V_{\overline{SHDN}}$ = 0V			20		µA
	Short-Circuit Current		●	–30	–55		mA
V_{FB}	Error Amp Reference Voltage	Measured at V_{FB} Pin		1.224	1.231	1.238	V
			●	1.215		1.245	V
I_{FB}	Feedback Input Current				25		nA
$V_{\overline{SHDN}}$	Enable Threshold (Rising)		●	1.3	1.35	1.4	V
	Threshold Hysteresis				120		mV
V_{SENSE}	Common Mode Range		●	0		36	V
	Current Limit Sense Voltage	$V_{SENSE^+} - V_{SENSE^-}$	●	140	150	175	mV
I_{SENSE}	Input Current	$V_{SENSE(CM)}$ = 0V			400		µA
	($I_{SENSE^+} + I_{SENSE^-}$)	$V_{SENSE(CM)}$ = 2.5V			2		µA
		$V_{SENSE(CM)}$ > 4V			–150		µA
f_{SW}	Operating Frequency			190	200	210	kHz
			●	175		220	kHz
		MP Grade	●	165	200	225	kHz
$V_{FB(SS)}$	Soft-Start Disable Voltage	V_{FB} Rising			1.185		V
	Soft-Start Disable Hysteresis				300		mV
I_{SS}	Soft-Start Capacitor Control Current				2		µA
g_m	Error Amp Transconductance		●	275	340	400	µmhos
A_V	Error Amp DC Voltage Gain				62		dB
V_C	Error Amp Output Range	Zero Current to Current Limit			1.2		V
I_{VC}	Error Amp Sink/Source Current				±30		µA
V_{TG}	Gate Drive Output On Voltage (Note 7)	C_{LOAD} = 3300pF			9.8		V
	Gate Drive Output Off Voltage	C_{LOAD} = 3300pF			0.1		V
t_{TG}	Gate Drive Rise/Fall Time	10% to 90% or 90% to 10%, C_{LOAD} = 3300pF			60		ns
$t_{TG(OFF)}$	Minimum Switch Off Time				350		ns
$t_{TG(ON)}$	Minimum Switch On Time		●		300	500	ns
I_{SW}	SW Pin Sink Current	V_{SW} = 2V			300		mA

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ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3724 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: The LT3724E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3724I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3724MP is 100% tested and guaranteed over the –55°C to 125°C operating junction temperature range.

Note 4: V_{IN} voltages below the start-up threshold (7.5V) are only supported when the V_{CC} is externally driven above 6.5V.

Note 5: Operating range is dictated by MOSFET absolute maximum V_{GS}.

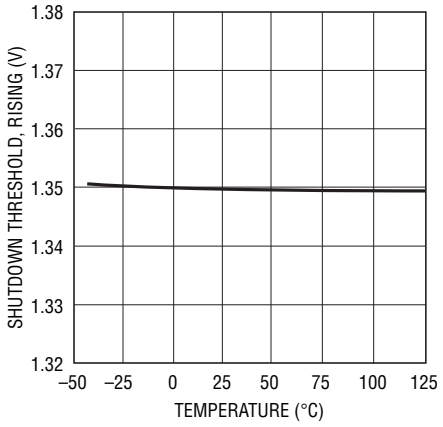
Note 6: Supply current specification does not include switch drive currents. Actual supply currents will be higher.

Note 7: DC measurement of gate drive output "ON" voltage is typically 8.6V. Internal dynamic bootstrap operation yields typical gate "ON" voltages of 9.8V during standard switching operation. Standard operation gate "ON" voltage is not tested but guaranteed by design.

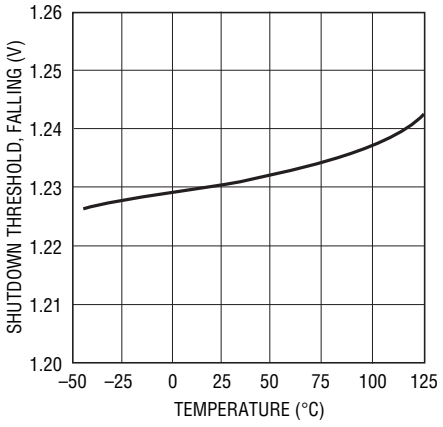
Note 8: The –1V absolute maximum on the SW pin is a transient condition. It is guaranteed by design and not subject to test.

TYPICAL PERFORMANCE CHARACTERISTICS

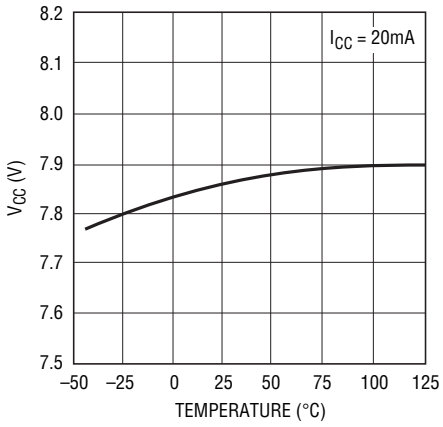
Shutdown Threshold (Rising) vs Temperature



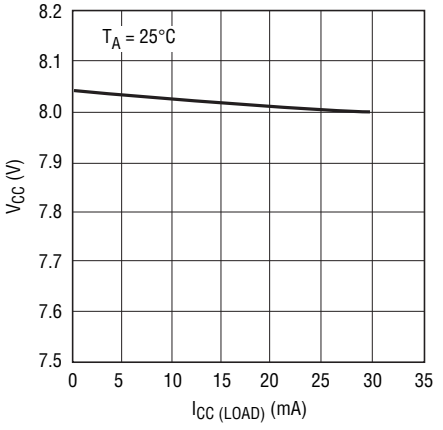
Shutdown Threshold (Falling) vs Temperature



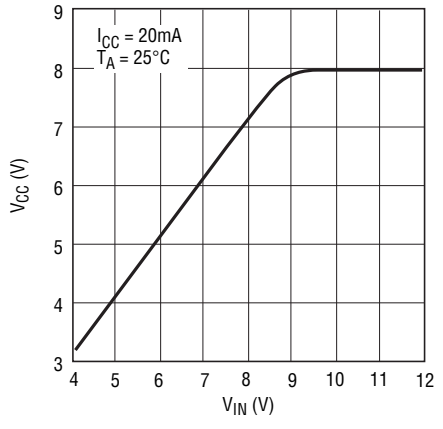
V_{CC} vs Temperature



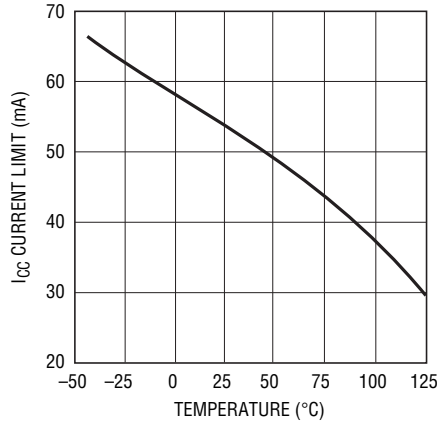
V_{CC} vs $I_{CC(LOAD)}$



V_{CC} vs V_{IN}



I_{CC} Current Limit vs Temperature



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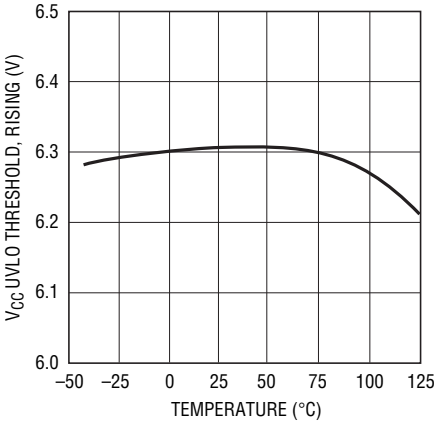
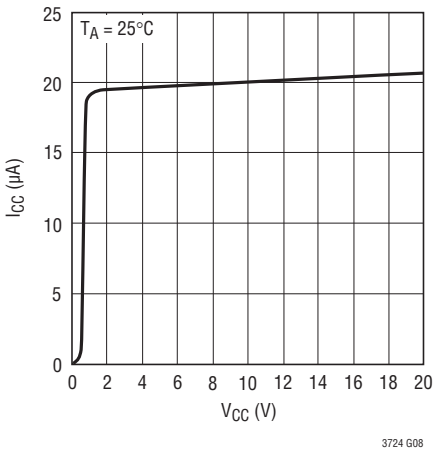
TYPICAL PERFORMANCE CHARACTERISTICS

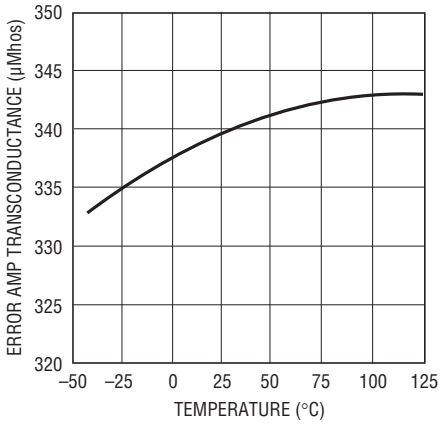
V_{CC} UVLO Threshold (Rising) vs Temperature



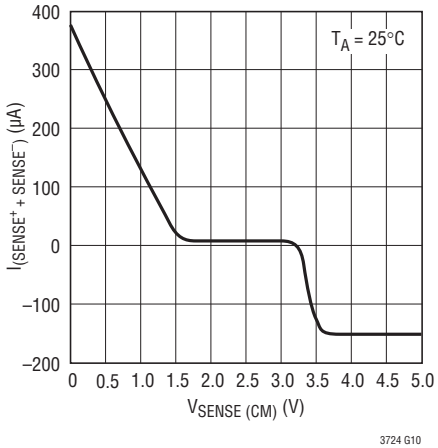
I_{CC} vs V_{CC} ($\overline{SHDN}$ = 0V)



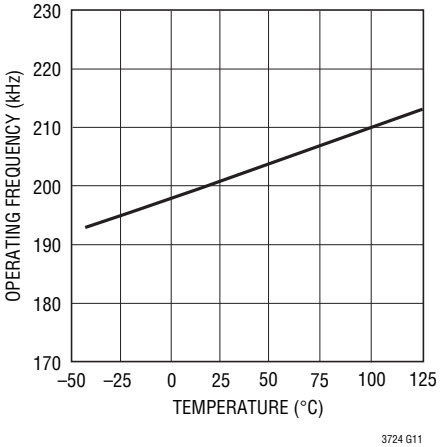
Error Amp Transconductance vs Temperature



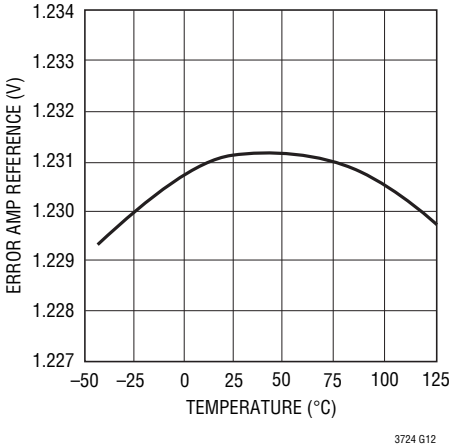
$I_{(SENSE^+ + SENSE^-)}$ vs $V_{SENSE (CM)}$



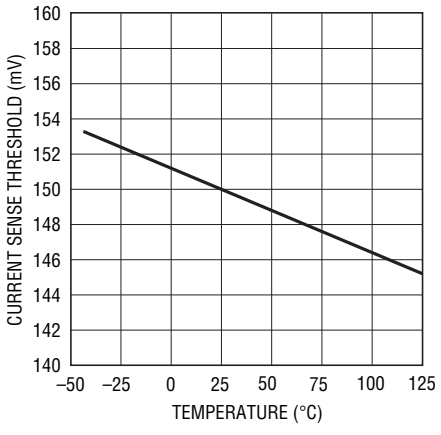
Operating Frequency vs Temperature



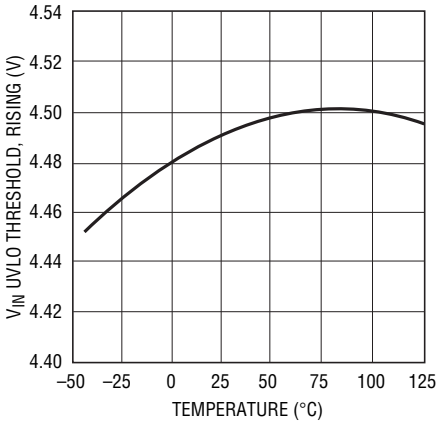
Error Amp Reference vs Temperature



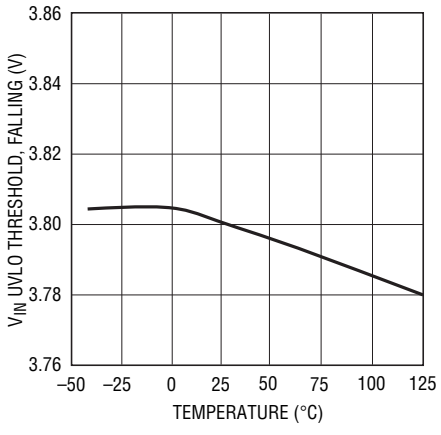
Maximum Current Sense Threshold vs Temperature



V_{IN} UVLO Threshold (Rising) vs Temperature



V_{IN} UVLO Threshold (Falling) vs Temperature



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PIN FUNCTIONS

V_{IN} (Pin 1): The V_{IN} pin is the main supply pin and should be decoupled to SGND with a low ESR capacitor located close to the pin.

NC (Pin 2): No Connection.

$\overline{SHDN}$ (Pin 3): The $\overline{SHDN}$ pin has a precision IC enable threshold of 1.35V (rising) with 120mV of hysteresis. It is used to implement an undervoltage lockout (UVLO) circuit. See Application Information section for implementing a UVLO function. When the $\overline{SHDN}$ pin is pulled below a transistor V_{BE} (0.7V), a low current shutdown mode is entered, all internal circuitry is disabled and the V_{IN} supply current is reduced to approximately 10µA. Typical pin input bias current is <10µA and the pin is internally clamped to 6V.

C_{SS} (Pin 4): The soft-start pin is used to program the supply soft-start function. The pin is connected to V_{OUT} via a ceramic capacitor (C_{SS}) and 200kΩ series resistor. During start-up, the supply output voltage slew rate is controlled to produce a 2µA average current through the soft-start coupling capacitor. Use the following formula to calculate C_{SS} for a given output voltage slew rate:

$$C_{SS} = 2\mu A(t_{SS}/V_{OUT})$$

See the application section for more information on setting the rise time of the output voltage during start-up. Shorting this pin to SGND disables the soft-start function.

BURST_EN (Pin 5): The BURST_EN pin is used to enable or disable Burst Mode operation. Connect the BURST_EN pin to ground to enable the burst mode function. Connect the pin to V_{CC} to disable the burst mode function.

V_{FB} (Pin 6): The output voltage feedback pin, V_{FB}, is externally connected to the supply output voltage via a resistive divider. The V_{FB} pin is internally connected to the inverting input of the error amplifier. In regulation, V_{FB} is 1.231V.

V_C (Pin 7): The V_C pin is the output of the error amplifier whose voltage corresponds to the maximum (peak) switch current per oscillator cycle. The error amplifier is typically configured as an integrator circuit by connecting an RC network from the V_C pin to SGND. This circuit creates the dominant pole for the converter regulation control loop. Specific integrator characteristics can be configured to optimize transient response. Connecting a 100pF or greater high frequency bypass capacitor from this pin to ground is recommended. When Burst Mode operation is enabled (see Pin 5 description), an internal low impedance clamp on the V_C pin is set at 100mV below the burst threshold, which limits the negative excursion of the pin voltage. Therefore, this pin cannot be pulled low with a low impedance source. If the V_C pin must be externally manipulated, do so through a 1kΩ series resistance.

SGND (Pin 8, 17): The SGND pin is the low noise ground reference. It should be connected to the $-V_{OUT}$ side of the output capacitors. Careful layout of the PCB is necessary to keep high currents away from this SGND connection. See the Application Information section for helpful hints on PCB layout of grounds.

$SENSE^-$ (Pin 9): The $SENSE^-$ pin is the negative input for the current sense amplifier and is connected to the V_{OUT} side of the sense resistor for step-down applications. The sensed inductor current limit is set to 150mV across the SENSE inputs.

$SENSE^+$ (Pin 10): The $SENSE^+$ pin is the positive input for the current sense amplifier and is connected to the inductor side of the sense resistor for step-down applications. The sensed inductor current limit is set to 150mV across the SENSE inputs.

PGND (Pin 11): The PGND pin is the high-current ground reference for internal low side switch and the V_{CC} regulator circuit. Connect the pin directly to the negative terminal of the V_{CC} decoupling capacitor. See the Application Information section for helpful hints on PCB layout of grounds.

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PIN FUNCTIONS

V_{CC} (Pin 12): The V_{CC} pin is the internal bias supply decoupling node. Use a low ESR 1µF ceramic capacitor to decouple this node to PGND. Most internal IC functions are powered from this bias supply. An external diode connected from V_{CC} to the BOOST pin charges the bootstrapped capacitor during the off-time of the main power switch. Back driving the V_{CC} pin from an external DC voltage source, such as the V_{OUT} output of the buck regulator supply, increases overall efficiency and reduces power dissipation in the IC. In shutdown mode this pin sinks 20µA until the pin voltage is discharged to 0V.

NC (Pin 13): No Connection.

SW (Pin 14): In step-down applications the SW pin is connected to the cathode of an external clamping Schottky diode, the source of the power MOSFET and the inductor. The SW node voltage swing is from V_{IN} during the on-time of the power MOSFET, to a Schottky voltage drop below ground during the off-time of the power MOSFET. In start-up and in operating modes where there is insufficient inductor current to freewheel the Schottky diode, an internal switch is turned on to pull the SW pin to ground so that the BOOST pin capacitor can be charged. Give careful consideration in choosing the Schottky diode to limit the negative voltage swing on the SW pin.

TG (Pin 15): The TG pin is the bootstrapped gate drive for the top N-Channel MOSFET. Since very fast high currents are driven from this pin, connect it to the gate of the power MOSFET with a short and wide, typically 0.02" width, PCB trace to minimize inductance.

BOOST (Pin 16): The BOOST pin is the supply for the bootstrapped gate drive and is externally connected to a low ESR ceramic boost capacitor referenced to SW pin. The recommended value of the BOOST capacitor, C_{BOOST}, is 50 times greater than the total input capacitance of the topside MOSFET. In most applications 0.1µF is adequate. The maximum voltage that this pin sees is V_{IN} + V_{CC}, ground referred.

Exposed Pad (SGND) (Pin 17): The exposed leadframe is internally connected to the SGND pin. Solder the exposed pad to the PCB ground for electrical contact and optimal thermal performance.

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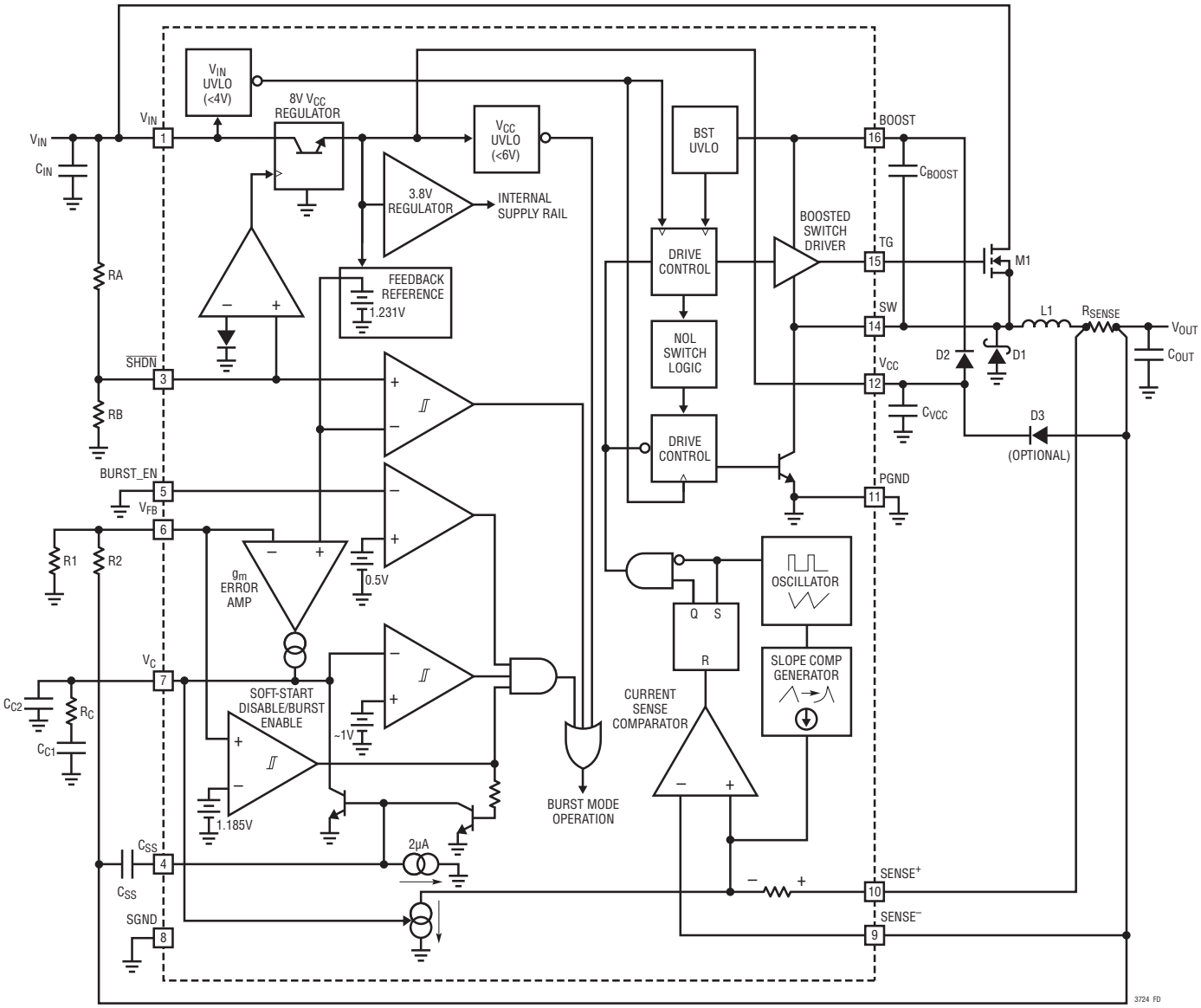
FUNCTIONAL DIAGRAM



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OPERATIONS (Refer to Functional Diagram)

The LT3724 is a PWM controller with a constant frequency, current mode control architecture. It is designed for low to medium power, switching regulator applications. Its high operating voltage capability allows it to step-up or down input voltages up to 60V without the need for a transformer. The LT3724 is used in nonsynchronous applications, meaning that a freewheeling rectifier diode (D1 of Function Diagram) is used instead of a bottom side MOSFET. For circuit operation, please refer to the Functional Diagram of the IC and Typical Application on the front page of the data sheet. The LT3800 is a similar part that uses synchronous rectification, replacing the diode with a MOSFET in a step-down application.

Main Control Loop

During normal operation, the external N-channel MOSFET switch is turned on at the beginning of each cycle. The switch stays on until the current in the inductor exceeds a current threshold set by the DC control voltage, V_C, the output of the voltage control loop. The voltage control loop monitors the output voltage, via the V_{FB} pin voltage, and compares it to an internal 1.231V reference. It increases the current threshold when the V_{FB} voltage is below the reference voltage and decreases the current threshold when the V_{FB} voltage is above the reference voltage. For instance, when an increase in the load current occurs, the output voltage drops causing the V_{FB} voltage to drop relative to the 1.231V reference. The voltage control loop senses the drop and increases the current threshold. The peak inductor current is increased until the average inductor current equals the new load current and the output voltage returns to regulation.

Current Limit/Short-Circuit

The inductor current is measured with a series sense resistor (see the Typical Application on the front page). When the voltage across the sense resistor reaches the maximum current sense threshold, typically 150mV, the TG MOSFET driver is disabled for the remainder of that cycle. If the maximum current sense threshold is still exceeded at the beginning of the next cycle, the entire cycle is skipped. Cycle skipping keeps the inductor currents to a controlled value during a short-circuit, particularly when V_{IN} is high. Setting the sense resistor value is discussed in the "Application Information" section.

V_{CC}/Boosted Supply

An internal V_{CC} regulator provides V_{IN} derived gate-drive power for start-up under all operating conditions with MOSFET gate charge loads up to 90nC. The regulator can operate continuously in applications with V_{IN} voltages up to 60V, provided the V_{IN} voltage and/or MOSFET gate charge currents do not create excessive power dissipation in the IC. Safe operating conditions for continuous regulator use are shown in Figure 1. In applications where these conditions are exceeded, V_{CC} must be derived from an external source after start-up. The LT3724 regulator can, however, be used for "full time" use in applications where short-duration V_{IN} transients exceed allowable continuous voltages.

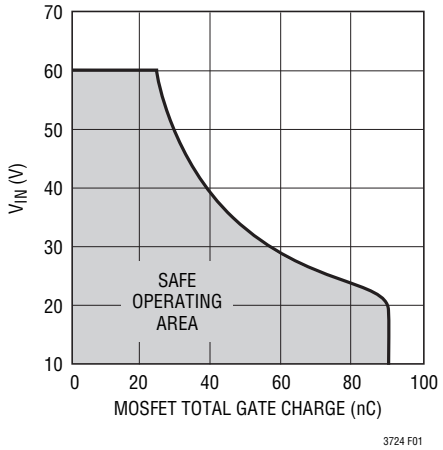

Figure 1. V_{CC} Regulator Continuous Operating Conditions

For higher converter efficiency and less power dissipation in the IC, V_{CC} can also be supplied from an external supply such as the converter output. When an external supply back drives the internal V_{CC} regulator through an external diode and the V_{CC} voltage is pulled to a diode above its regulation voltage, the internal regulator is disabled and goes into a low current mode. V_{CC} is the bias supply for most of the internal IC functions and is also used to charge the bootstrapped capacitor (C_{BOOST}) via an external diode. The external MOSFET switch is biased from the bootstrapped capacitor. While the external MOSFET switch is off, an internal BJT switch, whose collector is connected to the SW pin and emitter is connected to the PGND pin, is turned on to pull the SW node to PGND and recharge the bootstrap capacitor. The switch stays on until

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OPERATIONS (Refer to Functional Diagram)

either the start of the next cycle or until the bootstrapped capacitor is fully charged.

MOSFET Driver

The LT3724 contains a high speed boosted driver to turn on and off an external N-channel MOSFET switch. The MOSFET driver derives its power from the boost capacitor which is referenced to the SW pin and the source of the MOSFET. The driver provides a large pulse of current to turn on the MOSFET fast and minimize transition times. Multiple MOSFETs can be paralleled for higher current operation.

To eliminate the possibility of shoot through between the MOSFET and the internal SW pull-down switch, an adaptive nonoverlap circuit ensures that the internal pull-down switch does not turn on until the gate of the MOSFET is below its turn on threshold.

Low Current Operation (Burst Mode Operation)

To increase low current load efficiency, the LT3724 is capable of operating in Linear Technology's proprietary Burst Mode operation where the external MOSFET operates intermittently based on load current demand. The Burst Mode function is disabled by connecting the BURST_EN pin to V_{CC} and enabled by connecting the pin to SGND.

When the required switch current, sensed via the V_C pin voltage, is below 15% of maximum, Burst Mode operation is employed and that level of sense current is latched onto the IC control path. If the output load requires less than this latched current level, the converter will overdrive the output slightly during each switch cycle. This overdrive condition is sensed internally and forces the voltage on the V_C pin to continue to drop. When the voltage on V_C drops 150mV below the 15% load level, switching is disabled, and the LT3724 shuts down most of its internal circuitry, reducing total quiescent current to 100µA. When the converter output begins to fall, the V_C pin voltage begins to climb. When the voltage on the V_C pin climbs back to the 15% load level, the IC returns to normal operation and switching resumes. An internal clamp on the V_C pin is set at 100mV below the output disable threshold, which limits the negative excursion of the pin voltage, minimizing the converter output ripple during Burst Mode operation.

During Burst Mode operation, the V_{IN} pin current is 20µA and the V_{CC} current is reduced to 80µA. If no external drive is provided for V_{CC}, all V_{CC} bias currents originate from the V_{IN} pin, giving a total V_{IN} current of 100µA. Burst current can be reduced further when V_{CC} is driven using an output derived source, as the V_{CC} component of V_{IN} current is then reduced by the converter duty cycle ratio.

Start-Up

The following section describes the start-up of the supply and operation down to 4V once the step-down supply is up and running. For the protection of the LT3724 and the switching supply, there are internal undervoltage lockout (UVLO) circuits with hysteresis on V_{IN}, V_{CC} and V_{BOOST}, as shown in the Electrical Characteristics table. Start-up and continuous operation require that all three of these undervoltage lockout conditions be satisfied because the TG MOSFET driver is disabled during any UVLO fault condition. In startup, for most applications, V_{CC} is powered from V_{IN} through the high voltage linear regulator of the LT3724. This requires V_{IN} to be high enough to drive the V_{CC} voltage above its undervoltage lockout threshold. V_{CC}, in turn, has to be high enough to charge the BOOST capacitor through an external diode so that the BOOST voltage is above its undervoltage lockout threshold. There is an NPN switch that pulls the SW node to ground each cycle during the TG power MOSFET off-time, ensuring the BOOST capacitor is kept fully charged. Once the supply is up and running, the output voltage of the supply can backdrive V_{CC} through an external diode. Internal circuitry disables the high voltage regulator to conserve V_{IN} supply current. Output voltages that are too low or too high to backdrive V_{CC} require additional circuitry such as a voltage doubler or linear regulator. Once V_{CC} is backdriven from a supply other than V_{IN}, V_{IN} can be reduced to 4V with normal operation maintained.

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OPERATIONS (Refer to Functional Diagram)

Soft-Start

The soft-start function controls the slew rate of the power supply output voltage during start-up. A controlled output voltage ramp minimizes output voltage overshoot, reduces inrush current from the V_{IN} supply, and facilitates supply sequencing. A capacitor, C_{SS}, connected between V_{OUT} of the supply and the C_{SS} pin of the IC, programs the slew rate. The capacitor provides a current to the C_{SS} pin which is proportional to the dV/dt of the output voltage. The soft-start circuit overrides the control loop and adjusts the inductor current until the output voltage slew rate yields a 2µA current through the soft-start capacitor. If the current is greater than 2µA, then the current threshold set by the DC control voltage, V_C, is decreased and the inductor current is lowered. This in turn lowers the output current and the output voltage slew rate is decreased. If the current is less than 2µA, then the current threshold set by the DC control voltage, V_C, is increased and the inductor current is raised. This in turn increases the output current and the output voltage slew rate is increased. Once the output voltage is within 5% of its regulation voltage, the soft-start circuit is disabled and the main control regulates the output. The soft-start circuit is reactivated when the output voltage drops below 70% of its regulation voltage.

Slope/Antislope Compensation

The IC incorporates slope compensation to eliminate potential subharmonic oscillations in the current control loop. The IC's slope compensation circuit imposes an artificial ramp on the sensed current to increase the rising slope as duty cycle increases.

Unfortunately, this additional ramp typically affects the sensed current value, thereby reducing the achievable current limit value by the same amount as the added ramp represents. As such, the current limit is typically reduced as the duty cycle increases. The LT3724, however, contains antislope compensation circuitry to eliminate the current limit reduction associated with slope compensation. As the slope compensation ramp is added to the sensed current, a similar ramp is added to the current limit threshold. The end result is that the current limit is not compromised so the LT3724 can provide full power regardless of required duty cycle.

Shutdown

The LT3724 includes a shutdown mode where all the internal IC functions are disabled and the V_{IN} current is reduced to less than 10µA. The shutdown pin can be used for undervoltage lockout with hysteresis, micropower shutdown or as a general purpose on/off control of the converter output. The shutdown function has two thresholds. The first threshold, a precision 1.23V threshold with 120mV of hysteresis, disables the converter from switching. The second threshold, approximately a 0.7V referenced to SGND, completely disables all internal circuitry and reduces the V_{IN} current to less than 10µA. See the Application Information section for more information.

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APPLICATIONS INFORMATION

The basic LT3724 step-down (buck) application, shown in the Typical Application on the front page, converts a larger positive input voltage to a lower positive or negative output voltage. This Application Information section assists selection of external components for the requirements of the power supply.

R_{SENSE} Selection

The current sense resistor, R_{SENSE}, monitors the inductor current of the supply (See Typical Application on front page). Its value is chosen based on the maximum required output load current. The LT3724 current sense amplifier has a maximum voltage threshold of, typically, 150mV. Therefore, the peak inductor current is 150mV/R_{SENSE}. The maximum output load current, $I_{OUT(MAX)}$, is the peak inductor current minus half the peak-to-peak ripple current, ΔI_L.

Allowing adequate margin for ripple current and external component tolerances, R_{SENSE} can be calculated as follows:

$$R_{SENSE} = \frac{100mV}{I_{OUT(MAX)}}$$

Typical values for R_{SENSE} are in the range of 0.005Ω to 0.05Ω.

Inductor Selection

The critical parameters for selection of an inductor are minimum inductance value, volt-second product, saturation current and/or RMS current.

The minimum inductance value is calculated as follows:

$$L \geq V_{OUT} \bullet \frac{V_{IN(MAX)} - V_{OUT}}{f_{SW} \bullet V_{IN(MAX)} \bullet \Delta I_L}$$

f_{SW} is the switch frequency (200kHz).

The typical range of values for ΔI_L is (0.2 • $I_{OUT(MAX)}$) to (0.5 • $I_{OUT(MAX)}$), where $I_{OUT(MAX)}$ is the maximum load current of the supply. Using ΔI_L = 0.3 • $I_{OUT(MAX)}$ yields a good design compromise between inductor performance versus inductor size and cost. Higher values of ΔI_L will increase the peak currents, requiring more filtering on the input and output of the supply. If ΔI_L is too high, the slope compensation circuit is ineffective and current mode instability may occur at duty cycles greater than 50%. Lower values of ΔI_L require larger and more costly magnetics. A value of ΔI_L = 0.3 • $I_{OUT(MAX)}$ produces a ±15% of $I_{OUT(MAX)}$ ripple current around the DC output current of the supply.

Some magnetics vendors specify a volt-second product in their datasheet. If they do not, consult the magnetics vendor to make sure the specification is not being exceeded by your design. The volt-second product is calculated as follows:

$$\text{Volt-second (µsec)} = \frac{(V_{IN(MAX)} - V_{OUT}) \bullet V_{OUT}}{V_{IN(MAX)} \bullet f_{SW}}$$

The magnetics vendors specify either the saturation current, the RMS current or both. When selecting an inductor based on inductor saturation current, use the peak current through the inductor, $I_{OUT(MAX)} + \Delta I_L/2$. The inductor saturation current specification is the current at which the inductance, measured at zero current, decreases by a specified amount, typically 30%.

When selecting an inductor based on RMS current rating, use the average current through the inductor, $I_{OUT(MAX)}$. The RMS current specification is the RMS current at which the part has a specific temperature rise, typically 40°C, above 25°C ambient.

After calculating the minimum inductance value, the volt-second product, the saturation current and the RMS current for your design, select an off-the-shelf inductor. A list of magnetics vendors can be found at www.linear.com, or contact the Linear Technology Application Department.

For more detailed information on selecting an inductor, please see the "Inductor Selection" section of Linear Technology Application Note 44.

Step-Down Converter: MOSFET Selection

The selection criteria of the external N-channel standard level power MOSFET include on resistance($R_{DS(ON)}$), reverse transfer capacitance (C_{RSS}), maximum drain source voltage (V_{DSS}), total gate charge (Q_G), and maximum continuous drain current.

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APPLICATIONS INFORMATION

For maximum efficiency, minimize $R_{DS(ON)}$ and C_{RSS}. Low $R_{DS(ON)}$ minimizes conduction losses while low C_{RSS} minimizes transition losses. The problem is that $R_{DS(ON)}$ is inversely related to C_{RSS}. Balancing the transition losses with the conduction losses is a good idea in sizing the MOSFET. Select the MOSFET to balance the two losses.

Calculate the maximum conduction losses of the MOSFET:

$$P_{COND} = (I_{OUT(MAX)})^2 \left(\frac{V_{OUT}}{V_{IN}} \right) (R_{DS(ON)})$$

Note that $R_{DS(ON)}$ has a large positive temperature dependence. The MOSFET manufacturer's data sheet contains a curve, $R_{DS(ON)}$ vs Temperature.

Calculate the maximum transition losses:

$$P_{TRAN} = (k)(V_{IN})^2 (I_{OUT(MAX)})(C_{RSS})(f_{SW})$$

where k is a constant inversely related to the gate driver current, approximated by k = 2 for LT3724 applications.

The total maximum power dissipation of the MOSFET is the sum of these two loss terms:

$$P_{FET(TOTAL)} = P_{COND} + P_{TRAN}$$

To achieve high supply efficiency, keep the $P_{FET(TOTAL)}$ to less than 3% of the total output power. Also, complete a thermal analysis to ensure that the MOSFET junction temperature is not exceeded.

$$T_J = T_A + P_{FET(TOTAL)} \bullet \theta_{JA}$$

where θ_{JA} is the package thermal resistance and T_A is the ambient temperature. Keep the calculated T_J below the maximum specified junction temperature, typically 150°C.

Note that when V_{IN} is high, the transition losses may dominate. A MOSFET with higher $R_{DS(ON)}$ and lower C_{RSS} may provide higher efficiency. MOSFETs with higher voltage V_{DSS} specification usually have higher $R_{DS(ON)}$ and lower C_{RSS}.

Choose the MOSFET V_{DSS} specification to exceed the maximum voltage across the drain to the source of the MOSFET, which is $V_{IN(MAX)}$ plus any additional ringing on the switch node. Ringing on the switch node can be greatly reduced with good PCB layout and, if necessary, an RC snubber.

The internal V_{CC} regulator operating range limits the maximum total MOSFET gate charge, Q_G, to 90nC. The Q_G vs V_{GS} specification is typically provided in the MOSFET data sheet. Use Q_G at V_{GS} of 8V. If V_{CC} is back driven from an external supply, the MOSFET drive current is not sourced from the internal regulator of the LT3724 and the Q_G of the MOSFET is not limited by the IC. However, note that the MOSFET drive current is supplied by the internal regulator when the external supply back driving V_{CC} is not available such as during startup or short-circuit.

The manufacturer's maximum continuous drain current specification should exceed the peak switch current, $I_{OUT(MAX)} + \Delta I_L/2$.

During the supply startup, the gate drive levels are set by the V_{CC} voltage regulator, which is approximately 8V. Once the supply is up and running, the V_{CC} can be back driven by an auxiliary supply such as V_{OUT}. It is important not to exceed the manufacturer's maximum V_{GS} specification. A standard level threshold MOSFET typically has a V_{GS} maximum of 20V.

Step-Down Converter: Rectifier Selection

The rectifier diode (D1 on the Functional Diagram) in a buck converter generates a current path for the inductor current when the main power switch is turned off. The rectifier is selected based upon the forward voltage, reverse voltage and maximum current. A Schottky diode is recommended. Its low forward voltage yields the lowest power loss and highest efficiency. The maximum reverse voltage that the diode will see is $V_{IN(MAX)}$.

In continuous mode operation, the average diode current is calculated at maximum output load current and maximum V_{IN}:

$$I_{DIODE(AVG)} = I_{OUT(MAX)} \frac{V_{IN(MAX)} - V_{OUT}}{V_{IN(MAX)}}$$

To improve efficiency and to provide adequate margin for short-circuit operation, a diode rated at 1.5 to 2 times the maximum average diode current, $I_{DIODE(AVG)}$, is recommended.

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APPLICATIONS INFORMATION

Step-Down Converter: Input Capacitor Selection

A local input bypass capacitor is required for buck converters because the input current is pulsed with fast rise and fall times. The input capacitor selection criteria are based on the bulk capacitance and RMS current capability. The bulk capacitance will determine the supply input ripple voltage. The RMS current capability is used to keep from overheating the capacitor.

The bulk capacitance is calculated based on maximum input ripple, ΔV_{IN}:

$$C_{IN(BULK)} = \frac{I_{OUT(MAX)} \bullet V_{OUT}}{\Delta V_{IN} \bullet f_{SW} \bullet V_{IN(MIN)}}$$

ΔV_{IN} is typically chosen at a level acceptable to the user. 100mV-200mV is a good starting point. Aluminum electrolytic capacitors are a good choice for high voltage, bulk capacitance due to their high capacitance per unit area.

The capacitor's RMS current is:

$$I_{CIN(RMS)} = I_{OUT} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{(V_{IN})^2}}$$

If applicable, calculate it at the worst case condition, $V_{IN} = 2V_{OUT}$. The RMS current rating of the capacitor is specified by the manufacturer and should exceed the calculated $I_{CIN(RMS)}$. Due to their low ESR (Equivalent Series Resistance), ceramic capacitors are a good choice for high voltage, high RMS current handling. Note that the ripple current ratings from aluminum electrolytic capacitor manufacturers are based on 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required.

The combination of aluminum electrolytic capacitors and ceramic capacitors is an economical approach to meeting the input capacitor requirements. The capacitor voltage rating must be rated greater than $V_{IN(MAX)}$. Multiple capacitors may also be paralleled to meet size or height requirements in the design. Locate the capacitor very close to the MOSFET switch and use short, wide PCB traces to minimize parasitic inductance.

Step-Down Converter: Output Capacitor Selection

The output capacitance, C_{OUT}, selection is based on the design's output voltage ripple, ΔV_{OUT}, and transient load requirements. ΔV_{OUT} is a function of ΔI_L and the C_{OUT} ESR. It is calculated by:

$$\Delta V_{OUT} = \Delta I_L \bullet \left(ESR + \frac{1}{(8 \bullet f_{SW} \bullet C_{OUT})} \right)$$

The maximum ESR required to meet a ΔV_{OUT} design requirement can be calculated by:

$$ESR(MAX) = \frac{(\Delta V_{OUT})(L)(f_{SW})}{V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)}$$

Worst-case ΔV_{OUT} occurs at highest input voltage. Use paralleled multiple capacitors to meet the ESR requirements. Increasing the inductance is an option to lower the ESR requirements. For extremely low ΔV_{OUT}, an additional LC filter stage can be added to the output of the supply. Application Note 44 has some good tips on sizing an additional output filter.

Output Voltage Programming

A resistive divider sets the DC output voltage according to the following formula:

$$R2 = R1\left(\frac{V_{OUT}}{1.231V} - 1\right)$$

The external resistor divider is connected to the output of the converter as shown in Figure 2. Tolerance of the feedback resistors will add additional error to the output voltage.

Example: V_{OUT} = 12V; R1 = 10kΩ

$$R2 = 10k\Omega\left(\frac{12V}{1.231V} - 1\right) = 87.48k\Omega - \text{use } 86.6k\Omega\ 1\%$$

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APPLICATIONS INFORMATION

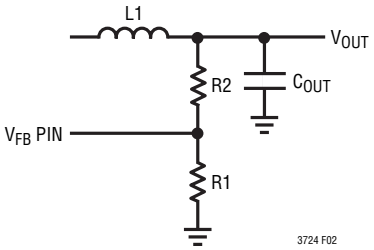

Figure 2. Output Voltage Feedback Divider

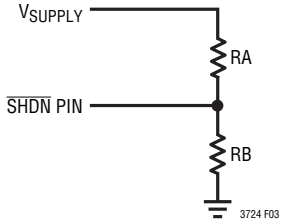

Figure 3. Undervoltage Lockout Circuit

The V_{FB} pin input bias current is typically 25nA, so use of extremely high value feedback resistors could cause a converter output that is slightly higher than expected. Bias current error at the output can be estimated as:

$$\Delta V_{OUT(BIAS)} = 25nA \bullet R2$$

Supply UVLO and Shutdown

The $\overline{SHDN}$ pin has a precision voltage threshold with hysteresis which can be used as an undervoltage lockout threshold (UVLO) for the power supply. Undervoltage lockout keeps the LT3724 in shutdown until the supply input voltage is above a certain voltage programmed by the user. The hysteresis voltage prevents noise from falsely tripping UVLO.

Resistors are chosen by first selecting RB. Then:

$$RA = RB \bullet \left(\frac{V_{SUPPLY(ON)}}{1.35V} - 1 \right)$$

$V_{SUPPLY(ON)}$ is the input voltage at which the undervoltage lockout is disabled and the supply turns on.

Example: Select RB = 49.9kΩ, $V_{SUPPLY(ON)}$ = 14.5V (based on a 15V minimum input voltage)

$$RA = 49.9k\Omega \bullet \left(\frac{14.5V}{1.35V} - 1 \right)$$

$$= 486.1k\Omega \text{ (499k}\Omega \text{ resistor is selected)}$$

If low supply current in standby mode is required, select a higher value of RB.

The supply turn off voltage is 9% below turn on. In the example the $V_{SUPPLY(OFF)}$ would be 13.2V.

If additional hysteresis is desired for the enable function, an external positive feedback resistor can be used from the LT3724 regulator output.

The shutdown function can be disabled by connecting the $\overline{SHDN}$ pin to the V_{IN} through a large value pull-up resistor. This pin contains a low impedance clamp at 6V, so the $\overline{SHDN}$ pin will sink current from the pull-up resistor(R_{PU}):

$$I_{\overline{SHDN}} = \frac{V_{IN} - 6V}{R_{PU}}$$

Because this arrangement will clamp the $\overline{SHDN}$ pin to the 6V, it will violate the 5V absolute maximum voltage rating of the pin. This is permitted, however, as long as the absolute maximum input current rating of 1mA is not exceeded. Input $\overline{SHDN}$ pin currents of <100µA are recommended: a 1MΩ or greater pull-up resistor is typically used for this configuration.

Soft-Start

The soft-start function forces the programmed slew rate while the converter output rises to 95% of regulation, which corresponds to 1.185V on the V_{FB} pin. Once 95% regulation is achieved, the soft-start circuit is disabled. The soft-start circuit will re-enable when the V_{FB} pin drops below 70% of regulation, which corresponds to 300mV of control hysteresis on the V_{FB} pin. This allows for a controlled recovery from a "brown-out" condition.

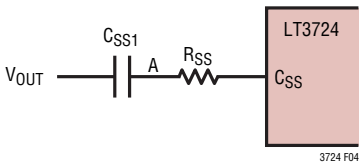

Figure 4.Soft-Start Circuit

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APPLICATIONS INFORMATION

The desired soft-start rise time (t_{SS}) is programmed via a programming capacitor C_{SS1}, using a value that corresponds to 2µA average current during the soft-start interval. This capacitor value follows the relation:

$$C_{SS1} = \frac{2 \bullet 10^{-6} \bullet t_{SS}}{V_{OUT}}$$

R_{SS} is typically set to 200k for most applications.

Considerations for Low-Voltage Output Applications

The LT3724 C_{SS} pin biases to 220mV during the soft-start cycle, and this voltage is increased at Figure 4 node "A" by the 2µA signal current through R_{SS}, so the output has to reach this value before the soft-start function is engaged. The value of this output soft-start startup voltage offset ($V_{OUT(SS)}$) follows the relation:

$$V_{OUT(SS)} = 220mV + R_{SS} \bullet 2 \bullet 10^{-6}$$

Which is typically 0.64V for R_{SS} = 200k.

In some low voltage output applications, it may be desirable to reduce the value of this soft-start startup voltage offset. This is possible by reducing the value of R_{SS}. With reduced values of R_{SS}, the signal component caused by voltage ripple on the output must be minimized for proper soft-start operation.

Peak-to-peak output voltage ripple (ΔV_{OUT}) will be imposed on node "A" through the capacitor C_{SS1}. The value of R_{SS} can be set using the following equation:

$$R_{SS} = \frac{\Delta V_{OUT}}{1.3 \bullet 10^{-6}}$$

It is important to use low ESR output capacitors for LT3724 voltage converter designs to minimize this ripple voltage component. A design with an excessive ripple component can be evidenced by observing the V_C pin during the start cycle.

The soft-start cycle should be evaluated to verify that the reduced R_{SS} value allows operation without excessive modulation of the V_C pin before finalizing the design.

If V_C pin has an excessive ripple component during the soft-start cycle, converter output ripple should be reduced.

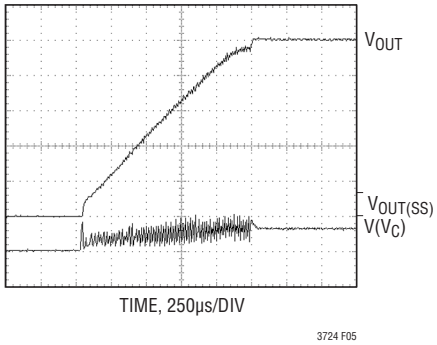

Figure 5. Soft-Start Characteristic Showing Excessive Ripple Component

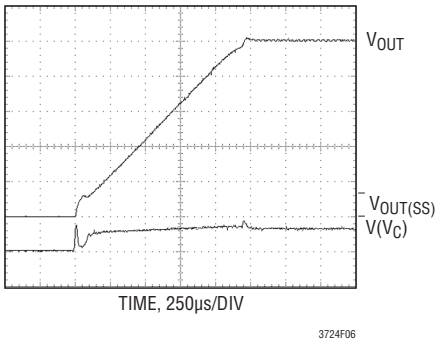

Figure 6. Desirable Soft-Start Characteristic

This is typically accomplished by increasing output capacitance and/or reducing output capacitor ESR.

External Current Limit Foldback Circuit

An additional startup voltage offset can occur during the period before the LT3724 soft-start circuit becomes active. Before the soft-start circuit throttles back the V_C pin in response to the rising output voltage, current as high as the peak programmed current limit (I_{MAX}) can flow in the switched inductor. Switching will stop once the soft-start circuit takes hold and reduces the voltage on the V_C pin, but the output voltage will continue to increase as the stored energy in the inductor is transferred to the output capacitor. With I_{MAX} in the inductor, the resulting leading-edge rise on V_{OUT} due to energy stored in the inductor follows the relation:

$$\Delta V_{OUT} = I_{MAX} \bullet \left(\frac{L}{C_{OUT}} \right)^{1/2}$$

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APPLICATIONS INFORMATION

Inductor current typically does not reach I_{MAX} in the few cycles that occur before soft-start becomes active, but can with high input voltages or small inductors, so the above relation is useful as a worst-case scenario.

This energy transfer increase in output voltage is typically small, but for some low voltage applications with relatively small output capacitors, it can become significant. The voltage rise can be reduced by increasing output capacitance, which puts additional limitations on C_{OUT} for these low voltage supplies. Another approach is to add an external current limit foldback circuit which reduces the value of I_{MAX} during start-up.

An external current limit foldback circuit can be easily incorporated into an LT3724 DC/DC converter application by placing a 1N4148 diode and a 47kΩ resistor from the converter output (V_{OUT}) to the LT3724's V_C pin. This limits the peak current to 0.25 • I_{MAX} when V_{OUT} = 0V. A current limit foldback circuit also has the added advantage of providing reduced output current in the DC/DC converter during short-circuit fault conditions, so a foldback circuit may be useful even if the soft-start function is disabled.

If the soft-start circuit is disabled by shorting the C_{SS} pin to ground, the external current limit foldback circuit must be modified by adding an additional diode and resistor. The 2-diode, 2-resistor network shown also provides 0.25 • I_{MAX} when V_{OUT} = 0V.

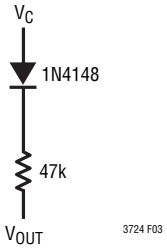

Figure 7. Current Limit Foldback Circuit for Applications that use Soft-Start

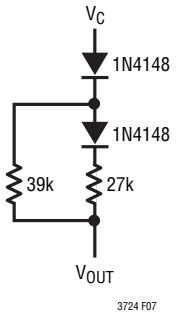

Figure 8. Current Limit Foldback Circuit for Applications that have Soft-Start Disabled (C_{SS} Pin Shorted to SGND)

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. Express percent efficiency as:

% Efficiency = 100% - (L1 + L2 + L3 + ...)

where L1, L2, etc. are individual loss terms as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main contributors usually account for most of the losses in LT3724 circuits:

1. LT3724 V_{IN} and V_{CC} current loss
2. I^2R conduction losses
3. MOSFET transition loss
4. Schottky diode conduction loss

1. The V_{IN} and V_{CC} currents are the sum of the quiescent currents of the LT3724 and the MOSFET drive currents. The quiescent currents are in the LT3724 Electrical Characteristics table. The MOSFET drive current is a result of charging the gate capacitance of the power MOSFET each cycle with a packet of charge, Q_G. Q_G is found in the MOSFET data sheet. The average charging current is calculated as Q_G • f_{SW}. The power loss term due to these currents can be reduced by backdriving V_{CC} with a lower voltage than V_{IN} such as V_{OUT}.

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APPLICATIONS INFORMATION

2. I^2R losses are calculated from the DC resistances of the MOSFET, the inductor, the sense resistor, and the input and output capacitors. In continuous conduction mode the average output current flows through the inductor and R_{SENSE} but is chopped between the MOSFET and the Schottky diode. The resistances of the MOSFET ($R_{DS(ON)}$) and the R_{SENSE} multiplied by the duty cycle can be summed with the resistances of the inductor and R_{SENSE} to obtain the total series resistance of the circuit. The total conduction power loss is proportional to this resistance and usually accounts for between 2% to 5% loss in efficiency.

3. Transition losses of the MOSFET can be substantial with input voltages greater than 20V. See MOSFET Selection section.

4. The Schottky diode can be a major contributor of power loss especially at high input to output voltage ratios (low duty cycles) where the diode conducts for the majority of the switch period. Lower V_f reduces the losses. Note that oversizing the diode does not always help because as the diode heats up the V_f is reduced and the diode loss term is decreased.

I^2R losses and the Schottky diode loss dominate at high load currents. Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% total additional loss in efficiency.

PCB Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation. These items are illustrated graphically in the layout diagram of Figure 9.

1. Keep the signal and power grounds separate. The signal ground consists of the LT3724 SGND pin, the exposed pad on the backside of the LT3724 IC and the (–) terminal of V_{OUT}. The signal ground is the quiet ground and does not contain any high, fast currents. The power ground consists of the Schottky diode anode, the (–) terminal of the input capacitor, and the ground return of the V_{CC} capacitor. This ground has very fast high currents and is considered the noisy ground. The two grounds are connected to each other only at the (–) terminal of V_{OUT}.

2. Use short wide traces in the loop formed by the MOSFET, the Schottky diode and the input capacitor to minimize high frequency noise and voltage stress from parasitic inductance. Surface mount components are preferred.

3. Connect the V_{FB} pin directly to the feedback resistors independent of any other nodes, such as the $SENSE^-$ pin. Connect the feedback resistors between the (+) and (–) terminals of C_{OUT}. Locate the feedback resistors in close proximity to the LT3724 to keep the high impedance node, V_{FB}, as short as possible.

4. Route the $SENSE^-$ and $SENSE^+$ traces together and keep as short as possible.

5. Locate the V_{CC} and BOOST capacitors in close proximity to the IC. These capacitors carry the MOSFET driver's high peak currents. Place the small signal components away from high frequency switching nodes (BOOST, SW, and TG). In the layout shown in Figure 9, place all the small signal components on one side of the IC and all the power components on the other. This helps to keep the signal and power grounds separate.

6. A small decoupling capacitor (100pF) is sometimes useful for filtering high frequency noise on the feedback and sense nodes. If used, locate as close to the IC as possible.

7. The LT3724 packaging will efficiently remove heat from the IC through the exposed pad on the backside of the part. The exposed pad is soldered to a copper footprint on the PCB. Make this footprint as large as possible to improve the thermal resistance of the IC case to ambient air. This helps to keep the LT3724 at a lower temperature.

8. Make the trace connecting the gate of MOSFET M1 to the TG pin of the LT3724 short and wide.

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APPLICATIONS INFORMATION

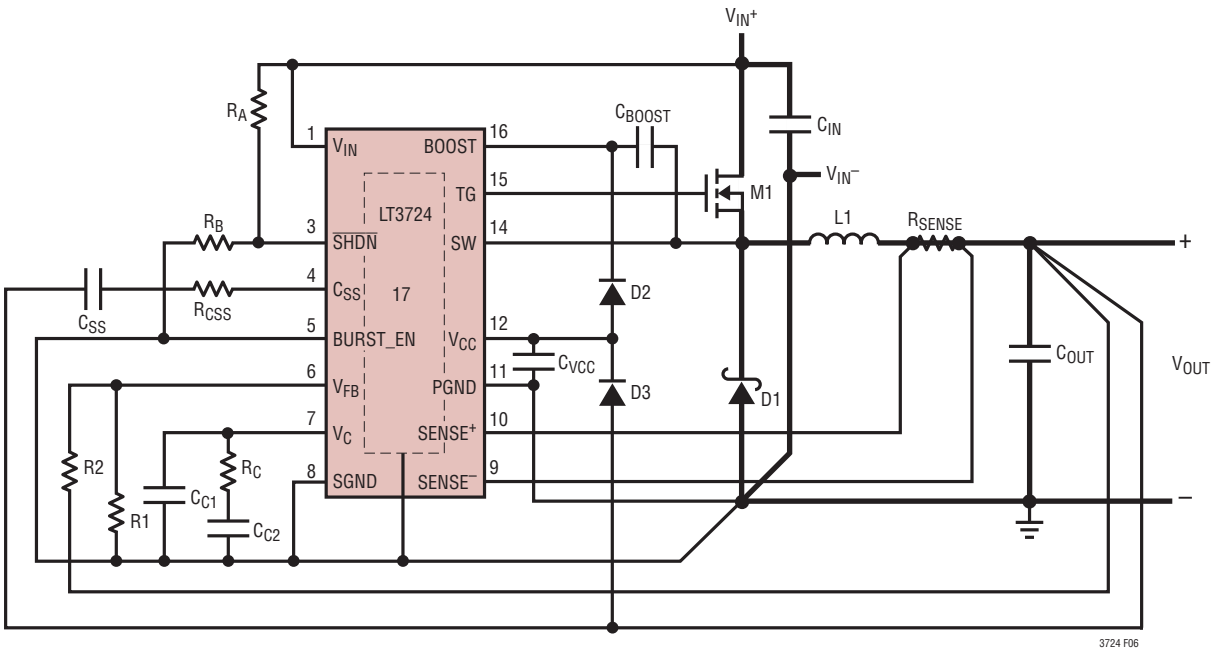

Figure 9. LT3724 Layout Diagram (See PCB Layout Checklist).

Minimum On-Time Considerations (Step-Down Converters)

Minimum on-time ($t_{TG(ON)}$) is the least amount of time that the LT3724 is capable of turning the MOSFET on and then off again. It is determined by internal timing delays and the gate charge of the MOSFET. Applications with high input to output differential voltages operate at low duty cycles and may approach this minimum on-time, typically 300nS. The LT3724 switching frequency is internally set to 200kHz, therefore, the minimum duty cycle of the MOSFET switch is 6%. When the duty cycle needs to be less than 6% the output will stay regulated, but cycle skipping may occur. Cycle skipping results in an increase in inductor ripple current. If it is important that cycle skipping does not occur, follow this guideline which takes into account worst case f_{SW} and $t_{TG(ON)}$:

$$V_{IN(MAX)} \leq 9 \bullet V_{OUT}$$

This is only an issue for supplies with $V_{OUT} < 7V$.

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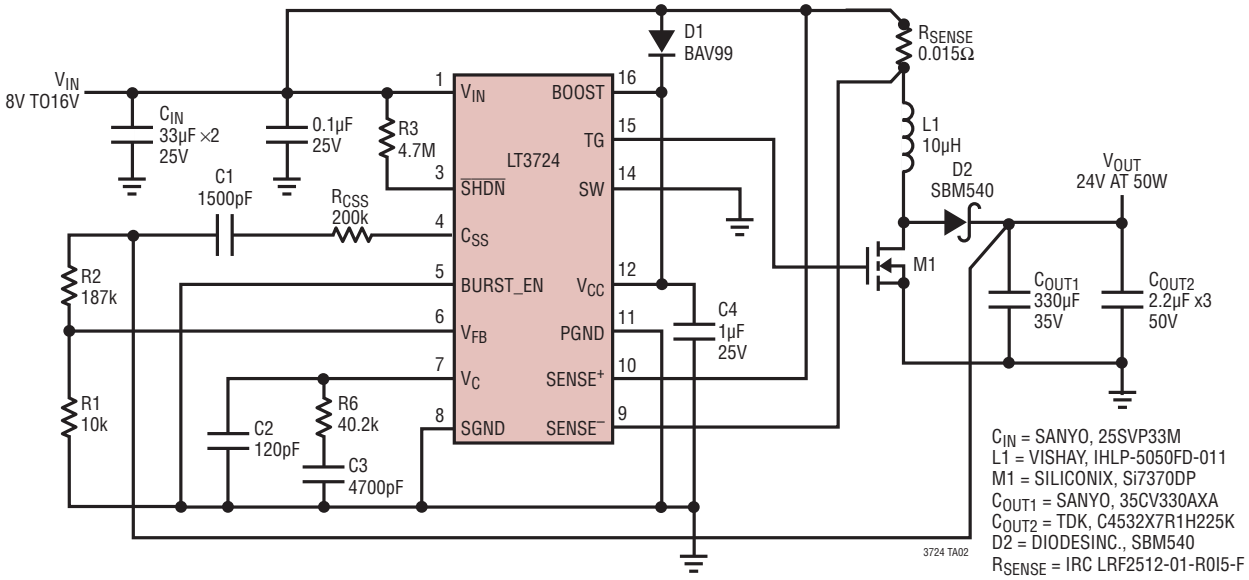
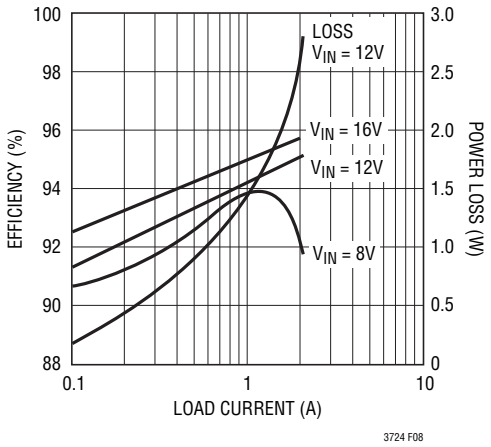
TYPICAL APPLICATIONS

12V to 24V/50W Boost (Step-Up) Converter



CIN = SANYO, 25SVP33M
L1 = VISHAY, IHLP-5050FD-011
M1 = SILICONIX, Si7370DP
COUT1 = SANYO, 35CV330AXA
COUT2 = TDK, C4532X7R1H225K
D2 = DIODESINC., SBM540
RSENSE = IRC LRF2512-01-R0I5-F

Efficiency and Power Loss vs Load Current



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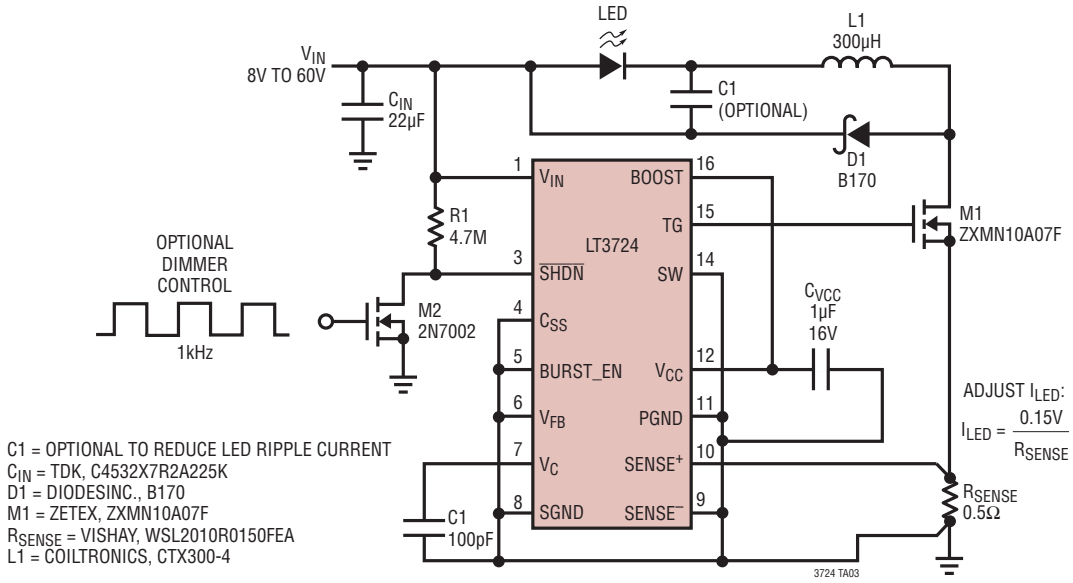
TYPICAL APPLICATIONS

High Voltage LED Driver with Dimmer Control



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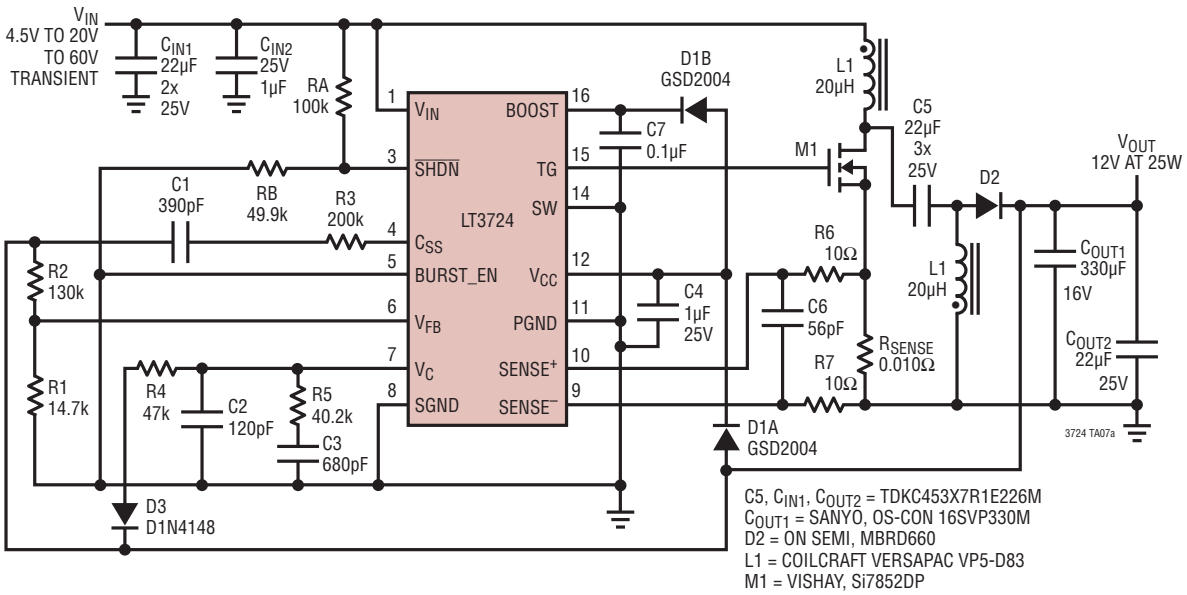
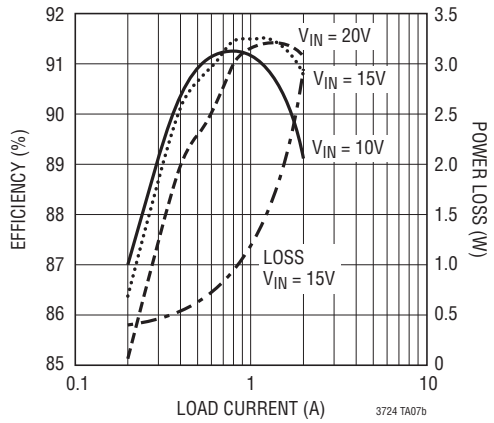
TYPICAL APPLICATIONS

4.5V to 20V Input to 12V at 25W Output SEPIC Converter with 60V Input Transient Capability



Efficiency and Power Loss vs Load Current



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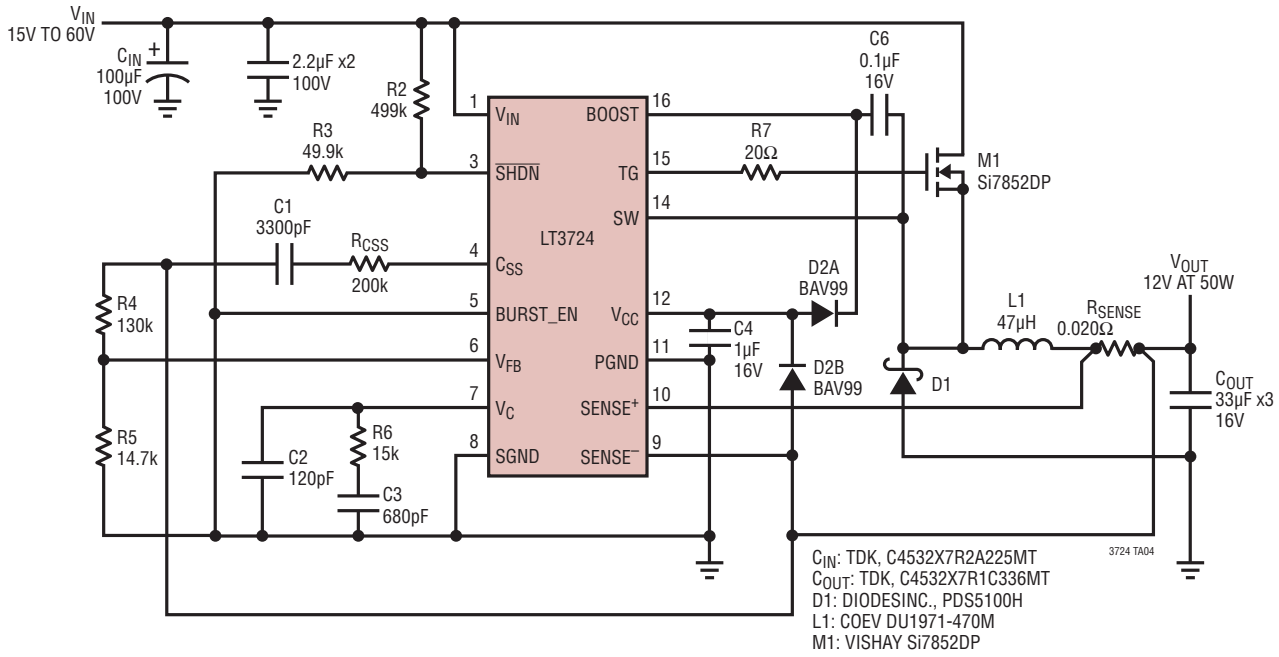
TYPICAL APPLICATIONS

12V Step-Down with V_{CC} Back Driven from V_{OUT} and Ceramic Capacitor in Output Filter



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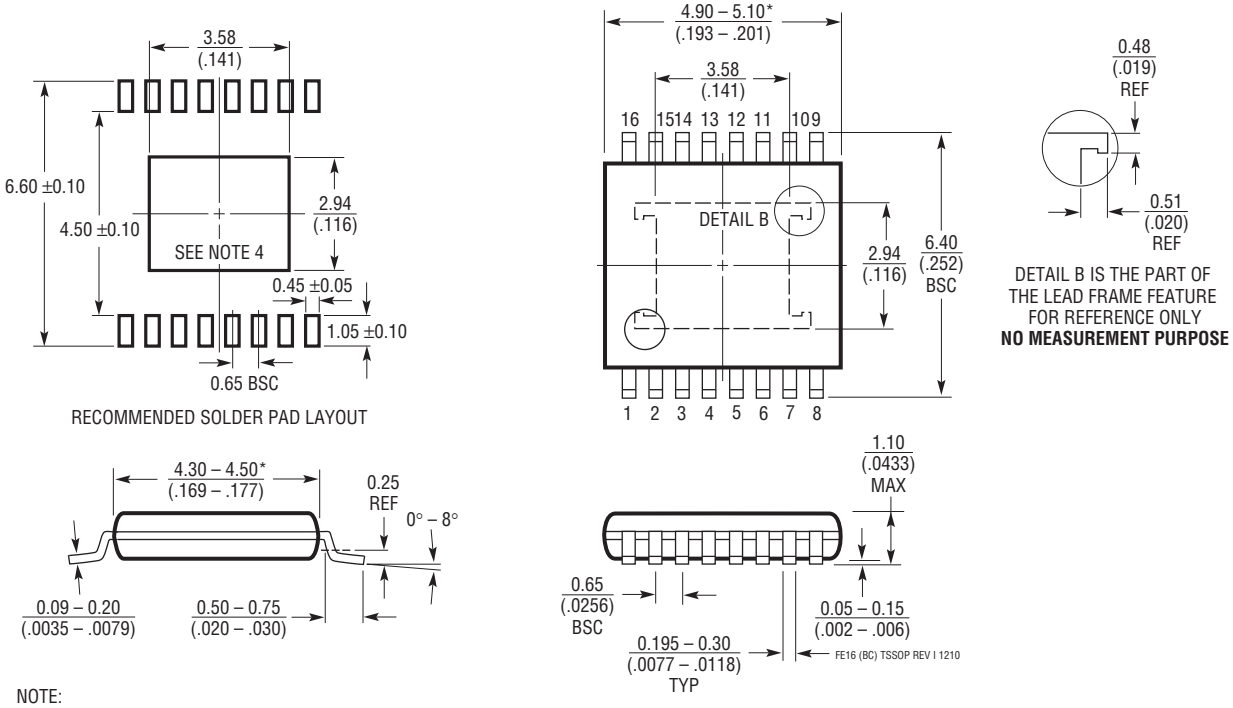
PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev I)
Exposed Pad Variation BC



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS / (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

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REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	3/11	Deleted last paragraph of Description	1
		Minor text edits made to SW and BOOST pin descriptions in Pin Functions section	7
		Minor text edits made to Main Control Loop and Current Limit/Short Circuit sections in Operations	9
		Revised High Voltage LED Driver with Dimmer Control in Typical Applications	21
		Revised Typical Application drawing and Related Parts list	24

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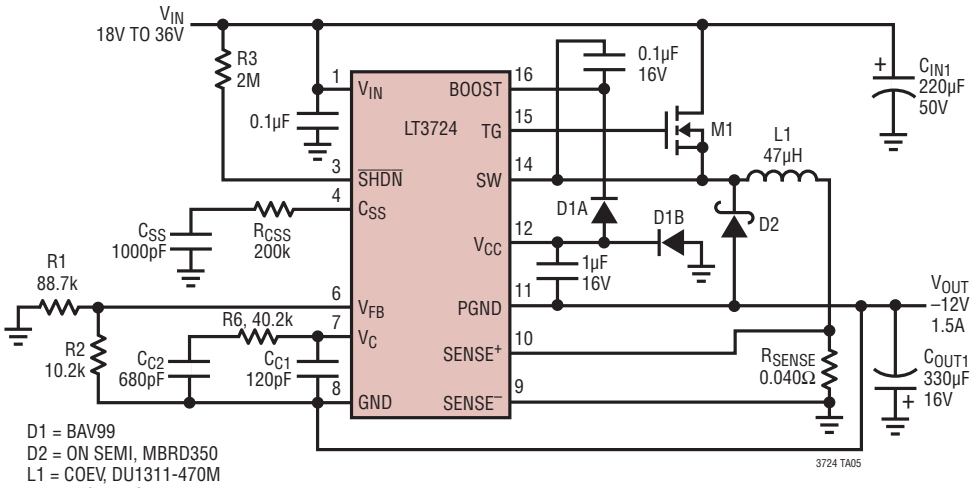
TYPICAL APPLICATION

Inverting –12V 1.5A Converter



D1 = BAV99
D2 = ON SEMI, MBRD350
L1 = COEV, DU1311-470M
M1 = VISHAY, Si7370DP
C_{IN1} = SANYO, 50CV220KX
C_{OUT1} = SANYO, 16SVP330M

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3845A	60V, Low I_Q, High Voltage Synchronous Step-Down DC/DC Controller	Adjustable Fixed Frequency 100kHz to 500kHz, 4V≤ V_{IN} ≤ 60V, 1.23V ≤ V_{OUT} ≤ 36V, I_Q = 120µA, TSSOP-16
LTC3891	60V, Low I_Q, High Voltage Synchronous Step-Down DC/DC Controller	Phase-Lockable Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA
LT3844	60V, Low I_Q, Single Output Step-Down DC/DC Controller	Synchronizable Fixed Frequency 50kHz to 600kHz, 4V≤ V_{IN} ≤ 60V, 1.23V ≤ V_{OUT} ≤ 36V, I_Q = 120µA, TSSOP-16
LT3741	High Power, Constant Current, Constant Voltage, Step-Down Controller	Fixed 200kHz to 1MHz Operating Frequency, ±6% Current Regulation, 6V≤ V_{IN} ≤ 36V, V_{OUT} Up to (V_{IN} - 2V)
LTC3824	60V, Low I_Q, Step-Down DC/DC Controller with 100% Duty Cycle	Selectable Fixed Frequency 200kHz to 600kHz, 4V≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 40µA, MSOP-10E
LTC3834/LTC3834-1 LTC3835/LTC3835-1	Low I_Q, Single Output Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	Phase-Lockable Fixed Frequency 140kHz to 650kHz, 4V≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 10V, I_Q = 30µA/80µA
LTC3859	Low I_Q, Triple Output Buck/Buck/Boost Synchronous DC/DC Controller	All Outputs Remain in Regulation Through Cold Crank 2.5V≤ V_{IN} ≤ 38V, $V_{OUT(BUCKS)}$ Up to 24V, $V_{OUT(BOOST)}$ Up to 60V, I_Q = 55µA

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