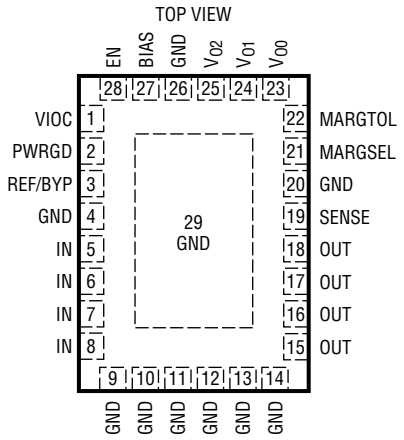
ABSOLUTE MAXIMUM RATINGS

(Note 1)

IN, OUT ..... –0.3V to 3.3V
BIAS ..... –0.3V to 4V
V_{O2}, V_{O1}, V_{O0} Inputs ..... –0.3V to 4V
MARGSEL, MARGTOL Input ..... –0.3V to 4V
EN Input ..... –0.3V to 4V
SENSE Input ..... –0.3V to 4V
VIOC, PWRGD Outputs ..... –0.3V to 4V
REF/BYP Output ..... –0.3V to 4V
Output Short-Circuit Duration ..... Indefinite
Operating Junction Temperature (Note 2)
LT3070-1E/LT3070-1I ..... –40°C to 125°C
LT3070-1MP ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 30°C/W TO 35°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3070EUFD-1#PBF	LT3070EUFD-1#TRPBF	30701	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3070IUFD-1#PBF	LT3070IUFD-1#TRPBF	30701	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3070MPUFD-1#PBF	LT3070MPUFD-1#TRPBF	30701	28-Lead (4mm × 5mm) Plastic QFN	–55°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT3070EUFD-1	LT3070EUFD-1#TR	30701	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3070IUFD-1	LT3070IUFD-1#TR	30701	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3070MPUFD-1	LT3070MPUFD-1#TR	30701	28-Lead (4mm × 5mm) Plastic QFN	–55°C to 125°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. C_{OUT} = 15µF (Note 9), V_{IN} = V_{OUT} + 0.3V (Note 5), V_{BIAS} = 2.5V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN Pin Voltage Range	$V_{IN} \geq V_{OUT}$ + 150mV, I_{OUT}= 5A	●	0.95		3.0	V
BIAS Pin Voltage Range (Note 3)		●	2.2		3.6	V
Regulated Output Voltage	V_{OUT} = 0.8V, 10mA ≤ I_{OUT} ≤ 5A, 1.05V ≤ V_{IN} ≤ 1.25V	●	0.792	0.800	0.808	V
	V_{OUT} = 0.9V, 10mA ≤ I_{OUT} ≤ 5A, 1.15V ≤ V_{IN} ≤ 1.35V	●	0.891	0.900	0.909	V
	V_{OUT} = 1V, 10mA ≤ I_{OUT} ≤ 5A, 1.25V ≤ V_{IN} ≤ 1.45V	●	0.990	1.000	1.010	V
	V_{OUT} = 1.1V, 10mA ≤ I_{OUT} ≤ 5A, 1.35V ≤ V_{IN} ≤ 1.55V	●	1.089	1.100	1.111	V
	V_{OUT} = 1.2V, 10mA ≤ I_{OUT} ≤ 5A, 1.45V ≤ V_{IN} ≤ 1.65V, V_{BIAS} = 3.3V	●	1.188	1.200	1.212	V
	V_{OUT} = 1.5V, 10mA ≤ I_{OUT} ≤ 5A, 1.75V ≤ V_{IN} ≤ 1.95V, V_{BIAS} = 3.3V	●	1.485	1.500	1.515	V
	V_{OUT} = 1.8V, 10mA ≤ I_{OUT} ≤ 5A, 2.05V ≤ V_{IN} ≤ 2.25V, V_{BIAS} = 3.3V	●	1.782	1.800	1.818	V
Regulated Output Voltage Margining (Note 3)	MARGTOL = 0V, MARGSEL = V_{BIAS}	●	0.8	1	1.2	%
	MARGTOL = 0V, MARGSEL = 0V, I_{OUT} = 10mA	●	–1.2	–1	–0.8	%
	MARGTOL = FLOAT, MARGSEL = V_{BIAS}	●	2.7	3	3.3	%
	MARGTOL = FLOAT, MARGSEL = 0V, I_{OUT} = 10mA	●	–3.3	–3	–2.7	%
	MARGTOL = V_{BIAS}, MARGSEL= V_{BIAS}	●	4.6	5	5.4	%
	MARGTOL = V_{BIAS}, MARGSEL = 0V, I_{OUT} = 10mA	●	–5.4	–5	–4.6	%
Line Regulation to V_{IN}	V_{OUT} = 0.8V, ΔV_{IN} = 1.05V to 2.7V, V_{BIAS} = 3.3V, I_{OUT} = 10mA	●			1.0	mV
	V_{OUT} = 1.8V, ΔV_{IN} = 2.05V to 2.7V, V_{BIAS} = 3.3V, I_{OUT} = 10mA	●			1.0	mV
Line Regulation to V_{BIAS}	V_{OUT} = 0.8V, ΔV_{BIAS} = 2.2V to 3.6V, V_{IN} = 1.1V, I_{OUT} = 10mA	●			2.0	mV
	V_{OUT} = 1.8V, ΔV_{BIAS} = 3.25V to 3.6V, V_{IN} = 2.1V, I_{OUT} = 10mA	●			1.0	mV
Load Regulation, ΔI_{OUT} = 10mA to 5A	V_{BIAS} = 2.5V, V_{IN} = 1.05V, V_{OUT} = 0.8V			–1.5	–3.0	mV
		●			–5.5	mV
	V_{BIAS} = 2.5V, V_{IN} = 1.25V, V_{OUT} = 1.0V			–2	–4.0	mV
		●			–7.5	mV
	V_{BIAS} = 3.3V, V_{IN} = 1.45V, V_{OUT} = 1.2V			–2	–4.0	mV
		●			–7.5	mV
	V_{BIAS} = 3.3V, V_{IN} = 1.75V, V_{OUT} = 1.5V			–2.5	–5.0	mV
		●			–9.0	mV
	V_{BIAS} = 3.3V, V_{IN} = 2.05V, V_{OUT} = 1.8V			–3	–7.0	mV
		●			–13	mV
Dropout Voltage, V_{IN} = $V_{OUT(NOMINAL)}$ (Note 6)	I_{OUT} = 1A, V_{OUT} = 1V	●		20	35	mV
	I_{OUT} = 2.5A, V_{OUT} = 1V			50	65	mV
		●			85	mV
	I_{OUT} = 5A, V_{OUT} = 1V			85	120	mV
		●			150	mV
SENSE Pin Current	V_{IN} = 1.1V, V_{SENSE} = 0.8V	●	35	50	65	µA
	V_{BIAS} = 3.3V, V_{IN} = 2.1V, V_{SENSE} = 1.8V	●	200	300	400	µA

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. C_{OUT} = 15µF (Note 9), V_{IN} = V_{OUT} + 0.3V (Note 5), V_{BIAS} = 2.5V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Ground Pin Current, V_{IN} = 1.3V, V_{OUT} = 1V	I_{OUT} = 10mA I_{OUT} = 5A	● ●	0.65 0.9	1.1 1.35	1.8 2.3	mA mA
BIAS Pin Current in Nap Mode	EN = Low	●	120	200	320	µA
BIAS Pin Current, V_{IN} = 1.3V, V_{OUT} = 1V	I_{OUT} = 10mA I_{OUT} = 100mA I_{OUT} = 500mA I_{OUT} = 1A I_{OUT} = 2.5A I_{OUT} = 5A	● ● ● ● ● ●	0.75 1.25 2.0 2.6 3.5 4.5	1.08 1.8 3.0 3.8 5.2 6.9	1.5 2.4 4.0 5.0 7.0 10.0	mA mA mA mA mA mA
Current Limit (Note 5)	V_{IN} – V_{OUT} < 0.3V, V_{BIAS} = 3.3V V_{IN} – V_{OUT} = 1.0V, V_{BIAS} = 3.3V V_{IN} – V_{OUT} = 1.7V, V_{BIAS} = 3.3V	● ● ●	5.1 3.2 1.2	6.4 4.5 2.5	7.7 5.8 4.3	A A A
Reverse Output Current (Note 8)	V_{IN} = 0V, V_{OUT} = 1.8V	●		300	450	µA
PWRGD V_{OUT} Threshold	Percentage of $V_{OUT(NOMINAL)}$, V_{OUT} Rising Percentage of $V_{OUT(NOMINAL)}$, V_{OUT} Falling	● ●	87 82	90 85	93 88	% %
PWRGD V_{OL}	I_{PWRGD} = 200µA (Fault Condition)	●		50	150	mV
V_{BIAS} Undervoltage Lockout	V_{BIAS} Rising V_{BIAS} Falling	● ●	1.1 0.9	1.55 1.4	2.1 1.7	V V
V_{IN}-V_{OUT} Servo Voltage by VIOC		●	250	300	350	mV
VIOC Output Current	V_{IN} = $V_{OUT(NOMINAL)}$ + 150mV, Sourcing Out of the Pin V_{IN} = $V_{OUT(NOMINAL)}$ + 450mV, Sinking Into the Pin	● ●	160 170	235 255	310 340	µA µA
V_{IL} Input Threshold (Logic-0 State), V_{O2}, V_{O1}, V_{O0}, MARGSEL, MARGTOL	Input Falling	●			0.25	V
V_{IZ} Input Range (Logic-Z State), V_{O2}, V_{O1}, V_{O0}, MARGSEL, MARGTOL		●	0.75		V_{BIAS} – 0.9	V
V_{IH} Input Threshold (Logic-1 State), V_{O2}, V_{O1}, V_{O0}, MARGSEL, MARGTOL	Input Rising	●	V_{BIAS} – 0.25			V
Input Hysteresis (Both Thresholds), V_{O2}, V_{O1}, V_{O0}, MARGSEL, MARGTOL				60		mV
Input Current High, V_{O2}, V_{O1}, V_{O0}, MARGSEL, MARGTOL	V_{IH} = V_{BIAS} = 2.5V, Current Flows Into Pin	●		25	40	µA
Input Current Low, V_{O2}, V_{O1}, V_{O0}, MARGSEL, MARGTOL	V_{IL} = 0V, V_{BIAS} = 2.5V, Current Flows Out of Pin	●		25	40	µA
EN Pin Threshold	V_{OUT} = Off to On, V_{BIAS} = 2.5V V_{OUT} = On to Off, V_{BIAS} = 2.5V V_{OUT} = Off to On, V_{BIAS} =2.2V to 3.6V V_{OUT} = On to Off, V_{BIAS} =2.2V to 3.6V	● ● ● ●	 0.9 0.36 • V_{BIAS}		1.4 0.56 • V_{BIAS} 	V V V V
EN Pin Logic High Current	V_{EN} = V_{BIAS} = 2.5V	●	2.5	4.0	6.5	µA

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. C_{OUT} = 15µF (Note 9), V_{IN} = V_{OUT} + 0.3V (Note 5), V_{BIAS} = 2.5V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
EN Pin Logic Low Current	V_{EN} = 0V	●			0.1	µA
V_{BIAS} Ripple Rejection	V_{BIAS} = V_{OUT} + 1.5V_{AVG}, V_{RIPPLE} =0.5V_{P-P} , f_{RIPPLE} = 120Hz, V_{IN} – V_{OUT} = 300mV, I_{OUT} = 2.5A			75		dB
V_{IN} Ripple Rejection (Notes 3, 4, 5)	V_{BIAS} = 2.5V, V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 120Hz, V_{IN} – V_{OUT} = 300mV, I_{OUT} = 2.5A			66		dB
Reference Voltage Noise (REF/BYP Pin)	$C_{REF/BYP}$ = 10nF, BW = 10Hz to 100kHz			10		μV_{RMS}
Output Voltage Noise	V_{OUT} = 1V, I_{OUT} = 5A, $C_{REF/BYP}$ = 10nF, C_{OUT} = 15µF, BW = 10Hz to 100kHz			25		μV_{RMS}

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3070-1 regulators are tested and specified under pulse load conditions such that $T_J \cong T_A$. The LT3070-1E is 100% tested at T_A = 25°C. Performance at –40°C and 125°C is assured by design, characterization and correlation with statistical process controls. The LT3070-1I is guaranteed over the –40°C to 125°C operating junction temperature range. The LT3070-1MP is 100% tested and guaranteed over the –55°C to 125°C operating junction temperature range.

Note 3: To maintain proper performance and regulation, the BIAS supply voltage must be higher than the IN supply voltage. For a given V_{OUT}, the BIAS voltage must satisfy the following conditions: 2.2V ≤ V_{BIAS} ≤ 3.6V and V_{BIAS} ≥ (1.25 • V_{OUT} + 1V). For V_{OUT} ≤ 0.95V, the minimum BIAS voltage is limited to 2.2V.

Note 4: Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum output current, limit the input voltage range to V_{IN} < V_{OUT} + 500mV.

Note 5: The LT3070-1 incorporates safe operating area protection circuitry. Current limit decreases as the V_{IN}-V_{OUT} voltage increases. Current limit foldback starts at V_{IN} – V_{OUT} > 500mV. See the Typical Performance Characteristics for a graph of Current Limit vs V_{IN} – V_{OUT} voltage. The current limit foldback feature is independent of the thermal shutdown circuitry.

Note 6: Dropout voltage, V_{DO}, is the minimum input to output voltage differential at a specified output current. In dropout, the output voltage equals V_{IN} – V_{DO}.

Note 7: GND pin current is tested with V_{IN} = $V_{OUT(NOMINAL)}$ + 300mV and a current source load. VIOC is a buffered output determined by the value of V_{OUT} as programmed by the V_{O2}-V_{O0} pins. VIOC's output is independent of the margining function.

Note 8: Reverse output current is tested with the IN pins grounded and the OUT + SENSE pins forced to the rated output voltage. This is measured as current into the OUT + SENSE pins.

Note 9: Frequency Compensation: The LT3070-1 must be frequency compensated at its OUT pins with a minimum C_{OUT} of 15µF configured as a cluster of (15×) 1µF ceramic capacitors or as a graduated cluster of 10µF/4.7µF/2.2µF ceramic capacitors of the same case size. Linear Technology only recommends X5R or X7R dielectric capacitors.

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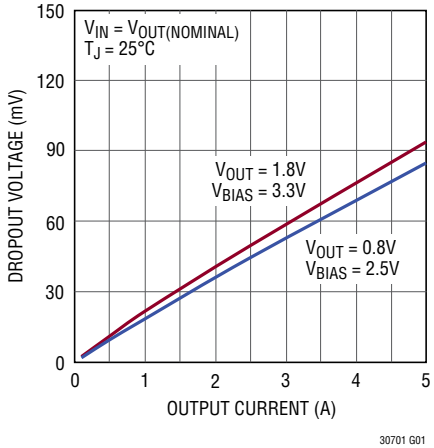
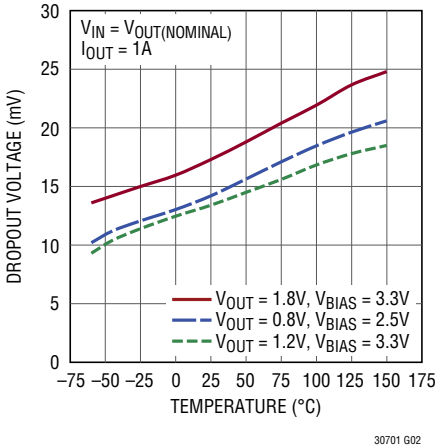
TYPICAL PERFORMANCE CHARACTERISTICS

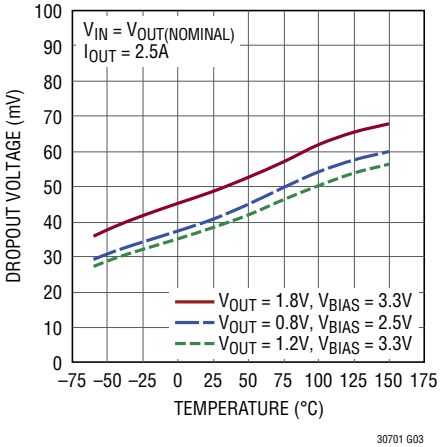
Dropout Voltage vs I_{OUT}



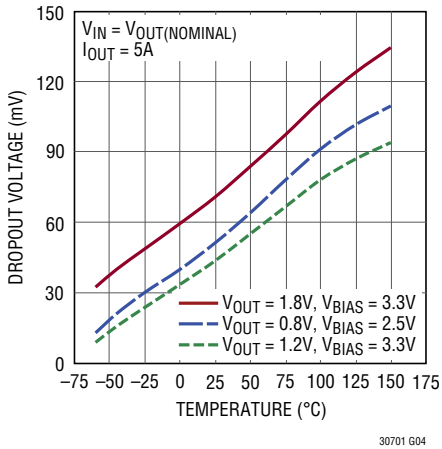
Dropout Voltage vs Temperature



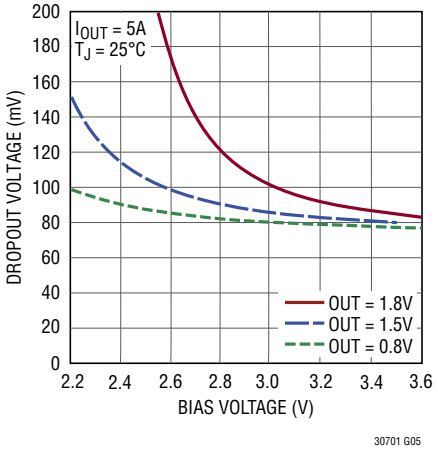
Dropout Voltage vs Temperature



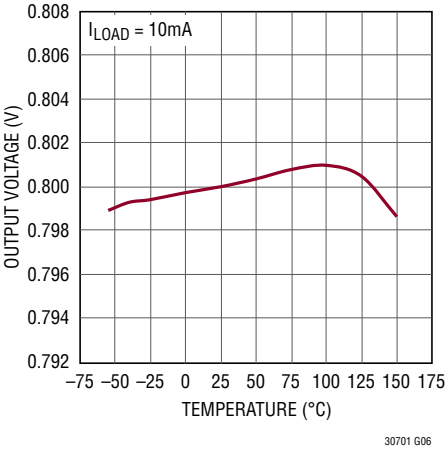
Dropout Voltage vs Temperature



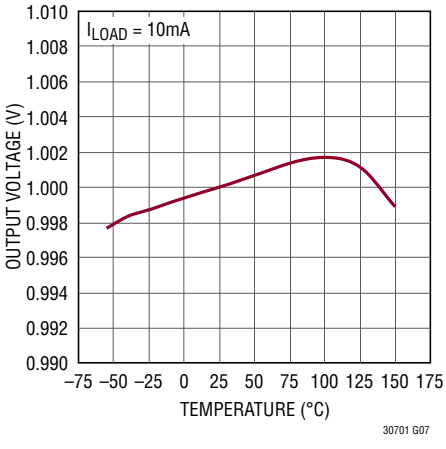
Dropout Voltage vs V_{BIAS}



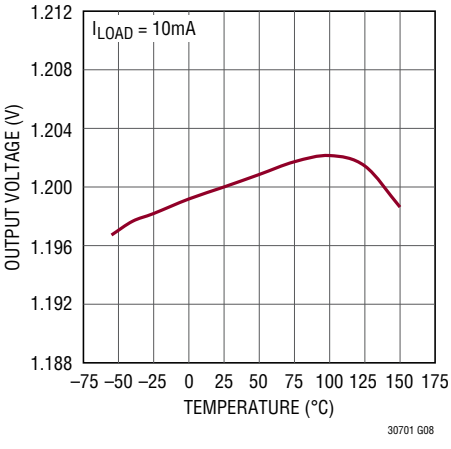
Output Voltage (0.8V) vs Temperature



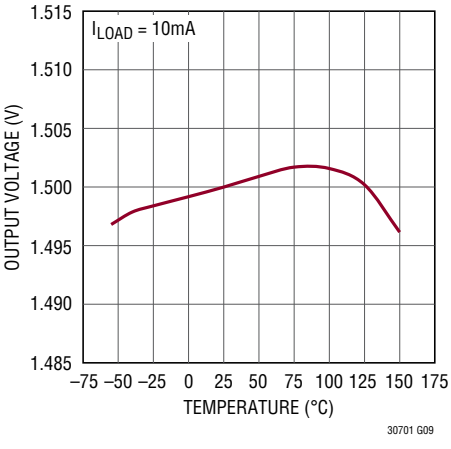
Output Voltage (1V) vs Temperature



Output Voltage (1.2V) vs Temperature



Output Voltage (1.5V) vs Temperature



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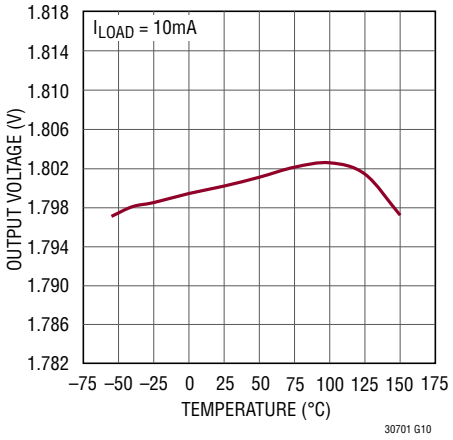
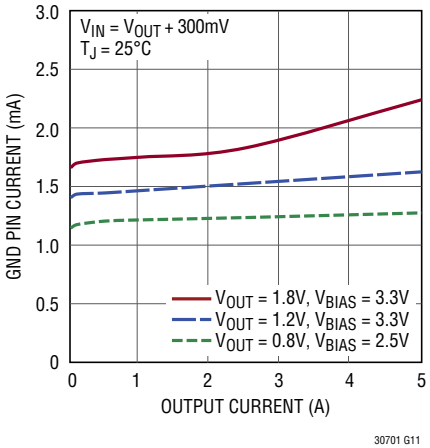
TYPICAL PERFORMANCE CHARACTERISTICS

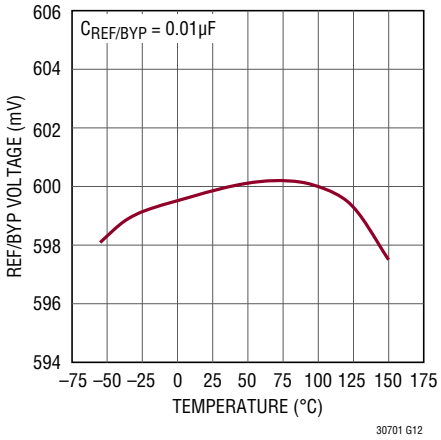
Output Voltage (1.8V) vs Temperature



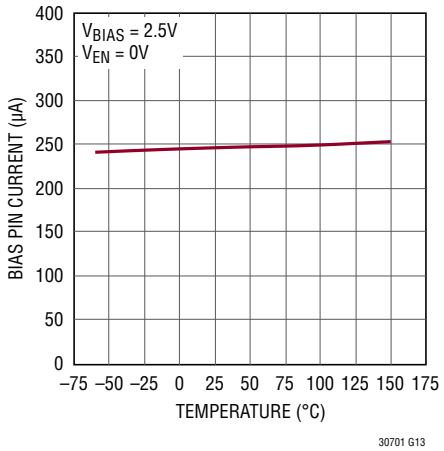
GND Pin Current vs I_{OUT}



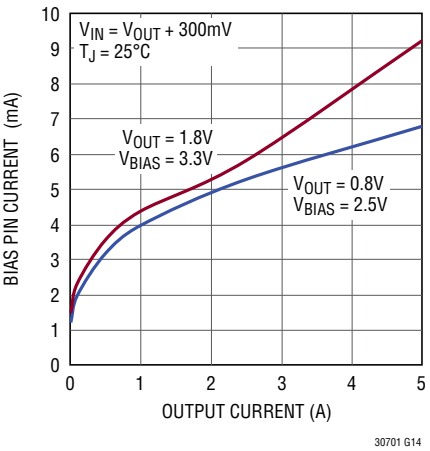
REF/BYP Pin Voltage vs Temperature



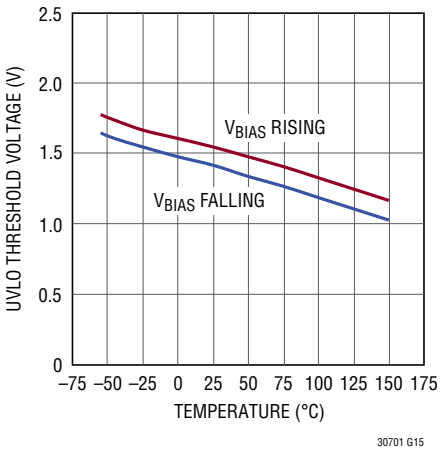
BIAS Pin Current in Nap Mode



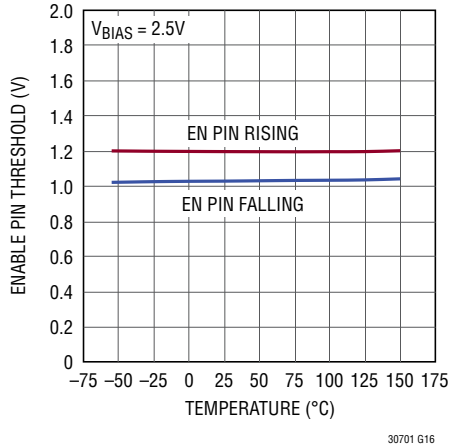
BIAS Pin Current vs I_{OUT}



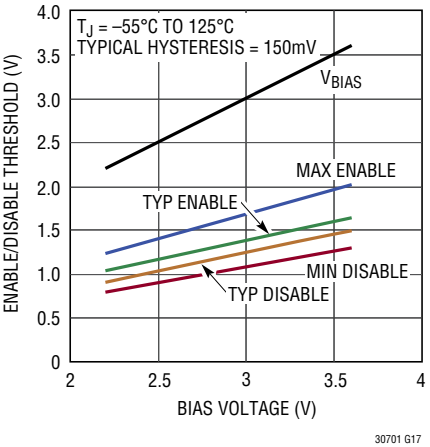
BIAS Pin Undervoltage Lockout Threshold



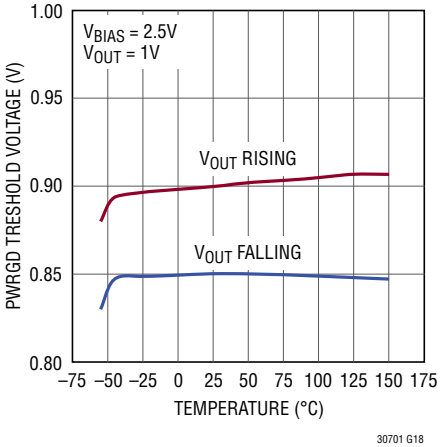
EN Pin Thresholds



Enable Pin Threshold and Hysteresis vs V_{BIAS}



PWRGD Threshold Voltage



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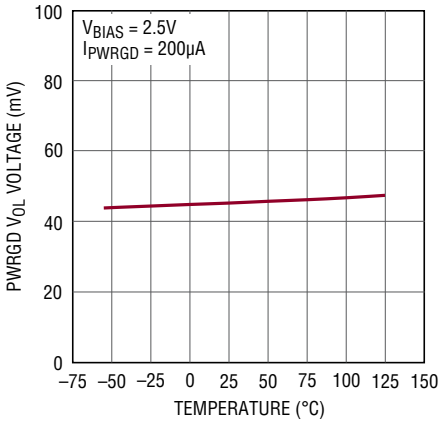
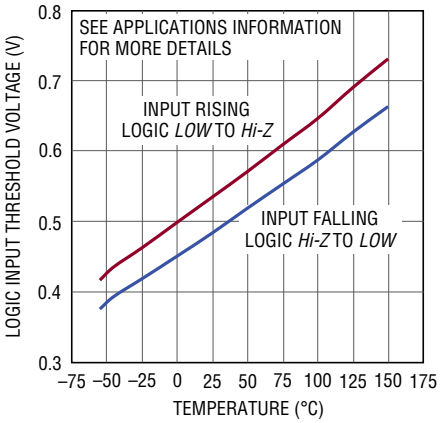
TYPICAL PERFORMANCE CHARACTERISTICS

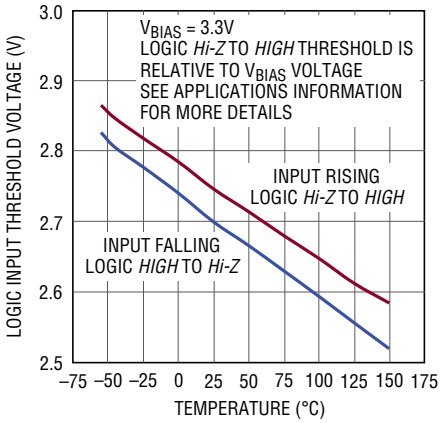
PWRGD V_{OL} vs Temperature



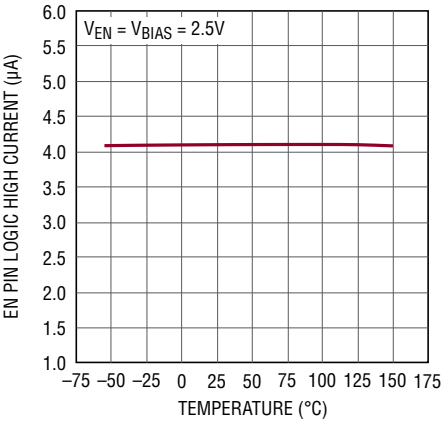
Logic Input Threshold Voltages Logic *Low* to *Hi-Z* State Transitions



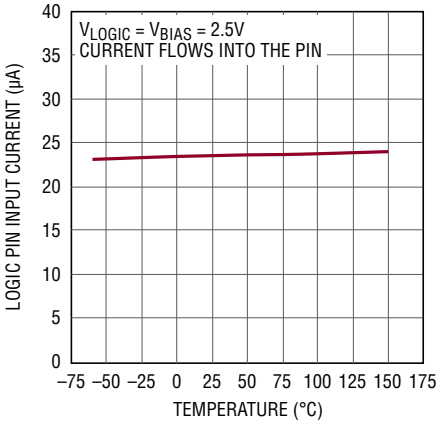
Logic Input Threshold Voltages Logic *Hi-Z* to *High* State Transitions



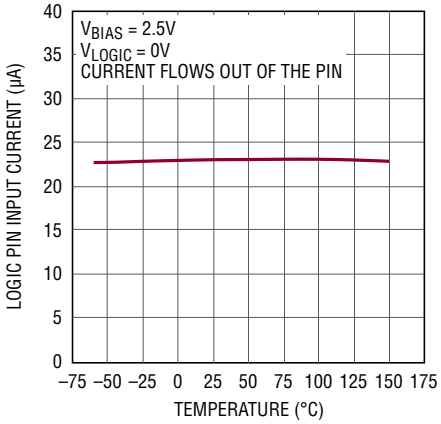
EN Pin Logic High Current



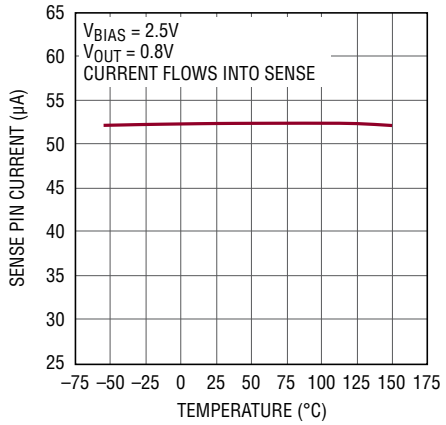
Logic Pin Input Current, *High* State



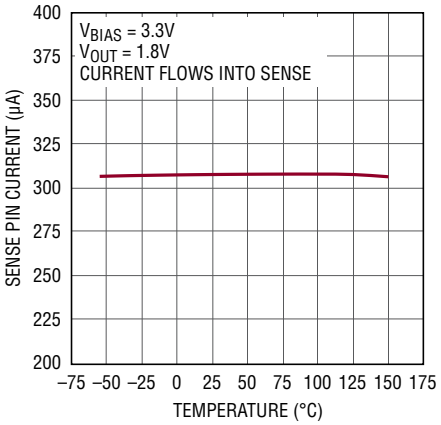
Logic Pin Input Current, *Low* State



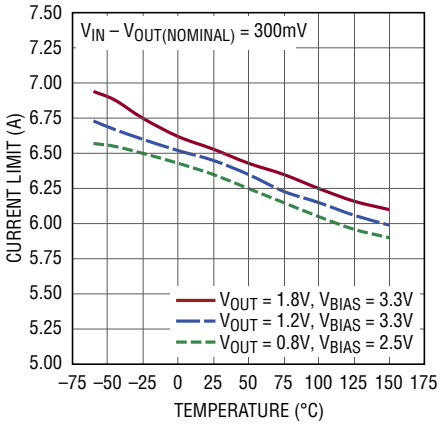
SENSE Pin Current



SENSE Pin Current



Current Limit vs Temperature



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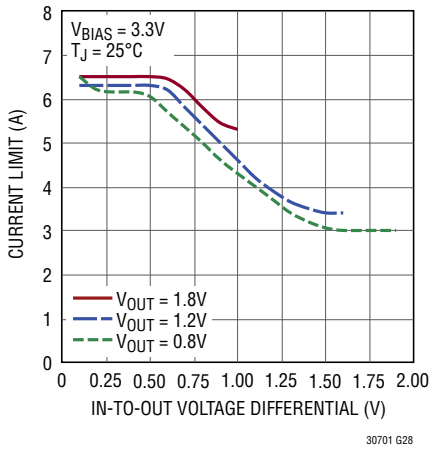
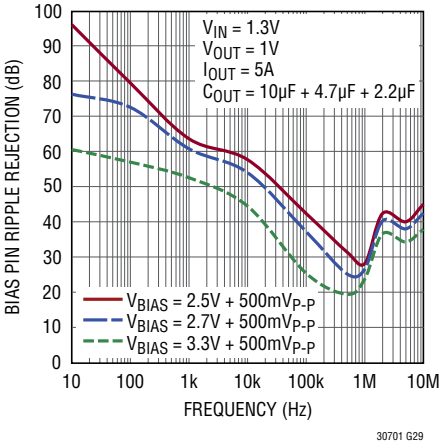
TYPICAL PERFORMANCE CHARACTERISTICS

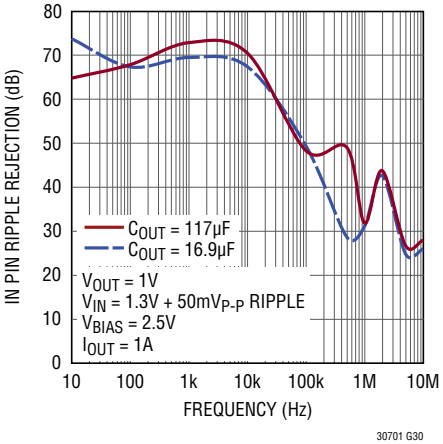
Current Limit vs $V_{IN} - V_{OUT}$



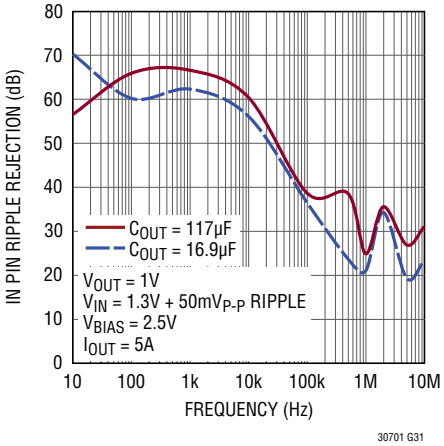
BIAS Pin Ripple Rejection



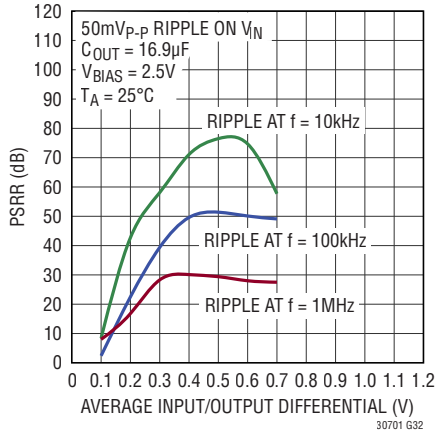
IN Pin Ripple Rejection



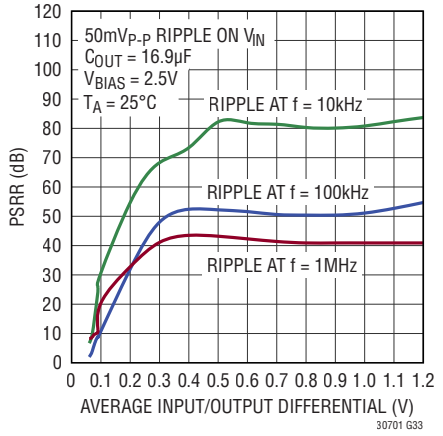
IN Pin Ripple Rejection



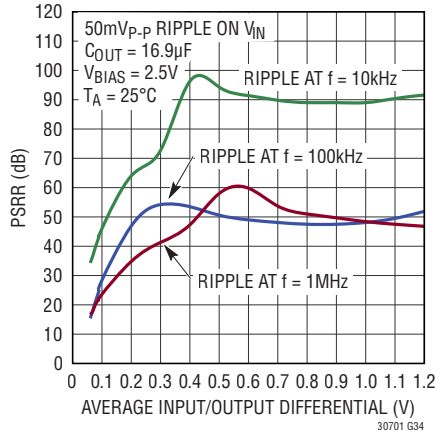
IN Pin Ripple Rejection vs $V_{IN} - V_{OUT}$, 1V/5A



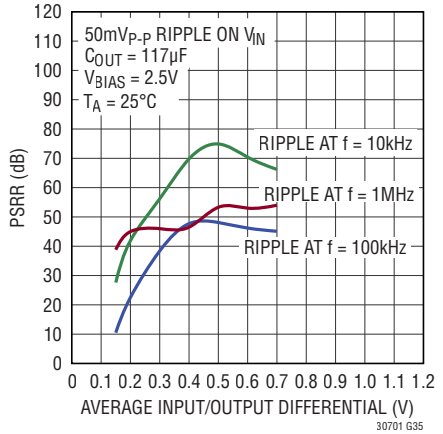
IN Pin Ripple Rejection vs $V_{IN} - V_{OUT}$, 1V/2.5A



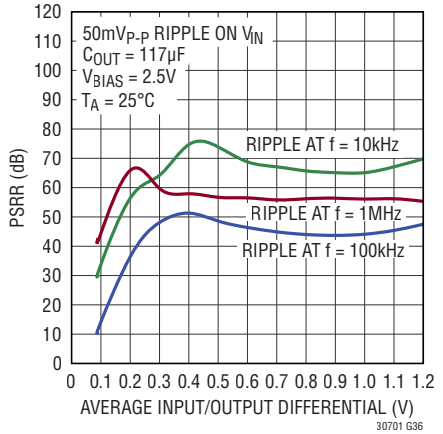
IN Pin Ripple Rejection vs $V_{IN} - V_{OUT}$, 1V/1A



IN Pin Ripple Rejection vs $V_{IN} - V_{OUT}$, 1V/5A



IN Pin Ripple Rejection vs $V_{IN} - V_{OUT}$, 1V/2.5A



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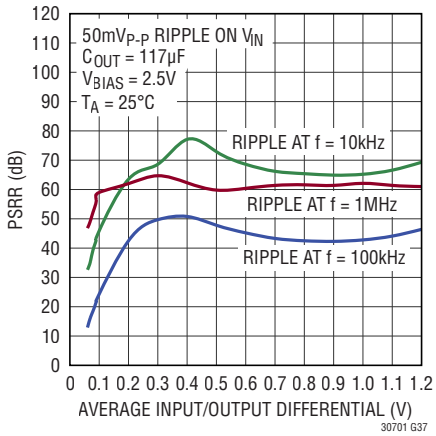
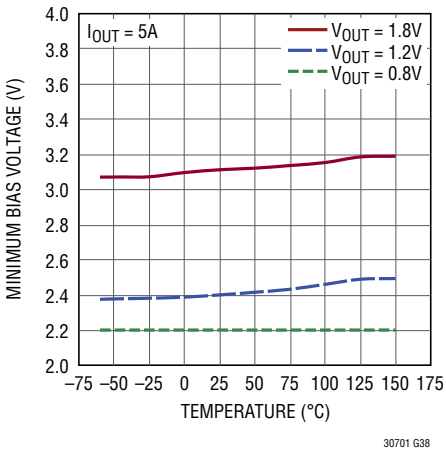
TYPICAL PERFORMANCE CHARACTERISTICS

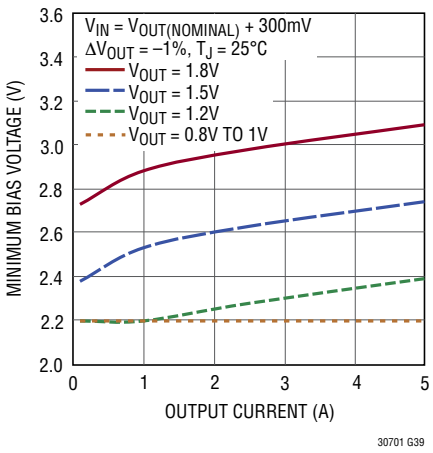
IN Pin Ripple Rejection vs $V_{IN} - V_{OUT}$, 1V/1A



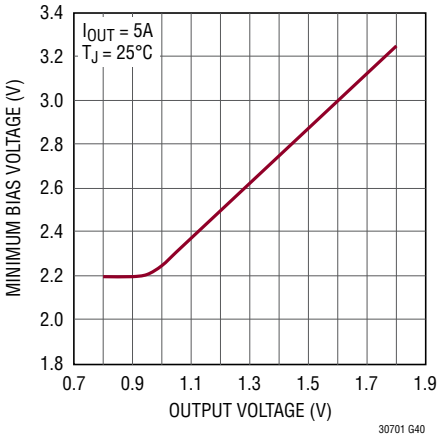
Minimum BIAS Voltage vs Temperature



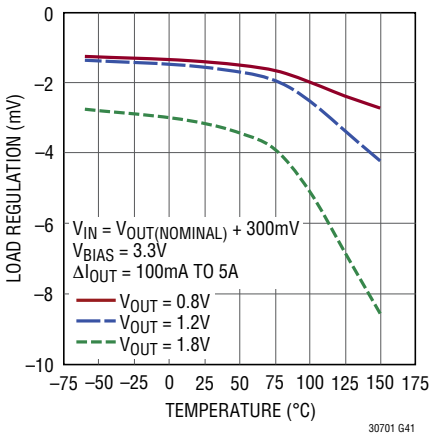
Minimum BIAS Voltage vs I_{OUT}



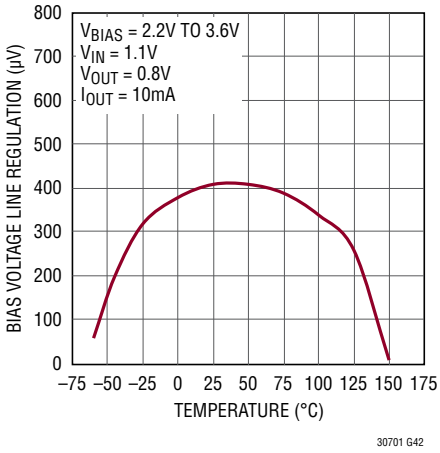
Minimum BIAS Voltage vs V_{OUT}



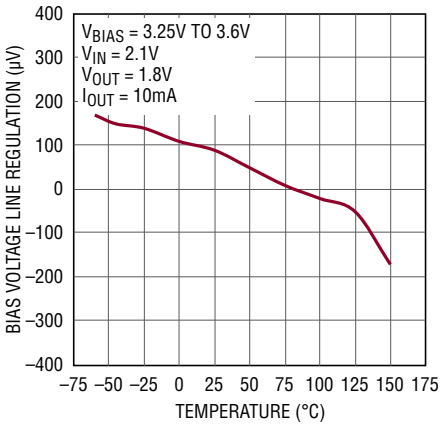
Load Regulation



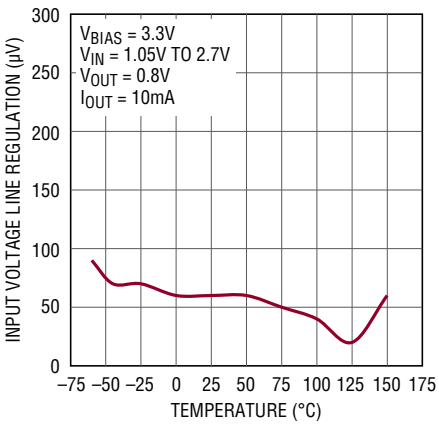
Bias Voltage Line Regulation



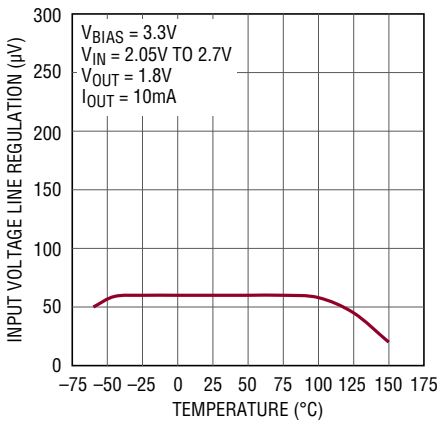
Bias Voltage Line Regulation



Input Voltage Line Regulation



Input Voltage Line Regulation



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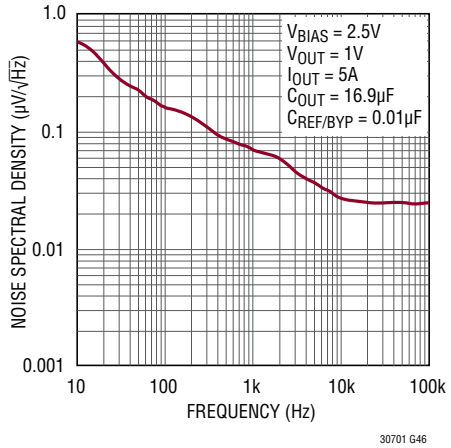
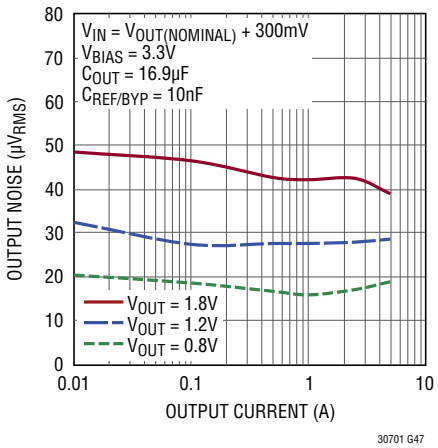
TYPICAL PERFORMANCE CHARACTERISTICS

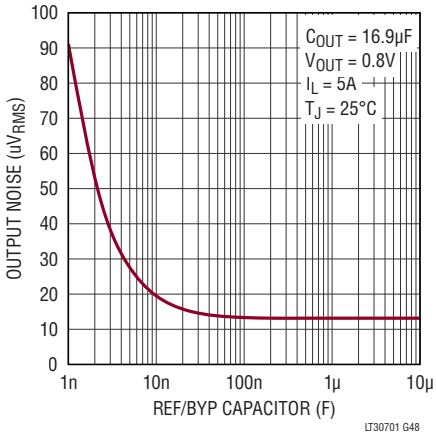
Output Noise Spectral Density



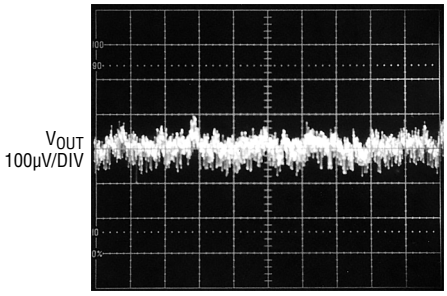
RMS Output Noise vs Output Current



RMS Output Noise vs CREF/BYP

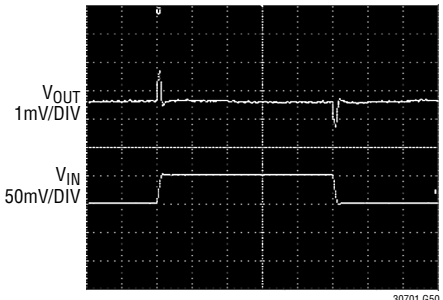


Output Noise (10Hz to 100kHz)



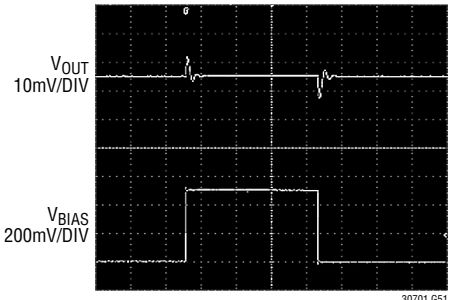
V_{OUT} = 1V
I_{OUT} = 5A
C_{OUT} = 16.9µF
1ms/DIV

Input Voltage Line Transient Response



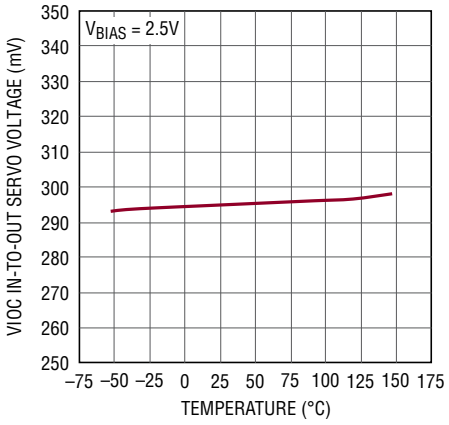
V_{IN} = 1.3V
V_{OUT} = 1V
I_{OUT} = 5A
C_{OUT} = 16.9µF
20µs/DIV

Bias Voltage Line Transient Response

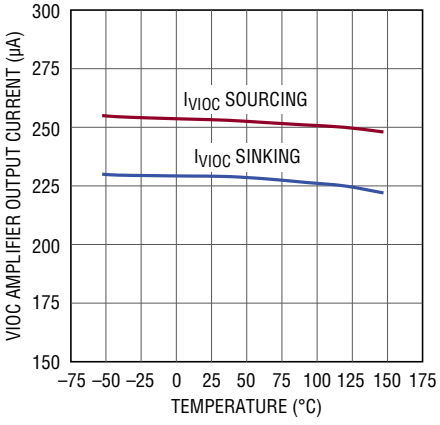


V_{IN} = 1.3V
V_{BIAS} = 2.5V
V_{OUT} = 1V
I_{OUT} = 5A
C_{OUT} = 16.9µF
20µs/DIV

VIOC Amplifier IN-to-OUT Servo Voltage



VIOC Amplifier Output Current vs Temperature



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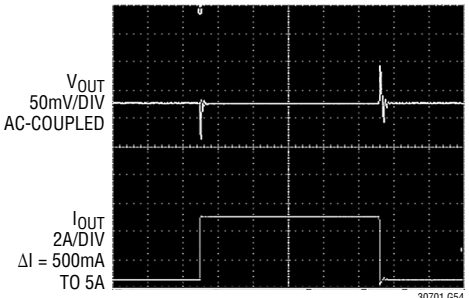
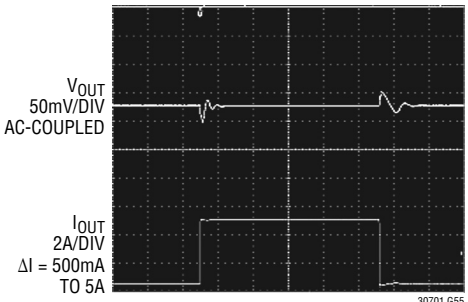
TYPICAL PERFORMANCE CHARACTERISTICS

Transient Load Response



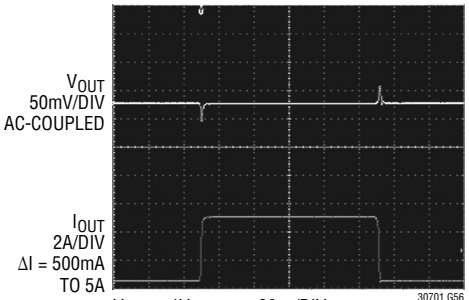
V_{OUT} = 1V 20µs/DIV
C_{OUT} = 10µF + 4.7µF + 2.2µF
I_{OUT} t_{RISE}/t_{FALL} = 100ns

Transient Load Response



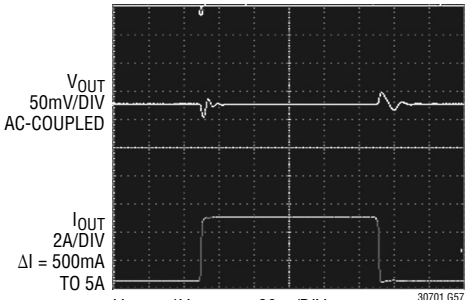
V_{OUT} = 1V 20µs/DIV
C_{OUT} = 117µF
I_{OUT} t_{RISE}/t_{FALL} = 100ns

Transient Load Response



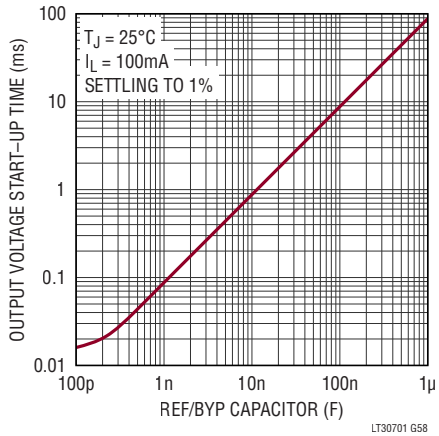
V_{OUT} = 1V 20µs/DIV
C_{OUT} = 10µF + 4.7µF + 2.2µF
I_{OUT} t_{RISE}/t_{FALL} = 1µs

Transient Load Response

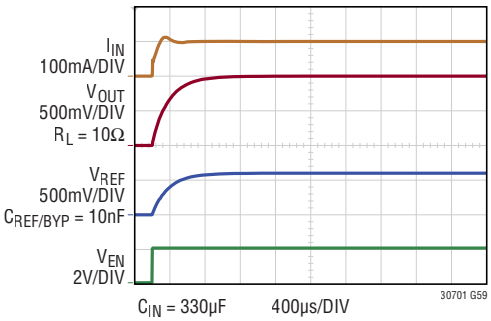


V_{OUT} = 1V 20µs/DIV
C_{OUT} = 117µF
I_{OUT} t_{RISE}/t_{FALL} = 1µs

Output Voltage Start-Up Time vs $C_{REF/BYP}$



EN Start-Up Response



C_{IN} = 330µF 400µs/DIV
C_{OUT} = 16.9µF
V_{OUT} = 1V

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PIN FUNCTIONS

VIOC (Pin 1): Voltage for In-to-Out Control. The IC incorporates a unique tracking function to control a buck regulator powering the LT3070-1's input. The VIOC pin is the output of this tracking function that drives the buck regulator to maintain the LT3070-1's input voltage at V_{OUT} + 300mV. This function maximizes efficiency and minimizes power dissipation. See the Applications Information section for more information on proper control of the buck regulator.

PWRGD (Pin 2): Power Good. The PWRGD pin is an open-drain NMOS output that actively pulls low if any one of these fault modes is detected:

- V_{OUT} is less than 90% of $V_{OUT(NOMINAL)}$ on the rising edge of V_{OUT}.
- V_{OUT} drops below 85% of $V_{OUT(NOMINAL)}$ for more than 25µs.
- Junction temperature typically exceeds 145°C.
- V_{BIAS} is less than its undervoltage lockout threshold.
- The OUT-to-IN reverse-current detector activates.

See the Applications Information section for more information on PWRGD fault modes.

REF/BYP (Pin 3): Reference Filter. The pin is the output of the bandgap reference and has an impedance of approximately 19kΩ. This pin must not be externally loaded. Bypassing the REF/BYP pin to GND with a capacitor decreases output voltage noise and provides a soft-start function to the reference. ADI recommends the use of a high quality, low leakage capacitor. See the Applications Information section for more information on noise and output voltage margining considerations.

GND (Pins 4, 9-14, 20, 26, 29): Ground. The exposed pad (Pin 29) of the QFN package is an electrical connection to GND. To ensure proper electrical and thermal performance, solder Pin 29 to the PCB ground and tie to all GND pins of the package. These GND pins are fused to the internal die attach paddle and the exposed pad to optimize heat sinking and thermal resistance characteristics. See the Applications Information section for thermal considerations and calculating junction temperature.

IN (Pins 5, 6, 7, 8): Input Supply. These pins supply power to the high current pass transistor. Tie all IN pins together for proper performance. The LT3070-1 requires a bypass capacitor at IN to maintain stability and low input impedance over frequency. A 47µF input bypass capacitor suffices for most battery and power plane impedances. Minimizing input trace inductance optimizes performance. Applications that operate with low V_{IN}-V_{OUT} differential voltages and that have large, fast load transients may require much higher input capacitor requirements to prevent the input supply from drooping and allowing the regulator to enter dropout. See the Applications Information section for more information on input capacitor requirements.

OUT (Pins 15, 16, 17, 18): Output. These pins supply power to the load. Tie all OUT pins together for proper performance. A minimum output capacitance of 15µF is required for stability. ADI recommends low ESR, X5R or X7R dielectric ceramic capacitors for best performance. A parallel ceramic capacitor combination of 10µF + 4.7µF + 2.2µF or 15 1µF ceramic capacitors in parallel provide excellent stability and load transient response. Large load transient applications require larger output capacitors to limit peak voltage transients. See the Applications Information section for more information on output capacitor requirements.

SENSE (Pin 19): Kelvin Sense for OUT. The SENSE pin is the inverting input to the error amplifier. Optimum regulation is obtained when the SENSE pin is connected to the OUT pins of the regulator. In critical applications, the resistance (R_P) of PCB traces between the regulator and the load cause small voltage drops, creating a load regulation error at the point of load. Connecting the SENSE pin at the load instead of directly to OUT eliminates this voltage error. Figure 1 illustrates this Kelvin-Sense connection method. Note that the voltage drop across the external PCB traces adds to the dropout voltage of the regulator. The SENSE pin input bias current depends on the selected output voltage. SENSE pin input current varies from 50µA typically at V_{OUT} = 0.8V to 300µA typically at V_{OUT} = 1.8V.

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PIN FUNCTIONS

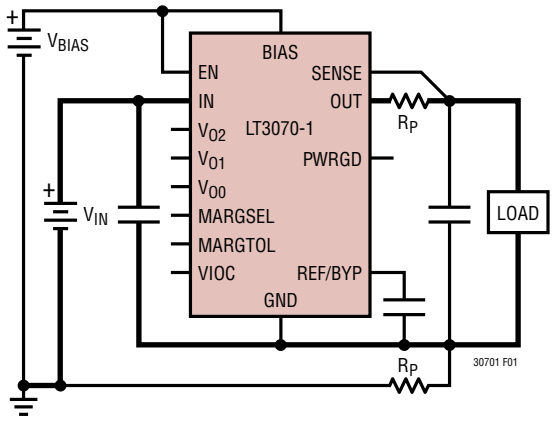

Figure 1. Kelvin Sense Connection

MARGSEL (Pin 21): Margining Enable and Polarity Selection. This three-state pin determines both the polarity and the active state of the margining function. The logic *low* threshold is less than 250mV referenced to GND and enables negative voltage margining. The logic *high* threshold is greater than V_{BIAS} – 250mV and enables positive voltage margining. The voltage range between these two logic thresholds as set by a window comparator defines the logic *Hi-Z* state and disables the margining function.

MARGTOL (Pin 22): Margining Tolerance. This three-state pin selects the absolute value of margining (1%, 3% or 5%) if enabled by the MARGSEL input. The logic *low* threshold is less than 250mV referenced to GND and enables either ±1% change in V_{OUT} depending on the state of the MARGSEL pin. The logic *high* threshold is greater than V_{BIAS} – 250mV and enables either ±5% change in V_{OUT} depending on the state of the MARGSEL pin. The voltage range between these two logic thresholds as set by a window comparator defines the logic *Hi-Z* state and enables either ±3% change in V_{OUT} depending on the state of the MARGSEL pin.

V_{O0}, V_{O1} and V_{O2} (Pins 23, 24, 25): Output Voltage Select. These three-state pins combine to select a nominal output voltage from 0.8V to 1.8V in increments of 50mV. Output voltage is limited to 1.8V maximum by an internal override of V_{O1} when V_{O2} = *high*. The input logic *low* threshold is less than 250mV referenced to GND and the logic *high* threshold is greater than V_{BIAS} – 250mV. The range between these two thresholds as set by a window comparator defines the logic *Hi-Z* state. See Table 1 in the Applications Information section that defines the V_{O2}, V_{O1} and V_{O0} settings versus V_{OUT}.

BIAS (Pin 27): Bias Supply. This pin supplies current to the internal control circuitry and the output stage driving the pass transistor. The LT3070-1 requires a minimum 2.2µF bypass capacitor for stability and proper operation. To ensure proper operation, the BIAS voltage must satisfy the following conditions: 2.2V ≤ V_{BIAS} ≤ 3.6V and V_{BIAS} ≥ (1.25 • V_{OUT} + 1V). For V_{OUT} ≤ 0.95V, the minimum BIAS voltage is limited to 2.2V.

EN (Pin 28): Enable. This pin enables/disables the reference output and output power device. The internal reference and all support functions are active if V_{BIAS} is above its UVLO threshold. Pulling EN low disables the REF/BYP pin current and the output pass transistor, putting the LT3070-1 into a low power *nap* mode. The maximum rising EN threshold is ratioed to 0.56 % of V_{BIAS} and the minimum falling EN threshold is 0.36 % of V_{BIAS}. Drive the EN pin with either a digital logic port or an open-collector NPN or an open-drain NMOS terminated with a pull-up resistor to V_{BIAS}. The pull-up resistor must be less than 35k to meet the V_{IH} condition of the EN pin. If unused, connect EN to BIAS.

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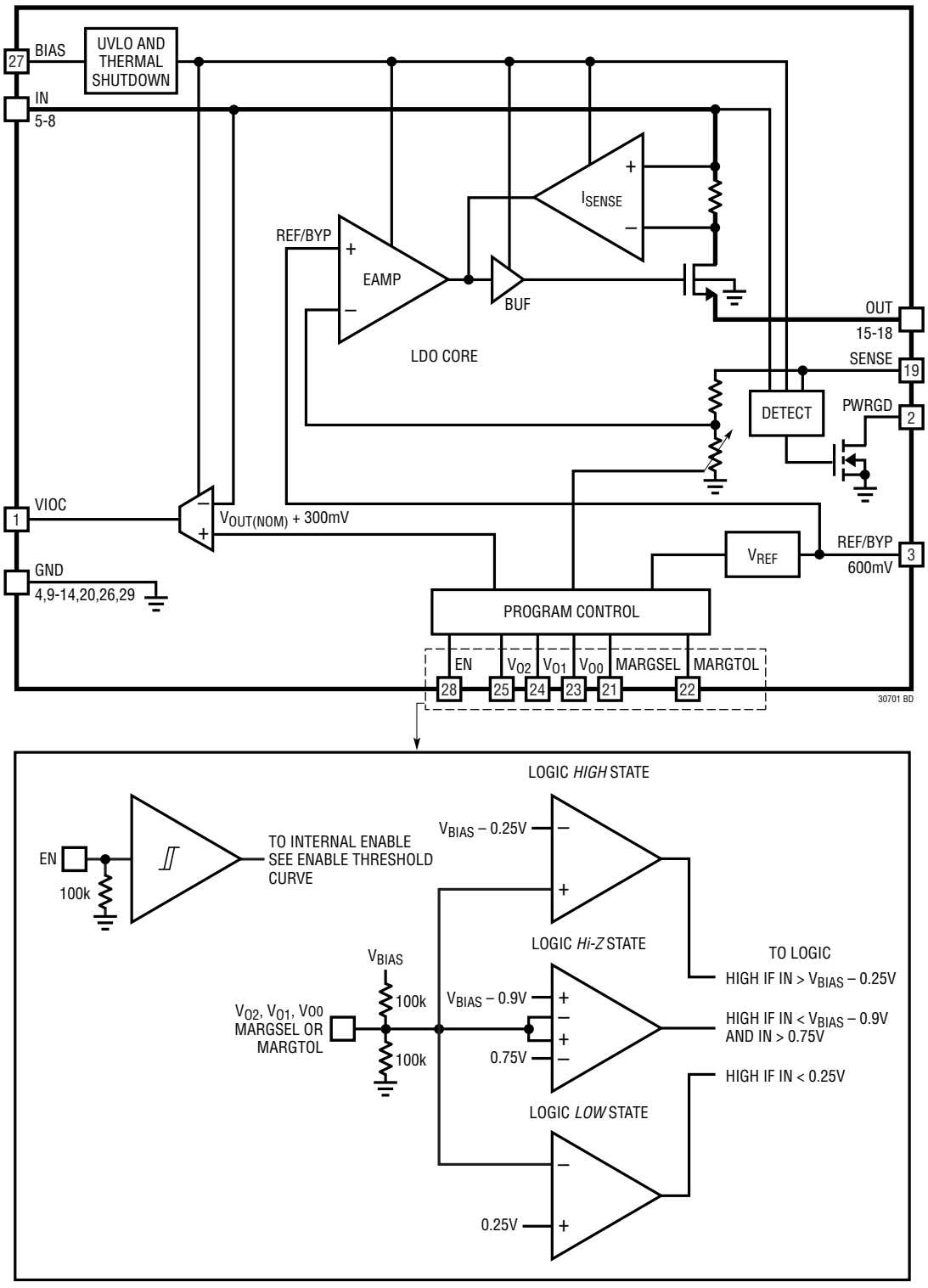
BLOCK DIAGRAM



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Introduction

Current generation FPGA and ASIC processors place stringent demands on the power supplies that power the core, I/O and transceiver channels. These microprocessors may cycle load current from near zero to amps in tens of nanoseconds. Output voltage specifications, especially in the 1V range, require tight tolerances including transient response as part of the requirement. Some ASIC processors require only a single output voltage from which the core and I/O circuitry operate. Some high performance FPGA processors require separate power supply voltages for the processor core, the I/O, and the transceivers. Often, these supply voltages must be low noise and high bandwidth to achieve the lowest bit-error rates. These requirements mandate the need for very accurate, low noise, high current, very high speed regulator circuits that operate at low input and output voltages.

The LT3070-1 is a low voltage, UltraFast transient response linear regulator. The device supplies up to 5A of output current with a typical dropout voltage of 85mV. A 0.01µF reference bypass capacitor decreases output voltage noise to 25µV_{RMS} (BW = 10Hz to 100kHz). The LT3070-1's high bandwidth provides UltraFast transient response using low ESR ceramic output capacitors (15µF minimum), saving bulk capacitance, PCB area and cost.

The LT3070-1's features permit *state-of-the-art* linear regulator performance. The LT3070-1 is ideal for high performance FPGAs, microprocessors, sensitive communication supplies, and high current logic applications that also operate over low input and output voltages.

Output voltage for the LT3070-1 is digitally selectable in 50mV increments over a 0.8V to 1.8V range. A margining function allows the user to adjust system output voltage in increments of ±1%, ±3% or ±5%.

The IC incorporates a unique tracking function, which if enabled by the user, controls an upsteam regulator powering the LT3070-1's input (see Figure 7). This tracking function drives the buck regulator to maintain the LT3070-1's input voltage to V_{OUT} + 300mV. This input-to-output voltage control allows the user to change the regulator output voltage, and have the switching regulator powering the LT3070-1's input to track to the optimum input voltage with no component changes.

This combines the efficiency of a switching regulator with superior linear regulator response. It also permits thermal management of the system even with a maximum 5A output load.

LT3070-1 internal protection includes input undervoltage lockout (UVLO), reverse-current protection, precision current limiting with power foldback and thermal shutdown. The LT3070-1 regulator is available in a thermally enhanced 28-lead, 4mm × 5mm QFN package.

The LT3070-1's architecture drives an internal N-channel power MOSFET as a source follower. This configuration permits a user to obtain an extremely low dropout, UltraFast transient response regulator with excellent high frequency PSRR performance. The LT3070-1 achieves superior regulator bandwidth and transient load performance by eliminating expensive bulk tantalum or electrolytic capacitors in the most modern and demanding microprocessor applications. Users realize significant cost savings as all additional bulk capacitance is removed. The additional savings of insertion cost, purchasing/inventory cost and board space are readily apparent. Precision incremental output voltage control accommodates legacy and future microprocessor power supply voltages.

Output capacitor networks simplify to direct parallel combinations of ceramic capacitors. Often, the high frequency ceramic decoupling capacitors required by these various FPGA and ASIC processors are sufficient to stabilize the system (see Stability and Output Capacitance section). This regulator design provides ample bandwidth and responds to transient load changes in a few hundred nanoseconds versus regulators that respond in many microseconds.

The LT3070-1 also incorporates precision current limiting, enable/disable control of output voltage and integrated overvoltage and thermal shutdown protection. The LT3070-1's unique design combines the benefits of low dropout voltage, high functional integration, precision performance and UltraFast transient response, as well as providing significant cost savings on the output capacitance needed in fast load transient applications.

As lower voltage applications become increasingly prevalent with higher frequency switching power supplies, the LT3070-1 offers superior regulation and an appreciable

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component cost savings. The LT3070-1 steps to the next level of performance for the latest generation FPGAs, DSPs and microprocessors. The simple versatility and benefits derived from these circuits exceed the power supply needs of today's high performance microprocessors.

Programming Output Voltage

Three tri-level input pins, V_{O2}, V_{O1} and V_{O0}, select the value of output voltage. Table 1 illustrates the 3-bit digital word to output voltage resulting from setting these pins *high*, *low* or allowing them to float.

These pins may be tied *high* or *low* by either pin-strapping them to V_{BIAS} or driving them with digital ports. Pins that float may either actually float or require logic that has *Hi-Z* output capability. This allows output voltage to be dynamically changed if necessary.

Output voltage is selectable from a minimum of 0.8V to a maximum of 1.8V in increments of 50mV. The MSB, V_{O2}, sets the *pedestal* voltage, and the LSB's, V_{O1} and V_{O0} increment V_{OUT}.

Output voltage is limited to 1.8V maximum by an internal override of V_{O1} (default to *low*) when V_{O2} = *high*.

Table 1. V_{O2} to V_{O0} Settings vs Output Voltage

V_{O2}	V_{O1}	V_{O0}	$V_{OUT(NOM)}$	V_{O2}	V_{O1}	V_{O0}	$V_{OUT(NOM)}$
0	0	0	0.80V	Z	0	1	1.35V
0	0	Z	0.85V	Z	Z	0	1.40V
0	0	1	0.90V	Z	Z	Z	1.45V
0	Z	0	0.95V	Z	Z	1	1.50V
0	Z	Z	1.00V	Z	1	0	1.55V
0	Z	1	1.05V	Z	1	Z	1.60V
0	1	0	1.10V	Z	1	1	1.65V
0	1	Z	1.15V	1	X	0	1.70V
0	1	1	1.20V	1	X	Z	1.75V
Z	0	0	1.25V	1	X	1	1.80V
Z	0	Z	1.30V				

X = Don't Care, 0 = Low, Z = Float, 1 = High

The input logic *low* threshold is less than 250mV referenced to GND and the logic *high* threshold is greater than V_{BIAS} – 250mV. The range between these two thresholds as set by a window comparator defines the logic *Hi-Z* state.

REF/BYP—Voltage Reference

This pin is the buffered output of the internal bandgap reference and has an output impedance of ≅19kΩ. The design includes an internal compensation pole at f_C = 4kHz. A 10nF REF/BYP capacitor to GND creates a low-pass pole at f_{LP} = 840Hz. The 10nF capacitor decreases reference voltage noise to about $10\mu V_{RMS}$ and soft-starts the reference. The LT3070-1 soft-starts the reference voltage when the EN pin is toggled from low to high. In comparison, the LT3070 soft-starts only when turning the BIAS supply voltage on. Output voltage noise is the RMS sum of the reference voltage noise in addition to the amplifier noise. Curves for start-up time and output noise vs REF/BYP capacitance appear in the Typical Performance Characteristics section.

The REF/BYP pin must not be DC loaded by anything except for applications that parallel other LT3070-1 regulators for higher output currents. Consult the Applications Section on Paralleling for further details.

Output Voltage Margining

Two tri-level input pins, MARGSEL (polarity) and MARGTOL (scale), select the polarity and amount of output voltage margining. Margining is programmable in increments of ±1%, ±3% and ±5%. Margining is internally implemented as a scaling of the reference voltage.

Table 2 illustrates the 2-bit digital word to output voltage margining resulting from setting these pins high, low or allowing them to float.

These pins may be set high or low by either pin-strapping them to V_{BIAS} or driving them with digital ports. Pins that float may either actually float or require logic that has "Hi-Z" output capability. This allows output voltage to be dynamically margined if necessary.

The MARGSEL pin determines both the polarity and the active state of the margining function. The logic *low* threshold is less than 250mV referenced to GND and enables negative voltage margining. The logic *high* threshold is greater than V_{BIAS} – 250mV and enables positive voltage margining. The voltage range between these two logic thresholds as set by a window comparator defines the logic *Hi-Z* state and disables the margining function.

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The MARGTOL pin selects the absolute value of margining (1%, 3% or 5%) if enabled by the MARGSEL input. The logic *low* threshold is less than 250mV referenced to GND and enables either ±1% change in V_{OUT} depending on the state of the MARGSEL pin. The logic *high* threshold is greater than V_{BIAS} – 250mV and enables either ±5% change in V_{OUT} depending on the state of the MARGSEL pin. The voltage range between these two logic thresholds as set by a window comparator defines the logic *Hi-Z* state and enables either ±3% change in V_{OUT} depending on the state of the MARGSEL pin.

Table 2. Programming Margining

MARGSEL	MARGTOL	% OF $V_{OUT(NOM)}$
0	0	–1
0	Z	–3
0	1	–5
Z	0	0
Z	Z	0
Z	1	0
1	0	1
1	Z	3
1	1	5

Enable Function—Turning On and Off

The EN pin enables/disables the reference output and output power device. The LT3070-1's support functions remain active if V_{BIAS} is above its UVLO threshold. Pulling the EN pin low puts the LT3070-1 into *nap* mode. In *nap* mode, the output is disabled and quiescent current decreases.

Drive the EN pin with either a digital logic port or an open-collector NPN or an open-drain NMOS terminated with a pull-up resistor to V_{BIAS}. The pull-up resistor must be less than 35k to meet the V_{IH} condition of the EN pin. If unused, connect EN to BIAS.

Input Undervoltage Lockout on BIAS Pin

An internal undervoltage lockout (UVLO) comparator monitors the BIAS supply voltage. If V_{BIAS} drops below the UVLO threshold, all functions shut down, the pass transistor is gated off and output current falls to zero. The typical BIAS pin UVLO threshold is 1.55V on the rising edge of V_{BIAS}. The UVLO circuit incorporates about 150mV of hysteresis on the falling edge of V_{BIAS}.

High Efficiency Linear Regulator—Input-to-Output Voltage Control

The VIOC (voltage input-to-output control) pin is a function to control a switching regulator and facilitate a design solution that maximizes system efficiency at high load currents and still provides low dropout voltage performance.

The VIOC pin is the output of an integrated transconductance amplifier that sources and sinks about 250µA of current. It typically regulates the output of most LTC® switching regulators or LTM® power modules, by sinking current from the ITH compensation node. The VIOC function controls a buck regulator powering the LT3070-1's input by maintaining the LT3070-1's input voltage to V_{OUT} + 300mV. This 300mV V_{IN}-V_{OUT} differential voltage is chosen to provide fast transient response and good high frequency PSRR while minimizing power dissipation and maximizing efficiency. For example, 1.5V to 1.2V conversion and 1.3V to 1V conversion yield 1.5W maximum power dissipation at 5A full output current.

Figure 2 depicts that the switcher's feedback resistor network sets the maximum switching regulator output voltage if the linear regulator is disabled. However, once the LT3070-1 is enabled, the VIOC feedback loop decreases the switching regulator output voltage back to V_{OUT} + 300mV.

Using the VIOC function creates a feedback loop between the LT3070-1 and the switching regulator. As such, the feedback loop must be frequency compensated for stability. Fortunately, the connection of VIOC to many ADI switching regulator ITH pins represents a high impedance characteristic which is the optimum circuit node to frequency compensate the feedback loop. Figure 2 illustrates the typical frequency compensation network used at the VIOC node to GND.

The VIOC amplifier characteristics are:

g_m = 3.2mS, I_{OUT} = ±250µA, BW = 10MHz.

If the VIOC function is not used, terminate the VIOC pin to GND with a small capacitor (1000pF) to prevent oscillations.

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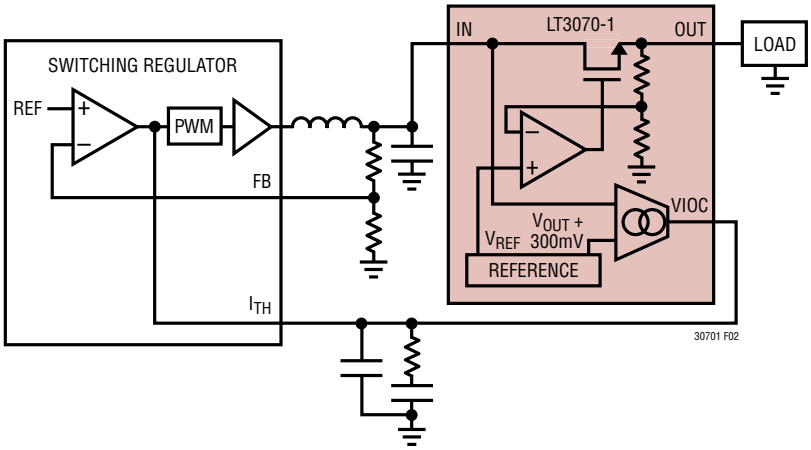

Figure 2. VIOC Control Block Diagram

PWRGD—Power Good

PWRGD pin is an open-drain NMOS digital output that actively pulls low if any one of these fault modes is detected:

- V_{OUT} is less than 90% of $V_{OUT(NOMINAL)}$ on the rising edge of V_{OUT}.
- V_{OUT} drops below 85% of $V_{OUT(NOMINAL)}$ for more than 25µs.
- V_{BIAS} is less than its undervoltage lockout threshold.
- The OUT-to-IN reverse-current detector activates.
- Junction temperature exceeds 145°C typically.*

  *The junction temperature detector is an early warning indicator that trips approximately 20°C before thermal shutdown engages.

Stability and Output Capacitance

The LT3070-1's feedback loop requires an output capacitor for stability. Choose C_{OUT} carefully and mount it in close proximity to the LT3070-1's OUT and GND pins. Include wide routing planes for OUT and GND to minimize inductance. If possible, mount the regulator immediately adjacent to the application load to minimize distributed inductance for optimal load transient performance. Point-of-Load applications present the best case layout scenario for extracting full LT3070-1 performance.

Low ESR, X5R or X7R ceramic chip capacitors are the ADI recommended choice for stabilizing the LT3070-1. Additional bulk capacitors distributed beyond the immediate decoupling capacitors are acceptable as their parasitic ESL and ESR, combined with the distributed PCB inductance isolates them from the primary compensation pole provided by the local surface mount ceramic capacitors.

The LT3070-1 requires a minimum output capacitance of 15µF for stability. ADI strongly recommends that the output capacitor network consist of several low value ceramic capacitors in parallel.

Why Do Multiple, Small-Value Output Capacitors Connected in Parallel Work Better?

The LT3070-1's unity-gain bandwidth with C_{OUT} of 15µF is about 1MHz at its full-load current of 5A. Surface mounted MLCC capacitors have a self-resonance frequency of $f_R = 1/(2\pi\sqrt{LC})$, which must be pushed to a frequency higher than the regulator bandwidth. Standard MLCC capacitors are acceptable. To keep the resonant frequency greater than 1MHz, the product $1/(2\pi\sqrt{LC})$ must be greater than 1MHz. At this bandwidth, PCB vias can add significant inductance, thus the fundamental decoupling capacitors must be mounted on the same plane as the LT3070-1.

Typical 0603 or 0805 case-size capacitors have an ESL of ~800pH and PCB mounting can contribute up to ~200pH. Thus, it becomes necessary to reduce the parasitic inductance by using a parallel capacitor combination. A

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suitable methodology must control this paralleling as capacitors with the same self-resonant frequency, f_R, will form a tank circuit that can induce ringing of their own accord. Small amounts of ESR (5mΩ to 20mΩ) have some benefit in dampening the resonant loop, but higher ESRs degrade the capacitor response to transient load steps with rise/fall times less than 1µs. The most area efficient parallel capacitor combination is a graduated 4/2/1 scale of f_R of the same case size. Under these conditions, the individual ESLs are relatively uniform, and the resonance peaks are deconstructively spread beyond the regulator bandwidth. The recommended parallel combination that approximates 15µF is 10µF + 4.7µF + 2.2µF. Capacitors with case sizes larger than 0805 have higher ESL and lower ESR (<5mΩ). Therefore, more capacitors with smaller values (<10µF) must be chosen. Users should consider new generation, low inductance capacitors to push out f_R and maximize stability. Refer to the surface mount ceramic capacitor manufacturer's data sheets for capacitor specifications. Figure 3 illustrates an optimum PCB layout for the parallel output capacitor combination, but also illustrates the GND connection between the IN capacitor and the OUT capacitors to minimize the AC GND loop for fast load transients. This tight bypassing connection minimizes EMI and optimizes bypassing.

Many of the applications in which the LT3070-1 excels, such as FPGA, ASIC processor or DSP supplies, typically require a high frequency decoupling capacitor network for the device being powered. This network generally consists of many low value ceramic capacitors in parallel. In some applications, this total value of capacitance may be close to the LT3070-1's minimum 15µF capacitance requirement. This may reduce the required value of capacitance directly at the LT3070-1's output. Multiple low value capacitors in parallel present a favorable frequency characteristic that pushes many of the parasitic poles/zeroes beyond the LT3070-1's unity-gain crossover frequency. This technique illustrates the method that extracts the full bandwidth performance of the LT3070-1.

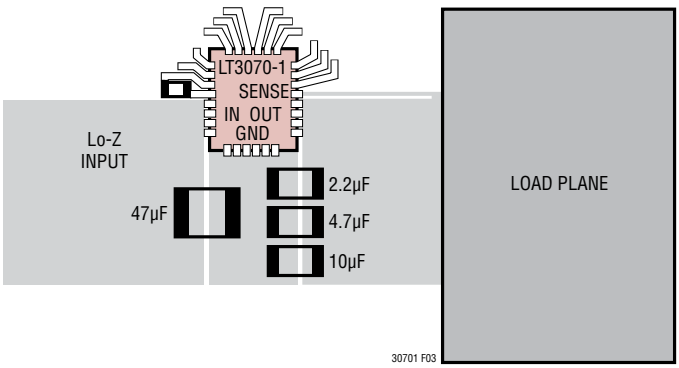

Figure 3. Example PCB Layout

Give additional consideration to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but they tend to have strong voltage and temperature coefficients as shown in Figure 4 and Figure 5. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied and over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified. Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric microphone works. For a ceramic capacitor the stress can be induced by vibrations in the system or thermal transients.

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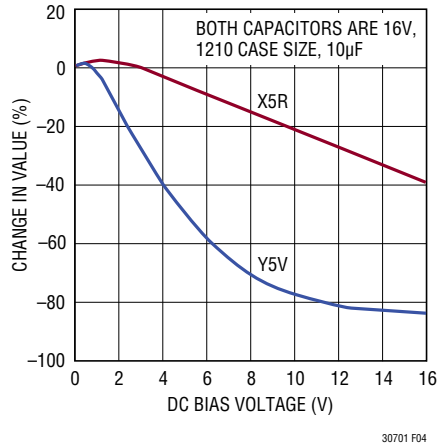

Figure 4. Ceramic Capacitor DC Bias Characteristics

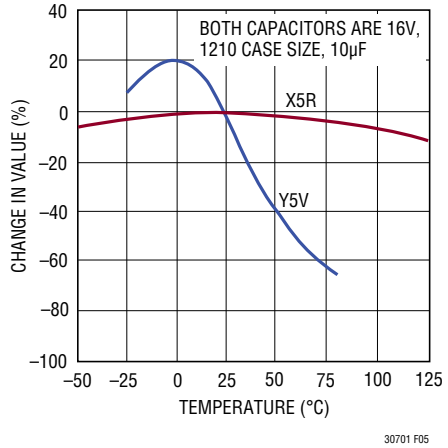

Figure 5. Ceramic Capacitor Temperature Characteristics

Stability and Input Capacitance

The LT3070-1 is stable with a minimum capacitance of 47µF connected to its IN pins. Use low ESR capacitors to minimize instantaneous voltage drops under large load transient conditions. Large V_{IN} droops during large load transients may cause the regulator to enter dropout with corresponding degradation in load transient response. Increased values of input and output capacitance may be necessary depending on an application's requirements. Sufficient input capacitance is critical as the circuit is intentionally operated close to dropout to minimize power. Ideally, the output impedance of the supply that powers IN should be less than 10mΩ to support a 5A load with large transients.

In cases where wire is used to connect a power supply to the input of the LT3070-1 (and also from the ground of the LT3070-1 back to the power supply ground), large input capacitors are required to avoid an unstable application.

This is due to the inductance of the wire forming an LC tank circuit with the input capacitor and not a result of the LT3070-1 being unstable. The self inductance, or isolated inductance, of a wire is directly proportional to its length. However, the diameter of a wire does not have a major influence on its self inductance. For example, one inch of 18-AWG, 0.04 inch diameter wire has 28nH of self inductance. The self inductance of a 2-AWG isolated wire with a diameter of 0.26 inch is about half the inductance of a 18-AWG wire. The overall self inductance of a wire can be reduced in two ways. One is to divide the current flowing towards the LT3070-1 between two parallel conductors which flows in the same direction in each. In this case, the farther the wires are placed apart from each other, the more inductance will be reduced, up to a 50% reduction when placed a few inches apart. Splitting the wires basically connects two equal inductors in parallel. However, when placed in close proximity from each other, mutual inductance is added to the overall self inductance of the wires. The most effective way to reduce overall inductance is to place the forward and return-current conductors (the wire for the input and the wire for the return ground) in very close proximity. Two 18-AWG wires separated by 0.05 inch reduce the overall self inductance to about one-fourth of a single isolated wire. If the LT3070-1 is powered by a battery mounted in close proximity with ground and power planes on the same circuit board, a 47µF input capacitor is sufficient for stability. However, if the LT3070-1 is powered by a distant supply, use a low ESR, large value input capacitor on the order of 330µF. As power supply output impedance varies, the minimum input capacitance needed for application stability also varies.

Bias Pin Capacitance Requirements

The BIAS pin supplies current to most of the internal control circuitry and the output stage driving the pass transistor. The LT3070-1 requires a minimum 2.2µF bypass capacitor for stability and proper operation. To ensure proper operation, the BIAS voltage must satisfy the following conditions: $2.2V \leq V_{BIAS} \leq 3.6V$ and $V_{BIAS} \geq (1.25 \bullet V_{OUT} + 1V)$. For $V_{OUT} \leq 0.95V$, the minimum BIAS voltage is limited to 2.2V.

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Load Regulation

The LT3070-1 provides a Kelvin sense pin for V_{OUT}, allowing the application to correct for parasitic package and PCB I-R drops. However, ADI recommends that the SENSE pin terminate in close proximity to the LT3070-1's OUT pins. This minimizes parasitic inductance and optimizes regulation. The LT3070-1 handles moderate levels of output line impedance, but excessive impedance between V_{OUT} and C_{OUT} causes excessive phase shift in the feedback loop and adversely affects stability.

Figure 1 in the Pin Functions section illustrates the Kelvin-Sense connection method that eliminates voltage drops due to PCB trace resistance. However, note that the voltage drop across the external PCB traces adds to the dropout voltage of the regulator. The SENSE pin input bias current depends on the selected output voltage. SENSE pin input current varies from 50µA typically at V_{OUT} = 0.8V to 300µA typically at V_{OUT} = 1.8V.

Short-Circuit and Overload Recovery

Like many IC power regulators, the LT3070-1 has safe operating area (SOA) protection. The safe area protection decreases current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage up to the absolute maximum voltage rating. V_{BIAS} must be above the UVLO threshold for any function. The LT3070-1 has a precision current limit specified at ±20% that is active if V_{BIAS} is above UVLO.

Under conditions of maximum I_{LOAD} and maximum V_{IN}-V_{OUT} the device's power dissipation peaks at about 3W. If ambient temperature is high enough, die junction temperature will exceed the 125°C maximum operating temperature. If this occurs, the LT3070-1 relies on two additional thermal safety features. At about 145°C, the PWRGD output pulls *low* providing an early warning of an impending thermal shutdown condition. At 165°C typically, the LT3070-1's thermal shutdown engages and the output is shut down until the IC temperature falls below the thermal hysteresis limit. The SOA protection decreases current limit as the IN-to-OUT voltage increases and keeps the power dissipation at safe levels for all values of input-to-output voltage. The LT3070-1 provides some output current at all values of input-to-output voltage up to the absolute maximum voltage rating. See the Current Limit vs V_{IN} curve in the Typical Performance Characteristics.

During start-up, after the BIAS voltage has cleared its UVLO threshold and V_{IN} is increasing, output voltage increases at the rate of current limit charging C_{OUT}.

With a high input voltage, a problem can occur where the removal of an output short will not allow the output voltage to recover. Other regulators with current limit foldback also exhibit this phenomenon, so it is not unique to the LT3070-1. The load line for such a load may intersect the output current curve at two points: normal operation and the SOA restricted load current settings. A common situation is immediately after the removal of a short circuit, but with a static load ≥ 1A. In this situation, removal of the load or reduction of I_{OUT} to <1A will clear this condition and allow V_{OUT} to return to normal regulation.

Reverse Voltage

The LT3070-1 incorporates a circuit that detects if V_{IN} decreases below V_{OUT}. This reverse-voltage detector has a typical threshold of about (V_{IN} – V_{OUT}) = –6mV. If the threshold is exceeded, this detector circuit turns off the drive to the internal NMOS pass transistor, thereby turning off the output. The output pulls low with the load current discharging the output capacitance. This circuit's intent is to limit and prevent back-feed current from OUT to IN if the input voltage collapses due to a fault or overload condition. It should be noted that a negative (–) reverse detection threshold implies that a small back-feed current can flow from V_{OUT} to V_{IN}, as long as the DUT is enabled. To guarantee shutdown the enable (EN) pin must be pulled low.

Thermal Considerations

The LT3070-1's maximum rated junction temperature of 125°C limits its power handling capability and is dominated by the output current multiplied by the input/output voltage differential:

$$I_{OUT} \bullet (V_{IN} - V_{OUT})$$

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The LT3070-1's internal power and thermal limiting circuitry protect it under overload conditions. For continuous normal load conditions, do not exceed the maximum junction temperature of 125°C. Give careful consideration to all sources of thermal resistance from junction to ambient. This includes junction to case, case-to-heat sink interface, heat sink resistance or circuit board to ambient as the application dictates. Also, consider additional heat sources mounted in proximity to the LT3070-1. The LT3070-1 is a surface mount device and as such, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Surface mount heat sinks and plated through-holes can also be used to spread the heat generated by power devices. Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly below the die. This is the lowest resistance path for heat flow. Proper mounting is required to ensure the best possible thermal flow from this area of the package to the heat sinking material. Note that the exposed pad is electrically connected to GND.

Table 3 lists thermal resistance as a function of copper area in a fixed board size. All measurements were taken in still air on a 4-layer FR-4 board with 1 oz solid internal planes and 2 oz top/bottom external trace planes with a total board thickness of 1.6mm. PCB layers, copper weight, board layout and thermal vias affect the resultant thermal resistance. For further information on thermal resistance and high thermal conductivity test boards, refer to JEDEC standard JESD51, notably JESD51-12 and JESD51-7. Achieving low thermal resistance necessitates attention to detail and careful PCB layout.

Table 3. UFD Plastic Package, 28-Lead QFN

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACK SIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	30°C/W
1000mm^2	2500mm^2	2500mm^2	32°C/W
225mm^2	2500mm^2	2500mm^2	33°C/W
100mm^2	2500mm^2	2500mm^2	35°C/W

*Device is mounted on topside

Calculating Junction Temperature

Example: Given an output voltage of 0.9V, an input voltage range of 1.2V ± 5%, a BIAS voltage of 2.5V, a maximum output current of 4A and a maximum ambient temperature of 50°C, what will the maximum junction temperature be?

The power dissipated by the device equals:

$$I_{OUT(MAX)} \bullet (V_{IN(MAX)} - V_{OUT}) + (I_{BIAS} - I_{GND}) \bullet V_{OUT} + I_{GND} \bullet V_{BIAS}$$

where:

$I_{OUT(MAX)} = 4A$

$V_{IN(MAX)} = 1.26V$

I_{BIAS} at ($I_{OUT} = 4A$, $V_{BIAS} = 2.5V$) = 6.91mA

I_{GND} at ($I_{OUT} = 4A$, $V_{BIAS} = 2.5V$) = 0.87mA

thus:

$$P = 4A(1.26V - 0.9V) + (6.91mA - 0.87mA)0.9V + 0.87mA(2.5V) = 1.448W$$

With the QFN package soldered to maximum copper area, the thermal resistance is 30°C/W. So the junction temperature rise above ambient equals:

1.448W at 30°C/W = 43.44°C

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient or:

T_{JMAX} = 50°C + 43.44°C = 93.44°C

Applications that cannot support extensive PCB space for heat sinking the LT3070-1 require a derating of output current or increased airflow.

Paralleling Devices for Higher I_{OUT}

Multiple LT3070-1s may be paralleled to obtain higher output current. This paralleling concept borrows from the scheme employed by the LT3080.

To accomplish this paralleling, tie the REF/BYP pins of the paralleled regulators together. This effectively gives an averaged value of multiple 600mV reference voltage sources. Tie the OUT pins of the paralleled regulators to

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APPLICATIONS INFORMATION

the common load plane through a small piece of PC trace ballast or an actual surface mount sense resistor beyond the primary output capacitors of each regulator. The required ballast is dependent upon the application output voltage and peak load current. The recommended ballast is that value which contributes 1% to load regulation. For example, two LT3070-1 regulators configured to output 1V, sharing a 10A load require 2mΩ of ballast at each output. The Kelvin SENSE pins connect to the regulator side of the ballast resistors to keep the individual control loops from conflicting with each other (see Figure 8 and Figure 9). Keep this ballast trace area free of solder to maintain a controlled resistance.

Table 4 shows a simple guideline for PCB trace resistance as a function of weight and trace width.

Table 4. PC Board Trace Resistance

WEIGHT (Oz)	100 MIL WIDTH*	200 MIL WIDTH*
1	5.43	2.71
2	2.71	1.36

*Trace resistance is measured in milliohms/in

Quieting the Noise

The LT3070-1 offers numerous noise performance advantages. Each LDO has several sources of noise. An LDO's most critical noise source is the reference, followed by the LDO error amplifier. Traditional low noise regulators buffer the voltage reference out to an external pin (usually through a large value resistor) to allow for bypassing and noise reduction of reference noise. The LT3070-1 deviates from the traditional voltage reference by generating a low voltage V_{REF} from a reference current into an internal resistor ≅19k. This intermediate impedance node (REF/BYP) facilitates external filtering directly. A 10nF filter capacitor minimizes reference noise to 10μV_{RMS} at the 600mV REF/BYP pin, equivalently a 17μV contribution to output noise at V_{OUT} = 1V. See the Typical Performance Characteristics for Noise vs Output Voltage performance as a function of $C_{REF/BYP}$.

This approach also accommodates reference sharing between LT3070-1 regulators that are hooked up in current sharing applications. The REF/BYP filter capacitor delays the initial power-up time by a factor of the RC time constant. V_{REF} is disabled in *nap* mode, thus start-up time is well controlled coming out of *nap* mode (EN:LO↑HI), soft-starting the output.

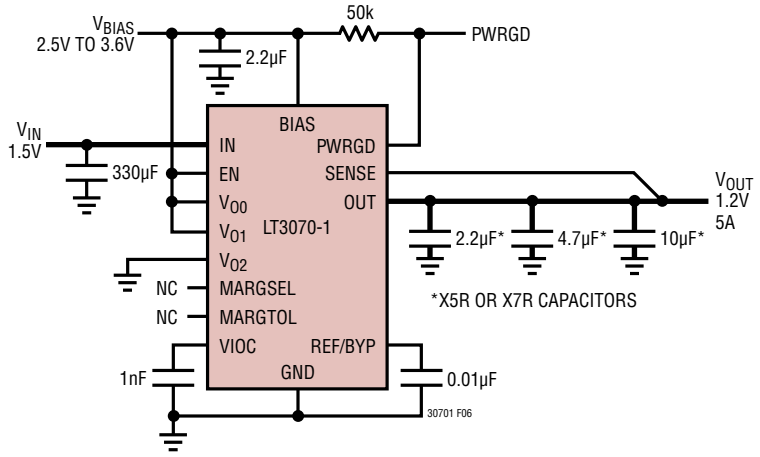

Figure 6. 1.5V to 1.2V Linear Regulator

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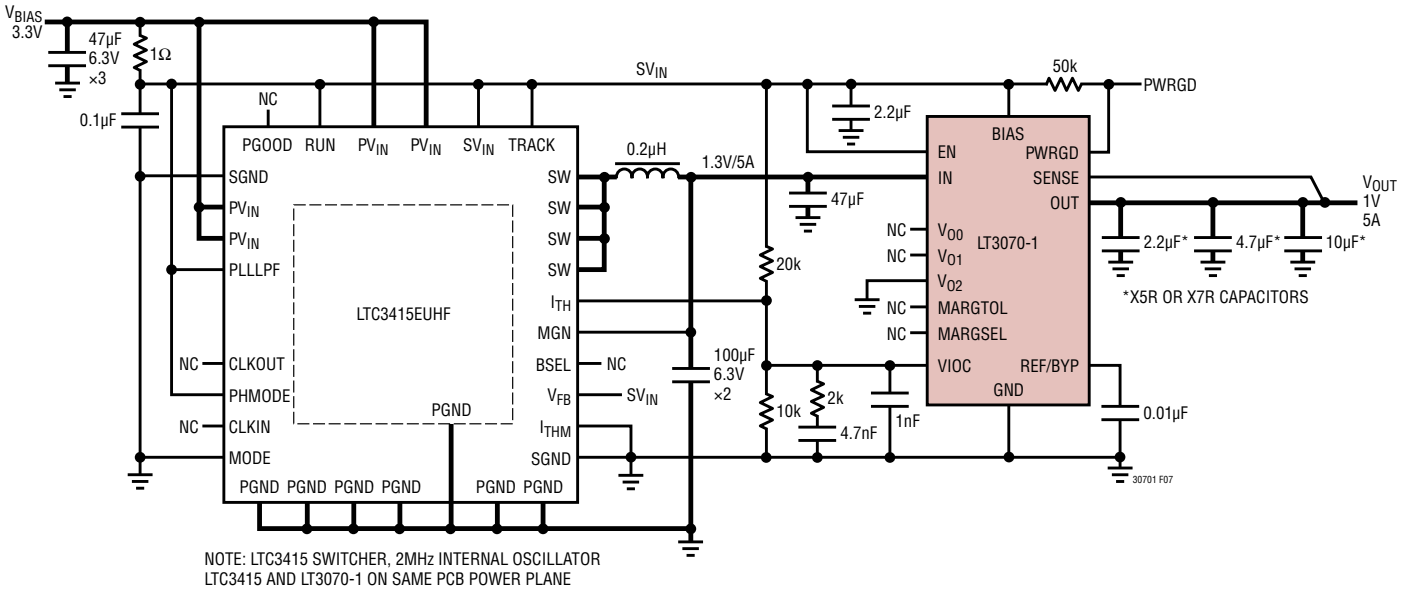

Figure 7. Regulator with VIOC Buck Control

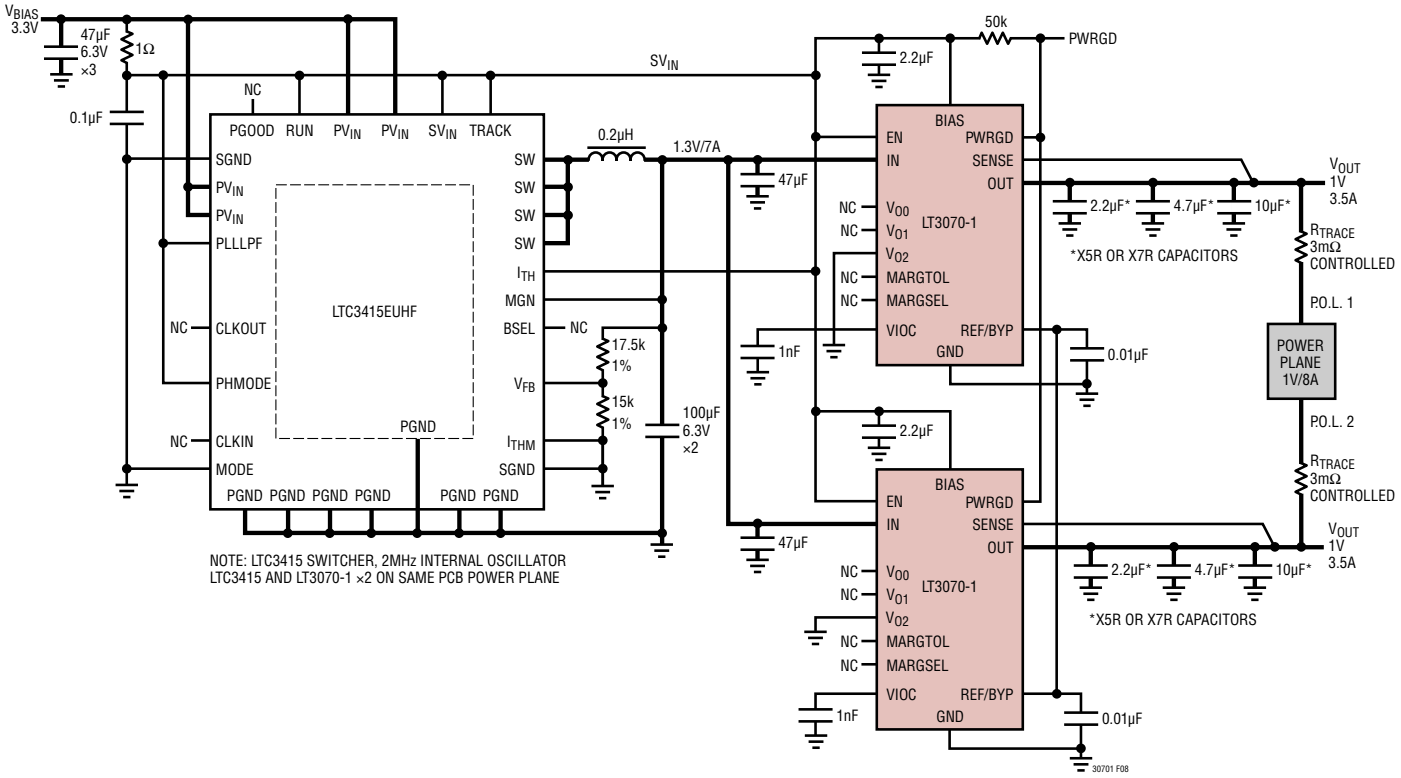

Figure 8. 1V, 7A Point-of-Load Current Sharing Regulators

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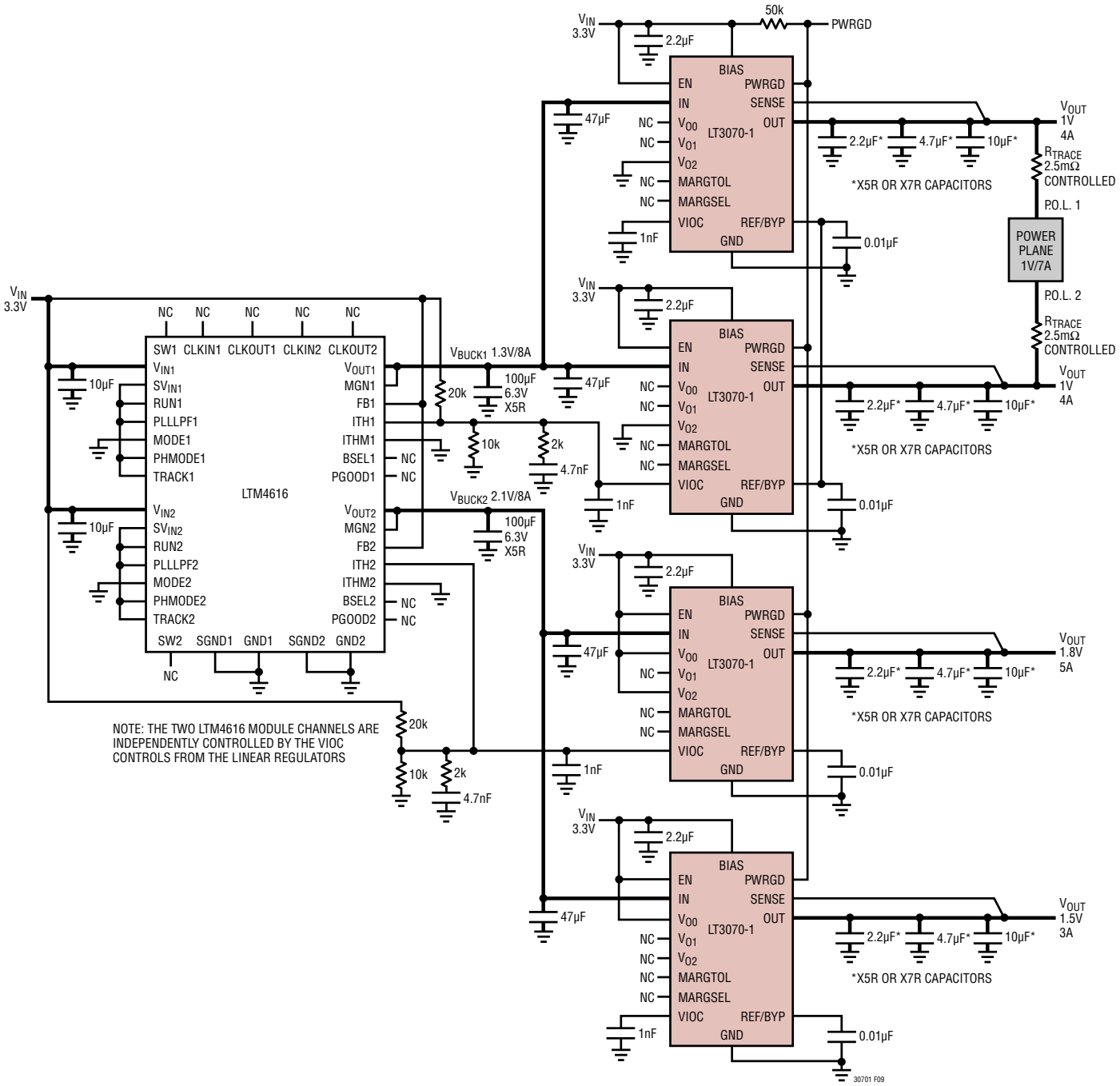

Figure 9. Triple Output Supply Providing 1V, 8A and 1.8V, 5A and 1.5V, 3A

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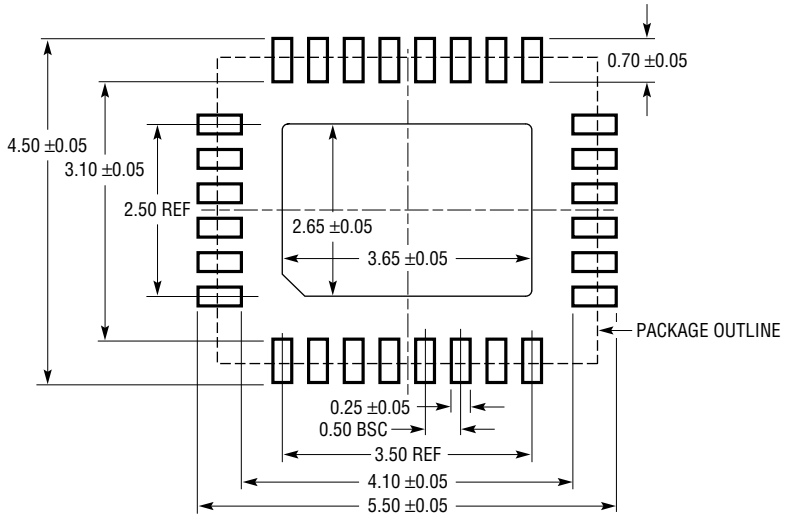
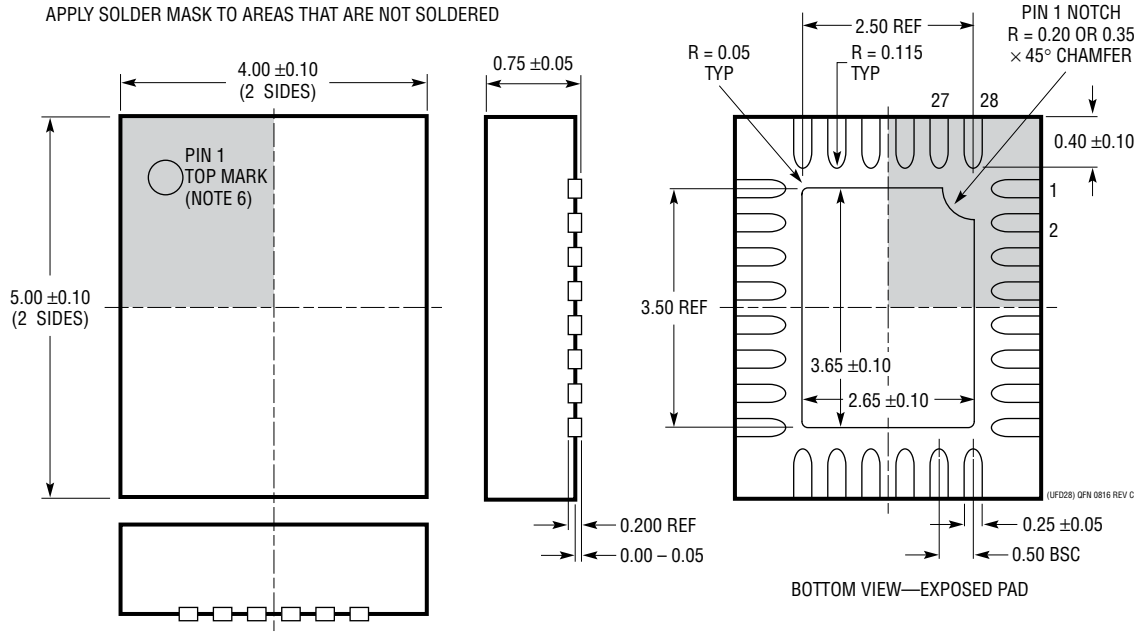
PACKAGE DESCRIPTION

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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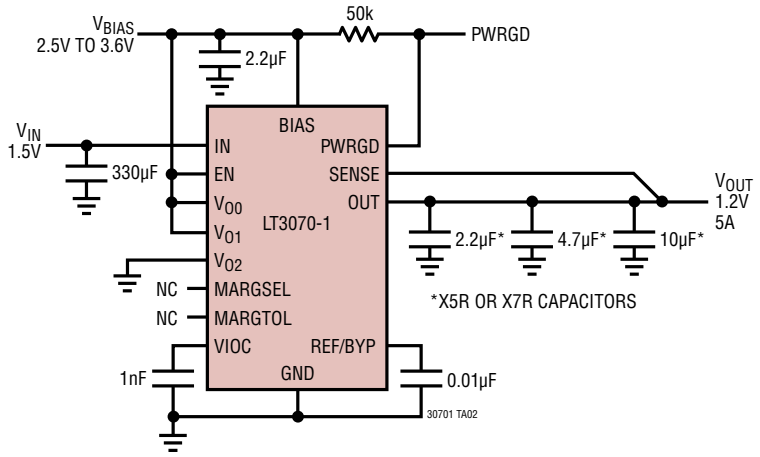
TYPICAL APPLICATION



1.5V to 1.2V Linear Regulator

RELATED PARTS

PART	DESCRIPTION	COMMENTS
LT1763	500mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN}: 1.8V to 20V, SO-8 Package
LT1764/LT1764A	3A, Fast Transient Response, Low Noise LDO	340mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN}: 2.7V to 20V, TO-220 and DD Packages "A" Version Stable Also with Ceramic Caps
LT1963/LT1963A	1.5A Low Noise, Fast Transient Response LDO	340mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN}: 2.5V to 20V, "A" Version Stable with Ceramic Caps, TO-220, DD, SOT-223 and SO-8 Packages
LT1965	1.1A, Low Noise, Low Dropout Linear Regulator	290mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN}: 1.8V to 20V, V_{OUT}: 1.2V to 19.5V, Stable with Ceramic Caps, TO-220, DD-Pak, MSOP and 3mm × 3mm DFN Packages
LT3021	500mA, Low Voltage, VLDO™ Linear Regulator	V_{IN}: 0.9V to 10V, Dropout Voltage = 160mV (Typ), Adjustable Output (V_{REF} = $V_{OUT(MIN)}$ = 200mV), Fixed Output Voltages: 1.2V, 1.5V, 1.8V, Stable with Low ESR, Ceramic Output Capacitors 16-Pin DFN (5mm × 5mm) and 8-Lead SO Packages
LT3080/LT3080-1	1.1A, Parallelable, Low Noise, Low Dropout Linear Regulator	300mV Dropout Voltage (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1 Resistor V_{OUT} Set; Directly Parallelable (No Op Amp Required), Stable with Ceramic Caps, TO-220, SOT-223, MSOP-8 and 3mm × 3mm DFN-8 Packages; LT3080-1 has Integrated Internal Ballast Resistor
LT3085	500mA, Parallelable, Low Noise, Low Dropout Linear Regulator	275mV Dropout Voltage (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1 Resistor V_{OUT} Set; Directly Parallelable (No Op Amp Required), Stable with Ceramic Caps, MSOP-8 and 2mm × 3mm DFN-6 Packages
LTC3025-1/ LTC3025-2	500mA Micropower VLDO Linear Regulator in 2mm × 2mm DFN	V_{IN} = 0.9V to 5.5V, Dropout Voltage: 75mV, Low Noise 80µV_{RMS}, Low I_Q: 54µA, Fixed Output: 1.2V (LTC3025-2); Adjustable Output Range: 0.4V to 3.6V (LTC3025-1) 2mm × 2mm 6-Lead DFN Package
LTC3026	1.5A, Low Input Voltage VLDO Regulator	V_{IN}: 1.14V to 3.5V (Boost Enabled), 1.14V to 5.5V (with External 5V), V_{DO} = 0.1V, I_Q = 950µA, Stable with 10µF Ceramic Capacitors, 10-Lead MSOP and DFN-10 Packages
LT3071	5A, Low Noise, Programmable Output, 85mV Dropout Linear Regulator with Analog Margining	V_{IN}: 0.95V to 3V, V_{OUT}: 0.8V to 1.8V in 50mV Increments, Low Noise: 25µV_{RMS}, Stable with Ceramic Capacitors, 4mm × 5mm 28-Lead QFN Package

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