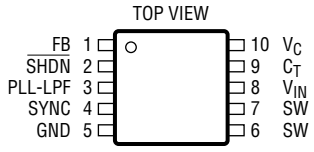
ABSOLUTE MAXIMUM RATINGS

(Note 1)

SW Voltage 36V
V_{IN} Voltage 18V
$\overline{SHDN}$ Voltage 18V
SYNC Voltage 5V
FB Voltage 5V
C_T Voltage 5V
V_C Voltage 2V
PLL-LPF Pin Current 1mA
Operating Temperature Range (Note 2) .. –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



MSE EXPOSED PAD PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 40°C/W

EXPOSED PAD IS GROUND
(MUST BE SOLDERED TO PCB)

ORDER PART NUMBER
LT1310EMSE
MSE PART MARKING
LTRZ

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V, $V_{\overline{SHDN}}$ = 3.3V, unless otherwise noted. (Note 2)

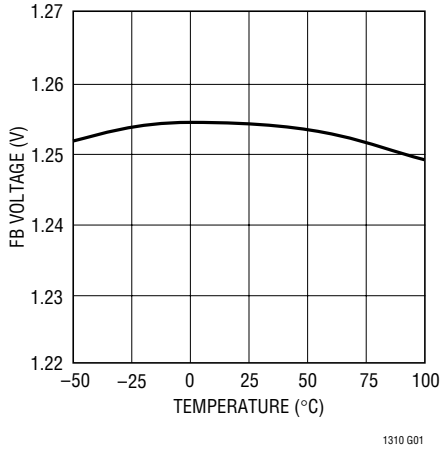
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Undervoltage Lockout					2.8	V
Maximum Input Voltage					18	V
Feedback Voltage		 ●	1.242 1.236	1.255	1.268 1.268	V V
FB Pin Bias Current				60	150	nA
Reference Line Regulation	V_{IN} = 2.9V to 18V			0.01	0.05	%/V
Error Amplifier Transconductance	ΔI = 5μA			350		μA/V
Error Amplifier Voltage Gain				200		V/V
SW Current Limit			1.5	2.1	2.8	A
SW Saturation Voltage	I_{SW} = 1A			0.240	0.320	V
SW Maximum Duty Cycle	C_T = 220pF C_T = 47pF		80 78	84 83		% %
SW Minimum On Time	I_{SW} = 150mA, V_C = 0.25V			70		ns
VCO Frequency	C_T = 220pF, PLL-LPF = High C_T = 220pF, PLL-LPF = High C_T = 220pF, PLL-LPF = Low C_T = 47pF, PLL-LPF = High	 ● 	0.950 0.800 	1.10 500 3.3	1.25 1.30 630 	MHz MHz kHz MHz
Frequency Foldback	C_T = 220pF, PLL-LPF = High, FB = 0V			200		kHz
PLL Lock Range	C_T = 220pF, Maximum C_T = 220pF, Minimum (Percent Change from Max)		0.950 –40	1.10 –50	1.25 	MHz %
Supply Current	$\overline{SHDN}$ = High $\overline{SHDN}$ = Low			11.5 	15 1	mA μA
SW Leakage Current	Switch Off, SW = 3.3V			0.1	5	μA
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 2.4V			35	65	μA
$\overline{SHDN}$ Pin High	Active Mode		2.4			V
$\overline{SHDN}$ Pin Low	Shutdown Mode				0.4	V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

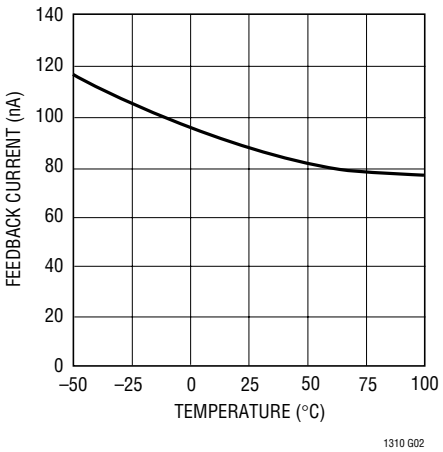
Note 2: The LT1310E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, chacterization and correlation with statistical process controls.

TYPICAL PERFORMANCE CHARACTERISTICS

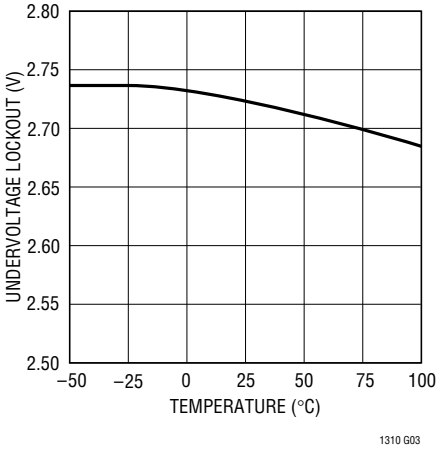
Feedback Voltage



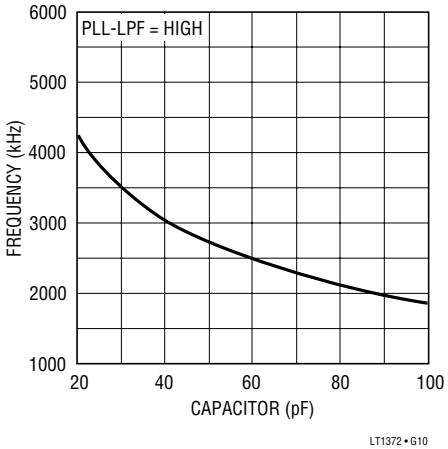
Feedback Pin Current



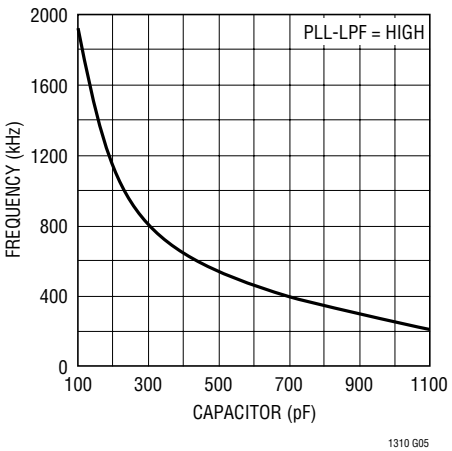
Undervoltage Lockout



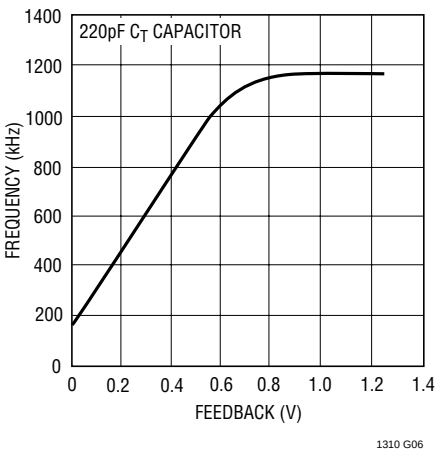
Oscillator Frequency vs C_T Capacitor



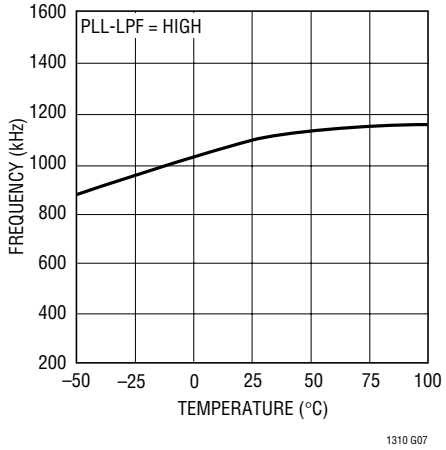
Oscillator Frequency vs C_T Capacitor



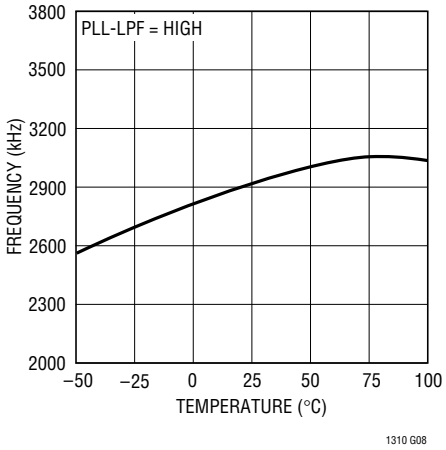
Oscillator Frequency vs Feedback Voltage



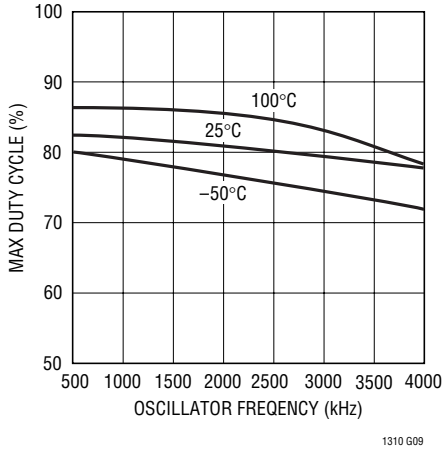
Oscillator Frequency 220pF Capacitor on C_T Pin



Oscillator Frequency 47pF Capacitor on C_T Pin

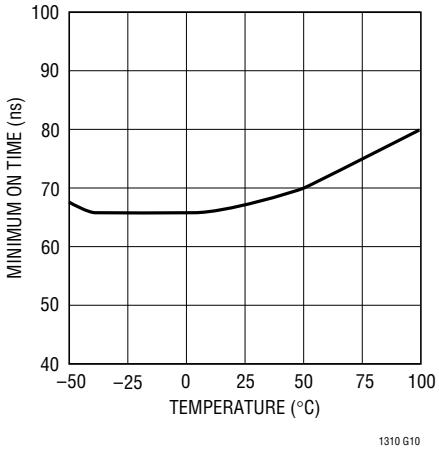


Maximum Duty Cycle vs Oscillator Frequency

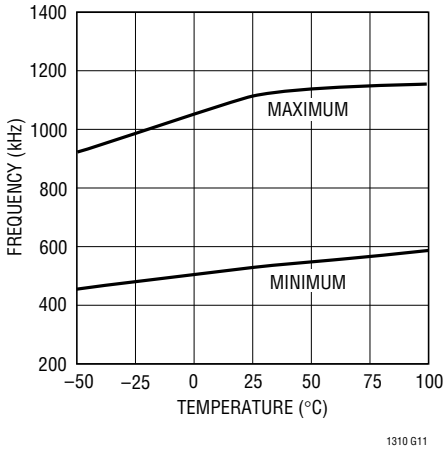


TYPICAL PERFORMANCE CHARACTERISTICS

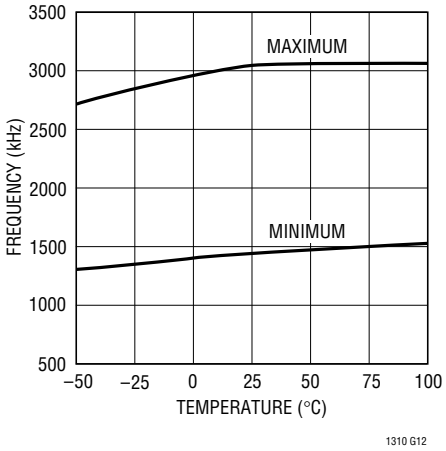
Switch Minimum On Time



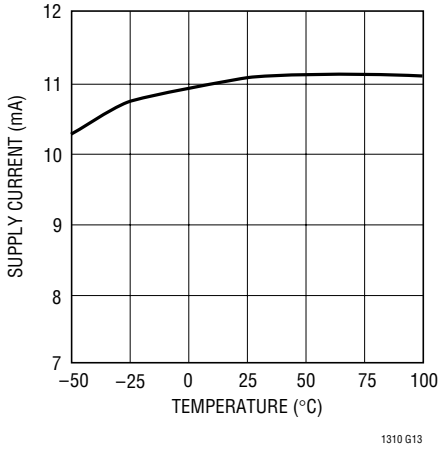
PLL Lock Range
220pF Capacitor on C_T Pin



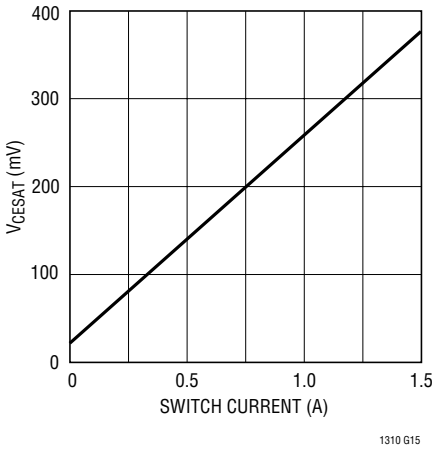
PLL Lock Range
47pF Capacitor on C_T Pin



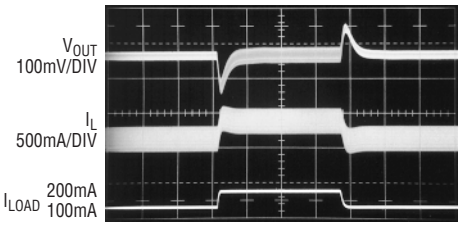
Supply Current



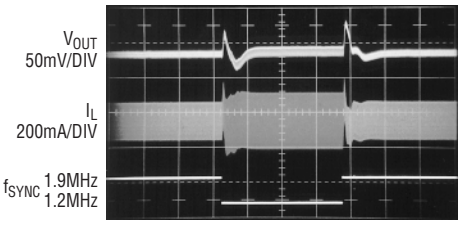
Switch V_{CESAT}



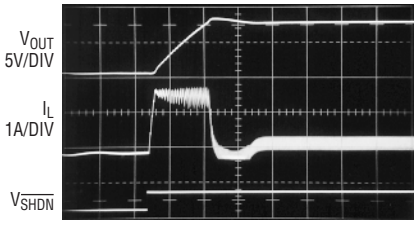
Transient Response



PLL Response



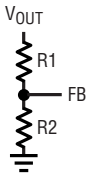
Start-Up Response



PIN FUNCTIONS

FB (Pin 1): Feedback Pin for Error Amplifier. Connect the resistor divider here to set output voltage according to the formula:

$$V_{OUT} = 1.255(1 + R1/R2)$$



Minimize trace area at this pin.

$\overline{\text{SHDN}}$ (Pin 2): Shutdown Pin. For active mode, tie this pin to a voltage between 2.4V and 18V. To disable the part and go into low current mode, pull this pin below 0.4V.

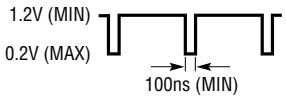
PLL-LPF (Pin 3): Phase Locked-Loop Filter Pin. This is the output of the phase detector and also the input to the voltage controlled oscillator (VCO). Connect an RC filter here. Typically, R = 3k and C = 1500pF. The voltage range at the PLL-LPF pin is approximately 0V to 1.5V with 1.5V corresponding to the maximum switching frequency. For applications not requiring synchronization, use a pull-up resistor at this pin; the pull-up voltage must be above 2.4V. Set the pull-up resistor value according to:

$$R_{PULLUP} = \frac{(V_{PULLUP} - 1.5V)}{300\mu A}$$

For a pull-up voltage of 5V:

$$R_{PULLUP} = \frac{(5V - 1.5V)}{300\mu A} \approx 11.6k$$

SYNC (Pin 4): Frequency Synchronization Pin. Inject the external synchronizing signal here. The phase detector is edge triggered and when locked the rising edge of the sync signal will be aligned with the turn-on of the power transistor. The SYNC signal must have a minimum HIGH amplitude of 1.2V and a maximum LOW amplitude of 0.2V with the signal staying low for at least 100ns.



GND (Pin 5, Exposed Pad): Ground. **Tie both Pin 5 and the exposed pad directly to local ground plane**. The ground metal to the exposed pad should be wide for better heat dissipation. Multiple vias (local ground plane ↔ ground backplane) placed close to the exposed pad can further aid in reducing thermal resistance. The exposed pad must be soldered to ground for the LT1310 to function properly.

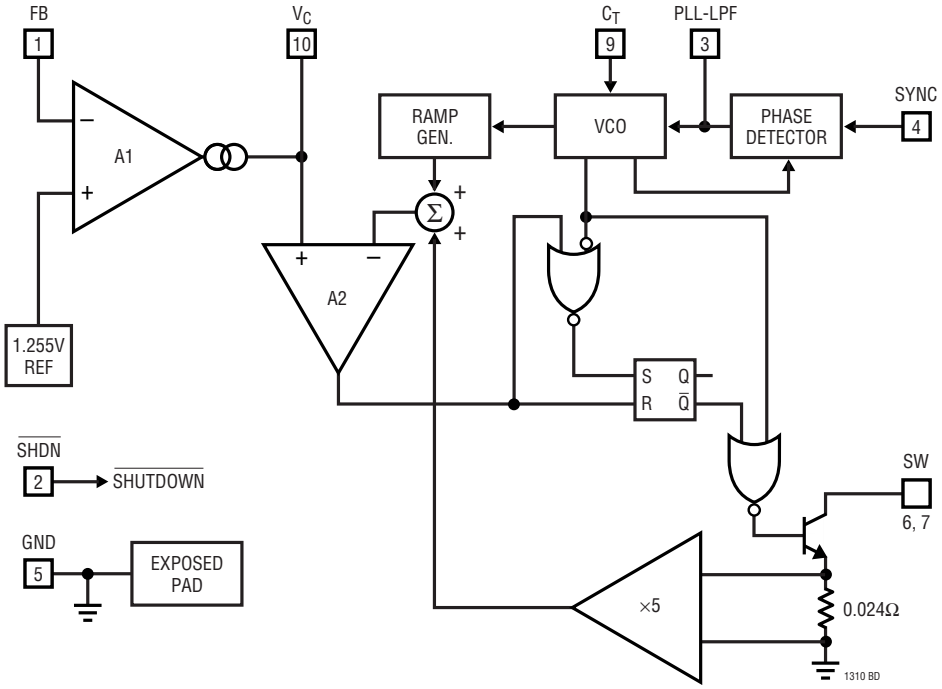
SW (Pins 6, 7): Switch Pin. **Must tie Pin 6 to Pin 7**. Connect inductor/diode here. Minimize trace area at this pin to keep EMI down.

V_{IN} (Pin 8): Supply Pin. Must be bypassed as close as possible to the pin.

C_T (Pin 9): Timing Capacitor Pin for VCO. Place the timing capacitor from this pin to ground to set the frequency range for the oscillator. Minimize trace at this pin to reduce stray capacitance.

V_C (Pin 10): Compensation Pin for Error Amplifier. Tie an RC network here to compensate the voltage feedback loop.

BLOCK DIAGRAM



OPERATION

To understand operation, refer to the Block Diagram. The LT1310 contains a boost switching regulator that can be phase locked to an external synchronizing signal. The boost regulator uses current mode control and contains a 1.5A NPN power transistor. This type of control uses two feedback loops. The main control loop sets output voltage and operates as follows: a load step causes V_{OUT} and the FB voltage to be slightly perturbed. The error amplifier A1 responds to this change in FB by driving the V_C pin either higher or lower. Because switch current is proportional to the V_C pin voltage, this change causes the switch current to be adjusted until V_{OUT} is once again satisfied. Loop compensation is taken care of by an RC network from the V_C pin to ground. Inside this main loop is another that sets current limit on a cycle-by-cycle basis. This loop utilizes current comparator A2 to control peak current. The oscillator issues a set pulse to the flip-flop at the beginning of each cycle, turning the switch on. With the switch now in the ON state, the SW pin is effectively connected to ground. Current ramps up in the inductor linearly at a rate of V_{IN}/L. Switch current is set by the V_C pin voltage and when the voltage across R_{SENSE} trips the current comparator, a reset pulse will be generated and the switch will be turned off. Since the inductor is now loaded up with current, the SW pin will fly high until it is clamped by the catch diode, D1. Current will flow through the diode decreasing at a rate of $(V_{OUT} – V_{IN})/L$ until the oscillator issues a new set pulse, causing the cycle to repeat.

The LT1310 is phase lockable up to 4.5MHz, giving the user precise control over switching frequency. The phase detector compares the incoming sync signal to the internal oscillator signal. If the switching frequency is lower than the sync signal, or if the phase lags the sync signal, then the phase detector output will source current into the PLL-LPF pin, driving it higher. The PLL-LPF pin is also the input to the voltage controlled oscillator. If the sync signal is slower than the switching frequency, the PLL-LPF pin will sink current until the PLL-LPF pin voltage drops. When locked, the PLL-LPF pin rests at a voltage between 0V and 1.5V. The PLL-LPF pin is capable of sinking or sourcing approximately 140μA.

OPERATION

C_T Selection for Operating Frequency

To synchronize to an external input signal, the timing capacitor and PLL filter components must be chosen properly. This is a simple process and can be done using the graph in Figure 2a.

In Figure 2a, operating frequency is plotted versus timing capacitor (C_T) with the upper and lower lines corresponding to the minimum and maximum lock frequency given a specific C_T value. To choose the right timing capacitor, find the intersection of the desired operating frequency and the dashed line. Then move to the corresponding C_T value.

Alternately, use the following equations as a starting point:

for $f_{LOCK} \geq 2MHz$:

$$C_T = 0.75\left(\frac{250 \bullet 10^{-6}}{f_{LOCK}} - 40 \bullet 10^{-12}\right)$$

for $f_{LOCK} \leq 2MHz$:

$$C_T = 0.75\left(\frac{310 \bullet 10^{-6}}{f_{LOCK}} - 60 \bullet 10^{-12}\right)$$

Because the lock range for the PLL is nearly 2:1, the nearest standard value NPO capacitor can be used. For the application shown in Figure 1, a 1.6MHz switching frequency corresponds to an 100pF timing capacitor. Since the switching frequency affects inductor ripple current, the inductor must also be scaled. Table 1 shows recommended component values for various switching frequencies.

Table 1. Recommended Component Values for Various Switching Frequencies (R_{LP} = 3.01k)

SWITCHING FREQUENCY	C_T	C_C	C_{LP}	R_C	L1
600kHz	330pF	1500pF	2700pF	10k	10µH
1MHz	180pF	1000pF	2200pF	10k	6.2µH
1.6MHz	100pF	820pF	1500pF	15k	5.6µH
2MHz	68pF	820pF	1500pF	15k	4.7µH
2.5MHz	47pF	330pF	1500pF	20k	3.3µH
3MHz	33pF	330pF	1000pF	20k	2.7µH

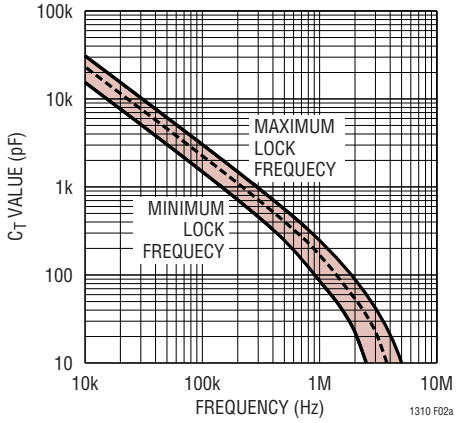


Figure 2a. C_T vs Operating Frequency

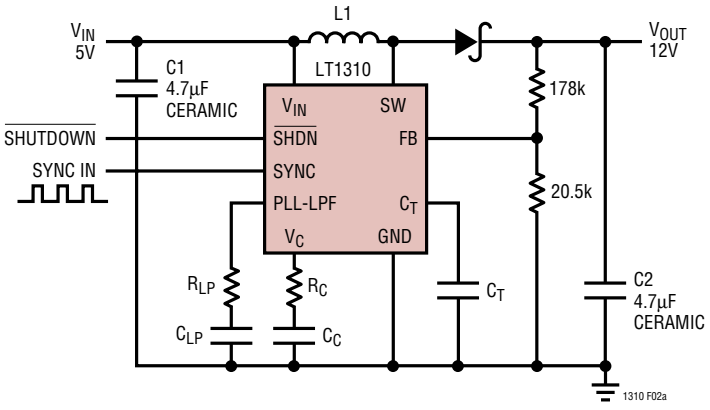


Figure 2b. Circuit Used for C_T Selection

APPLICATIONS INFORMATION

Inductor Selection

Several inductors that work well with the LT1310 are listed in Table 2. This table is not exclusive; there are many other manufacturers and inductors that can be used. Consult each manufacturer for more detailed information and for their entire selection of related parts, as many different sizes and shapes are available. Ferrite core inductors should be used to obtain the best efficiency, as core losses at high frequency are much lower for ferrite cores than for the cheaper powdered-iron ones. Choose an inductor that can handle at least 1.5A without saturating, and ensure that the inductor has a low DCR (copper wire resistance) to minimize I^2R power losses. Note that in some applications, the current handling requirements of the inductor can be lower, such as in the SEPIC topology where each inductor only carries one-half of the total switch current. Switching frequency will also affect inductor requirements with higher frequencies corresponding to lower inductance values. A good starting point is to set the inductor ripple current equal to one-third of the peak switch current.

The inductors shown in Table 2 were chosen for small size. For better efficiency, use similar valued inductors with a larger volume.

Table 2. Recommended Inductors

PART	L (µH)	MAX DCR (mΩ)	SIZE L × W × H (mm)	VENDOR
CDRH5D18-4R1	4.1	57	5.7 × 5.7 × 2	Sumida
CDRH5D18-5R4	5.4	76		(847) 956-0666
CDRH5D28-5R3	5.3	38	5.7 × 5.7 × 3	www.sumida.com
CDRH5D28-6R2	6.2	45		
CDRH5D28-8R2	8.2	53		
CR43-2R2	2.2	71	4.5 × 4 × 3.2	
CR43-3R3	3.3	86		
ELL6SH-4R7M	4.7	50	6.4 × 6 × 3	Panasonic
ELL6SH-5R6M	5.6	59		(408) 945-5660
ELL6SH-6R8M	6.8	62		www.panasonic.com
RLF5018T-4R7M1R4	4.7	45	5.6 × 5.2 × 1.8	TDK
RLF5018-1R5M2R1	1.5	25	5.2 × 5.6 × 1.8	(847) 803-6100
RLF5018-2R7M1R8	2.7	33		www.tdk.com
RLF5018-4R7M1R4	4.7	45		
RLF5018-100MR94	10	67		
LPO1704-122MC	1.2	80	5.5 × 6.6 × 1	Coilcraft
LPO1704-222MC	2.2	120		(800) 322-2645
				www.coilcraft.com

Capacitor Selection

Low ESR (equivalent series resistance) capacitors should be used at the output to minimize the output ripple voltage. Multilayer ceramic capacitors are an excellent choice, as they have an extremely low ESR and are available in very small packages. X5R dielectrics are preferred, followed by X7R, as these materials retain the capacitance over wide voltage and temperature ranges. A 4.7µF to 20µF output capacitor is sufficient for most applications, but systems with very low output currents may need only a 1µF or 2.2µF output capacitor. Solid tantalum or OS-CON capacitors can be used, but they will occupy more board area than a ceramic and will have a higher ESR. Always use a capacitor with a sufficient voltage rating.

Ceramic capacitors also make a good choice for the input decoupling capacitor, which should be placed as close as possible to the LT1310. A 2.2µF to 4.7µF input capacitor is sufficient for most applications. Table 3 shows a list of several ceramic capacitor manufacturers. Consult the manufacturers for detailed information on their entire selection of ceramic parts.

Table 3. Ceramic Capacitor Manufacturers

Taiyo Yuden	(408) 573-4150 www.t-yuden.com
AVX	(803) 448-9411 www.avxcorp.com
Murata	(714) 852-2001 www.murata.com

Compensation—Adjustment

To compensate the feedback loop of the LT1310, a series resistor-capacitor network should be connected from the V_C pin to GND. For most applications, a capacitor in the range of 220pF to 1500pF will suffice. With a switching frequency of 1.6MHz, a good starting value for the compensation capacitor, C_C, is 820pF. The compensation resistor, R_C, is usually in the range of 5k to 30k. A good technique to compensate a new application is to use a 30kΩ potentiometer in place of R_C, and use a 820pF capacitor for C_C. By adjusting the potentiometer while observing the transient response, the optimum value for R_C can be found. Figures 3a to 3c illustrate this process for the circuit of Figure 1 with a load current stepped from

APPLICATIONS INFORMATION

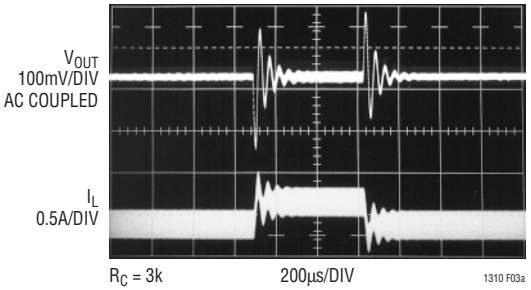


Figure 3a. Transient Response Shows Excessive Ringing

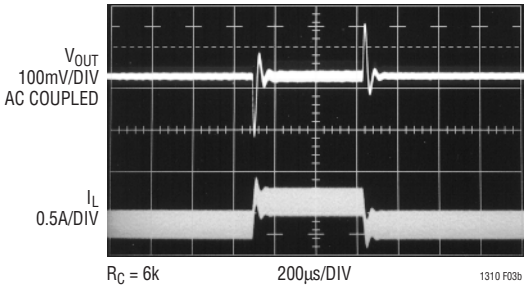


Figure 3b. Transient Response is Better

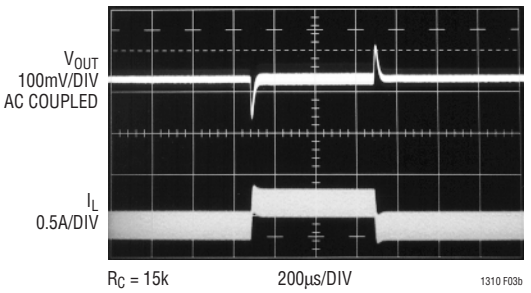


Figure 3c. Transient Response is Well Damped

100mA to 200mA. Figure 3a shows the transient response with R_C equal to 3k. The phase margin is poor as evidenced by the excessive ringing in the output voltage and inductor current. In Figure 3b, the value of R_C is increased to 6k, which results in a more damped response. Figure 3c shows the results when R_C is increased further to 15k. The transient response is nicely damped and the compensation procedure is complete.

Compensation—Theory

Like all other current mode switching regulators, the LT1310 needs to be compensated for stable and efficient operation. Two feedback loops are used in the LT1310: a fast current loop which does not require compensation, and a slower voltage loop which does. Standard Bode plot analysis can be used to understand and adjust the voltage feedback loop.

As with any feedback loop, identifying the gain and phase contribution of the various elements in the loop is critical. Figure 4 shows the key equivalent elements of a boost converter. Because of the fast current control loop, the power stage of the IC, inductor and diode have been replaced by the equivalent transconductance amplifier g_{mp}. g_{mp} acts as a current source where the output current is proportional to the V_C voltage. Note that the maximum output current of g_{mp} is finite due to the current limit in the IC.

From Figure 4, the DC gain, poles and zeroes can be calculated as follows:

$$\text{Output Pole: } P1 = \frac{2}{2 \bullet \pi \bullet R_L \bullet C_{OUT}}$$

$$\text{Error Amp Pole: } P2 = \frac{1}{2 \bullet \pi \bullet R_O \bullet C_C}$$

$$\text{Error Amp Zero: } Z1 = \frac{1}{2 \bullet \pi \bullet R_C \bullet C_C}$$

$$\text{DC Gain: } A = \frac{1.25}{V_{OUT}} \bullet g_{ma} \bullet R_O \bullet g_{mp} \bullet R_L$$

In addition to the elements from Figure 4, current mode control aslo results in some other poles and zeroes. These are as follows:

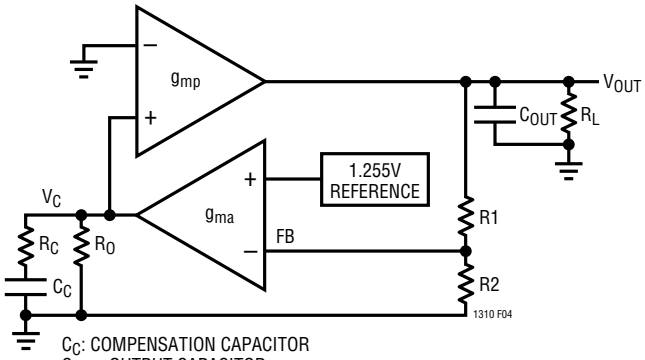
$$\text{RHP Zero: } Z2 = \frac{V_{IN}^2 \bullet R_L}{2 \bullet \pi \bullet V_{OUT}^2 \bullet L}$$

$$\text{Output Zero: } Z3 = \frac{1}{2 \bullet \pi \bullet ESR \bullet C_{OUT}}$$

$$\text{Current Mode Pole: } P3 > \frac{f_S}{3}$$

The Current Mode zero is a right half plane zero which can be an issue in feedback control design, but is manageable with proper external component selection.

APPLICATIONS INFORMATION



CC: COMPENSATION CAPACITOR
COUT: OUTPUT CAPACITOR
gma: TRANSCONDUCTANCE AMPLIFIER INSIDE IC
gmp: POWER STAGE TRANSCONDUCTANCE AMPLIFIER
RC: COMPENSATION RESISTOR
RL: OUTPUT RESISTANCE DEFINED AS V_{OUT} DIVIDED BY $I_{LOAD(MAX)}$
RO: OUTPUT RESISTANCE OF gma
R1, R2: FEEDBACK RESISTOR DIVIDER NETWORK

Figure 4. Boost Converter Equivalent Model

Using the circuit of Figure 1 as an example, the following table shows the parameters used to generate the Bode plot shown in Figure 5.

Table 4. Bode Plot Parameters

PARAMETER	VALUE	UNITS	COMMENT
R_L	30	Ω	Application Specific
C_{OUT}	4.7	µF	Application Specific
R_O	2	MΩ	Not Adjustable
C_C	820	pF	Adjustable
R_C	15	kΩ	Adjustable
V_{OUT}	12	V	Application Specific
V_{IN}	5	V	Application Specific
g_{ma}	500	µmho	Not Adjustable
g_{mp}	1.5	mho	Not Adjustable
L	5.6	µH	Application Specific
f_S	1.6	MHz	Adjustable
ESR	10	mΩ	Not Adjustable

From Figure 5, the phase is 120° when the gain reaches 0dB giving a phase margin of 60°. This is more than adequate. The crossover frequency is 50kHz, which is about three times lower than the frequency of the right half plane zero Z2. It is important that the crossover frequency be at least three times lower than the frequency of the RHP zero to achieve adequate phase margin.

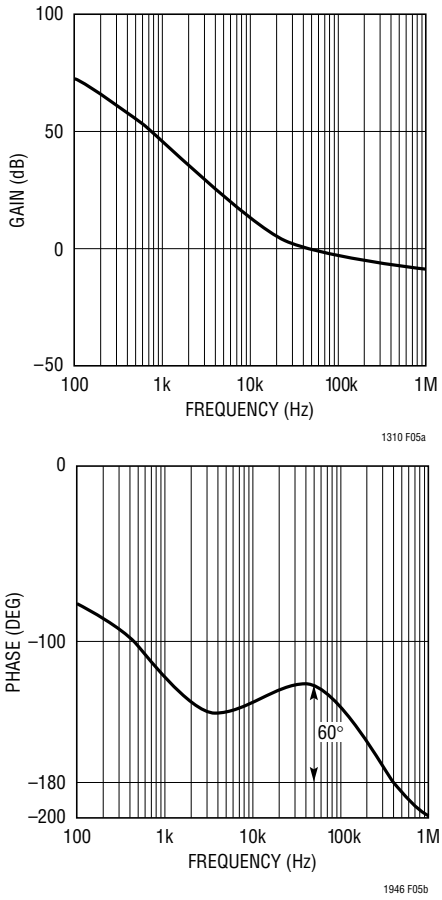


Figure 5. Bode Plot of Figure 1's Circuit

Diode Selection

A Schottky diode is recommended for use with the LT1310. The Microsemi UPS120 is a very good choice. Where the input to output voltage differential exceeds 20V, use the UPS140 (a 40V diode). These diodes are rated to handle an average forward current of 1A. For applications where the average forward current of the diode is less than 0.5A, an ON Semiconductor MBR0520 diode can be used.

Setting Output Voltage

To set the output voltage, select the values of R1 and R2 (see Figure 1) according to the following equation:

$$R1 = R2\left(\frac{V_{OUT}}{1.255V} - 1\right)$$

A good range for R2 is from 5k to 30k.

APPLICATIONS INFORMATION

Layout Hints

The high speed operation of the LT1310 demands careful attention to board layout. You will not get advertised performance with careless layout. Figure 6 shows the recommended component placement for a boost converter.

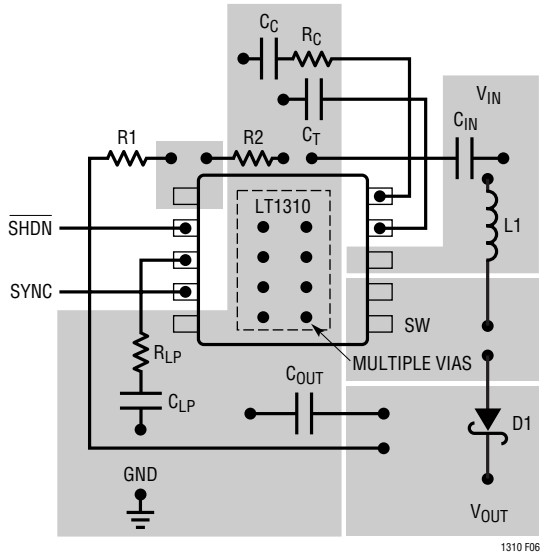
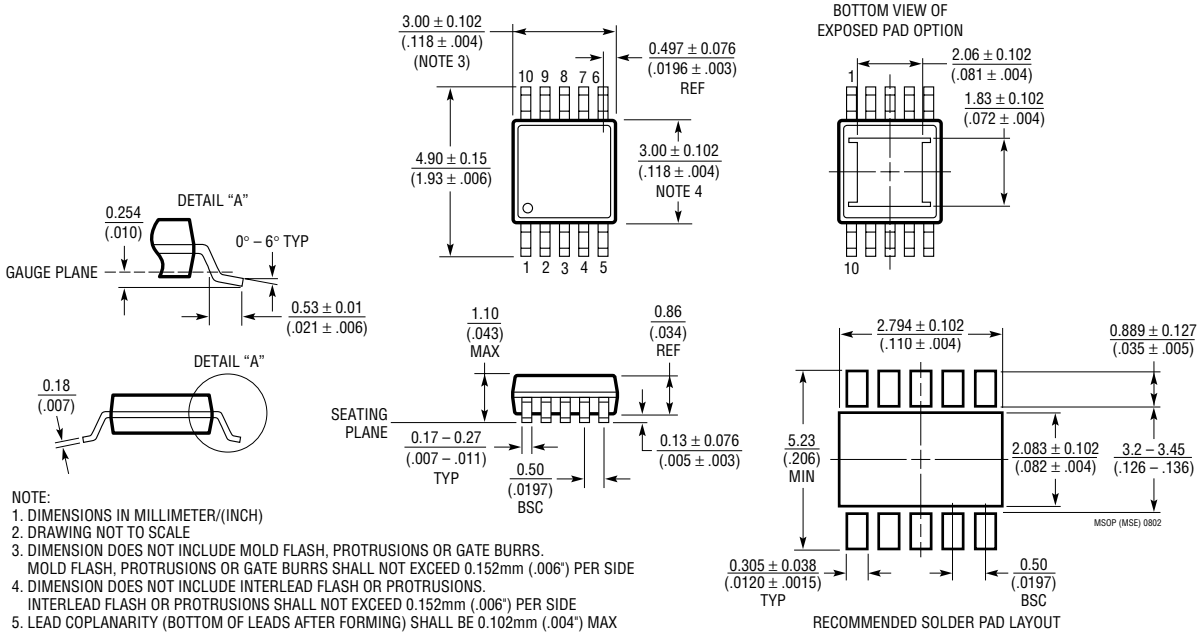


Figure 6. Recommended Component Placement for Boost Converter. Note Direct High Current Paths Using Wide PC Traces. Minimize Trace Area at Pin 10 (V_C), Pin 9 (C_T) and Pin 1 (FB). Use Multiple Vias to Tie Pin 5 Copper and the Exposed Pad to Ground Plane. Use Vias at One Location Only to Avoid Introducing Switching Currents Into the Ground Plane

PACKAGE DESCRIPTION

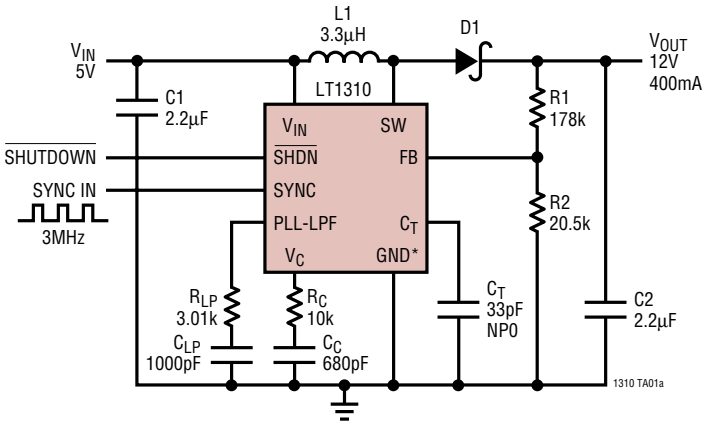
MSE Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1663)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

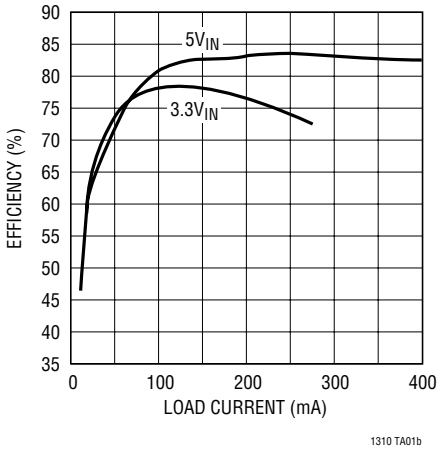
TYPICAL APPLICATION

3MHz 5V to 12V Converter



C1, C2: TAIYO YUDEN LMK212BJ225MG
D1: MOTOROLA MBRM120
L1: PANASONIC ELL6RH2R7M
*EXPOSED PAD MUST ALSO BE GROUNDED

Efficiency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1613	550mA (I_{SW}), 1.4MHz High Efficiency Step-Up DC/DC Converter	90% Efficiency, V_{IN}: 0.9V to 10V, $V_{OUT(MAX)}$: 34V, I_Q: 3mA, I_{SD}: <1µA, ThinSOT™ Package
LT1618	1.5A (I_{SW}), 1.25MHz, High Efficiency Step-Up DC/DC Converter	90% Efficiency, V_{IN}: 1.6V to 18V, $V_{OUT(MAX)}$: 35V, I_Q: 1.8mA, I_{SD}: <1µA, 10-Lead MS Package
LT1946/LT1946A	1.5A (I_{SW}), 1.2/2.7MHz, High Efficiency Step-Up DC/DC Converters	V_{IN}: 2.45V to 16V, $V_{OUT(MAX)}$: 34V, I_Q: 3.2mA, I_{SD}: <1µA, MS8 Package
LT1961	1.5A (I_{SW}), 1.25MHz, High Efficiency Step-Up DC/DC Converter	90% Efficiency, V_{IN}: 3V to 25V, $V_{OUT(MAX)}$: 35V, I_Q: 0.9mA, I_{SD}: 6µA, MS8E Package
LTC®3400/LTC3400B	600mA (I_{SW}), 1.2MHz, Synchronous Step-Up DC/DC Converters	92% Efficiency, V_{IN}: 0.85V to 5V, $V_{OUT(MAX)}$: 5V, I_Q: 19µA/300µA, I_{SD}: <1µA, ThinSOT Package
LTC3401	1A (I_{SW}), 3MHz, Synchronous Step-Up DC/DC Converter	97% Efficiency, V_{IN}: 0.5V to 5V, $V_{OUT(MAX)}$: 6V, I_Q: 38µA, I_{SD}: <1µA, 10-Lead MS Package
LTC3402	2A (I_{SW}), 3MHz, Synchronous Step-Up DC/DC Converter	97% Efficiency, V_{IN}: 0.5V to 5V, $V_{OUT(MAX)}$: 6V, I_Q: 38µA, I_{SD}: <1µA, 10-Lead MS Package

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Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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