- OPEN Alliance-compliant wake-up concept (global wake-up support)
  - Robust remote wake-up detection via bus lines
  - Wake-up forwarding on PHY level
- OPEN Alliance-compliant sleep concept
- Local wake-up pin
- Wake-up via SMI-access

2.4 Diagnosis

- Real-time monitoring of link stability and transmitted data quality
- Diagnosis of cable errors (shorts and opens)
- Gap-free supply undervoltage detection with fail-silent behavior
- Internal, external and remote loopback modes for diagnosis

2.5 Miscellaneous

- Reverse MII mode for back-to-back connection of two PHYs
- On-chip regulators to provide 3.3 V single-supply operation
- Supports optional 1.8 V external supply for digital core
- On-chip termination resistors for the differential cable pair
- Jumbo frame support up to 16 kB

3 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TJA1101AHN	HVQFN36	plastic thermal enhanced very thin quad flat package; no leads; 36 terminals; body 6 × 6 × 0.85 mm	SOT1092-2

4 Block diagram

A block diagram of the TJA1101 is shown in Figure 1. The 100BASE-T1 section contains the functional blocks specified in the 100BASE-T1 standard (see Ref.1) that make up the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) layer for both the transmit and receive signal paths. The MII/RMII interface (including the Serial Management Interface (SMI)) conforms to IEEE802.3 clause 22.

Additional blocks are defined for mode control, register configuration, interrupt control, system configuration, reset control, local wake-up, remote wake-up, undervoltage detection and configuration control. A number of power-supply-related functional blocks are defined: an internal 1.8 V regulator for the digital core, a Very Low Power (VLP) supply for Sleep mode, the reset circuit, supply monitoring and inhibit control.

The clock signals needed for the operation of the PHY are generated in the PLL block, derived from an external crystal or an oscillator input signal.

Pin strapping allows a number of default PHY settings (e.g. Master or Slave configuration) to be hardware-configured at power-up.

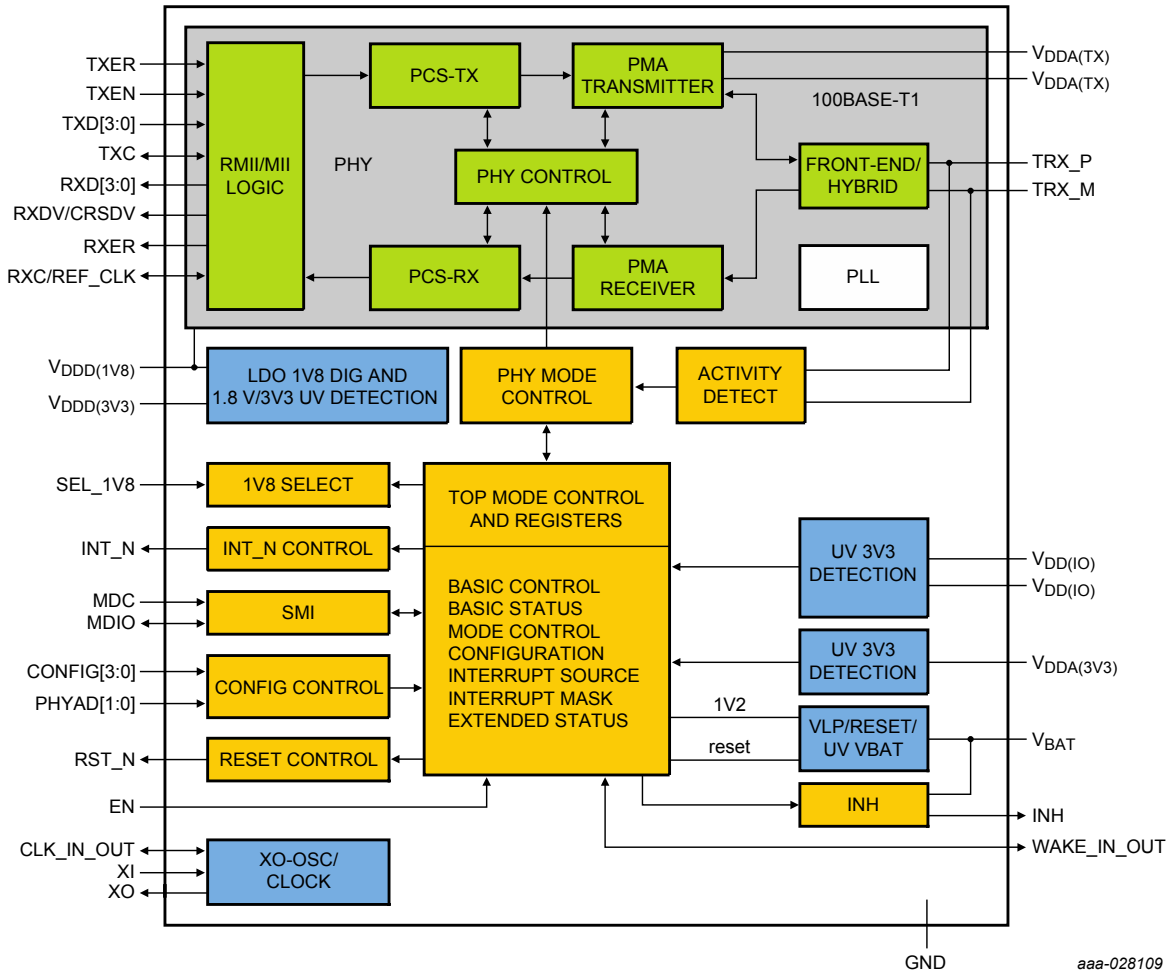


Figure 1. Block diagram

5 Functional description

5.1 System configuration

The TJA1101 contains a 100BASE-T1 compliant Ethernet PHY, with 100 Mbit/s transmit and receive capability over a single unshielded twisted-pair cable. It supports a cable length of at least 15 m, with a bit error rate of 1E-10 or less. It is optimized for capacitive signal coupling to the twisted-pair lines. A common-mode choke is typically inserted into the signal path to comply with automotive EMC requirements.

The TJA1101 is designed to provide a cost-optimized system solution for automotive Ethernet links. It communicates with the Media Access Control (MAC) unit via the MII or RMII interface.

The TJA1101 can operate with a crystal or an external clock. The clock can be forwarded to other PHYs (see Figure 2). The clocking and power supply schemes are independent of each other.

The TJA1101 can be powered via a single 3.3 V supply. An internal LDO generates the required 1.8 V supply, requiring only the addition of a decoupling capacitor.

When the TJA1101 is used in a switch application with several PHY ports, it may be more efficient to use an external SMPS to provide the 1.8 V supply. In this configuration, the internal LDO is switched off to allow an external supply to be used.

The state of SEL_1V8 is captured when the device is powered up, and used to enable and disable the internal 1.8 V LDO. If SEL_1V8 is LOW, the internal LDO is disabled and $V_{DDD(1V8)}$ must be supplied externally.

Control and status information is exchanged with the host controller via the SMI interface. The INH output can be used to switch off the external regulator when all ports are in Sleep mode.

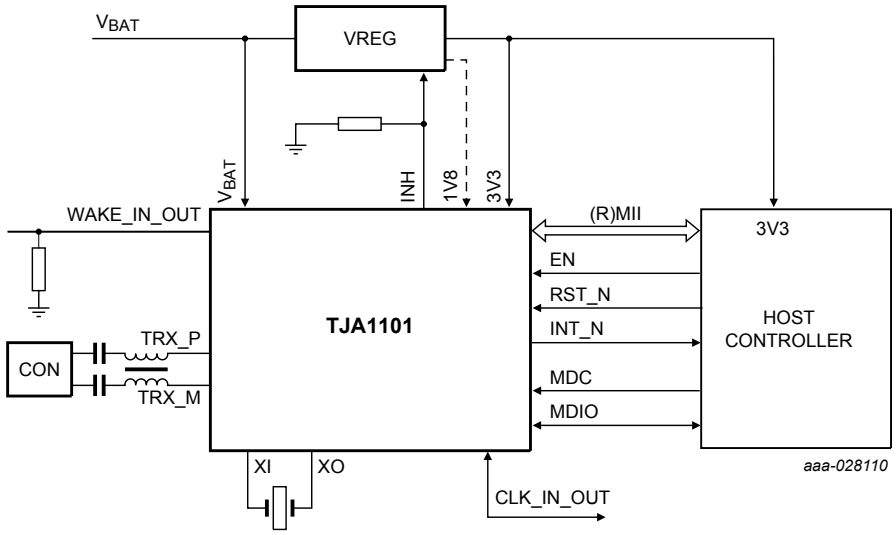


Figure 2. Typical TJA1101 switch application circuit

5.2 MII and RMII

The TJA1101 supports a number of MII modes that can be selected via pin strapping or the SMI. The following modes are supported:

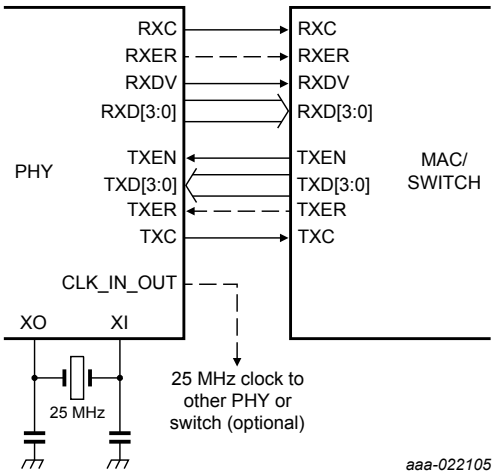
- MII
- RMII (25 MHz XTAL or external 50 MHz via REF_CLK)
- Reverse MII (connected externally)

The strength of the (R)MII output driver signals can be limited in all modes to optimize EMC.

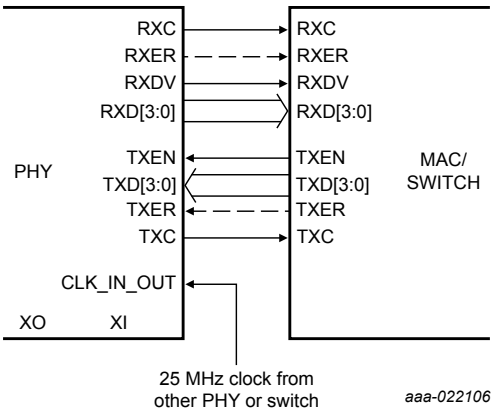
5.2.1 MII

The connections between the PHY and the MAC are shown in more detail in Figure 3. Data is exchanged via 4-bit wide data nibbles on TXD[3:0] and RXD[3:0]. Transmit and receive data is synchronized with the transmit (TXC) and receive (RXC) clocks. Both clock signals are provided by the PHY and are typically derived from an external clock or crystal running at a nominal frequency of 25 MHz (±100 ppm). Normal data transmission

is initiated with a HIGH level on TXEN, while a HIGH level on RXDV indicates normal data reception.



a. Using external XTAL showing optional 25 MHz clock output



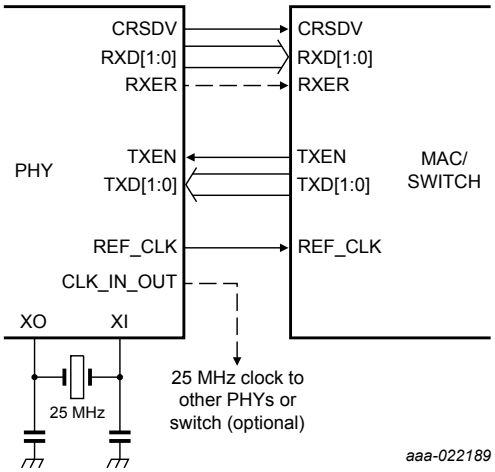
b. Using external reference clock

Figure 3. MII signaling

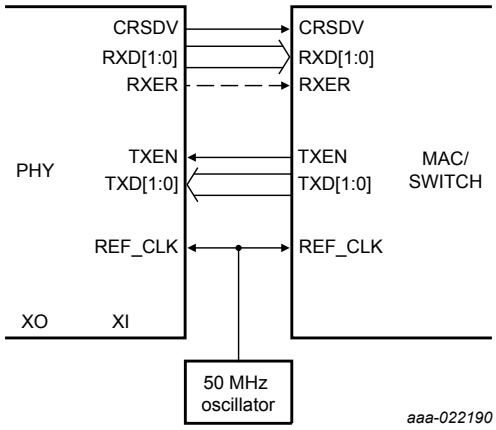
5.2.2 RMII

5.2.2.1 Signaling and encoding

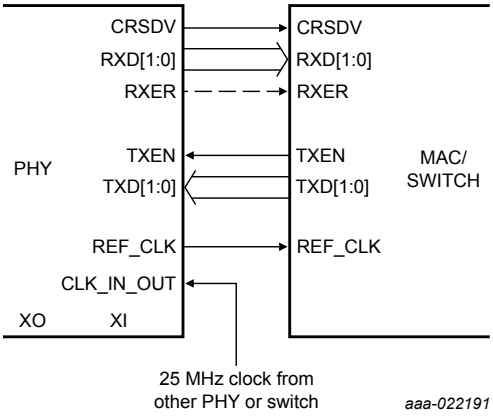
RMII data is exchanged via 2-bit wide data nibbles on TXD[1:0] and RXD[1:0], as illustrated in Figure 4. To achieve the same data rate as MII, the interface is clocked at a nominal frequency of 50 MHz. A single clock signal, REF_CLK, is provided for both transmitted and received data. This clock signal is provided by the PHY and is typically derived from an external 25 MHz (±100 ppm) crystal (see Figure 4 (a)). Alternatively, a 50 MHz clock signal (±50 ppm) generated by an external oscillator can be connected to pin REF_CLK (see Figure 4 (b)). A third option is to connect a 25 MHz (±100 ppm) clock signal generated by another PHY or switch to pin CLK_IN_OUT (see Figure 4 (c)).



a. Using external XTAL showing optional 25 MHz clock output



b. Using external reference clock



c. Using externally generated 25 MHz reference clock

Figure 4. RMII signaling

5.2.3 Reverse MII

In Reverse MII mode, two PHYs are connected back-to-back via the MII interface to realize a repeater function on the physical layer (see Figure 5). The MII signals are cross-connected: RX output signals from each PHY are connected to the TX inputs on the other PHY. For the PHY connected in Reverse MII mode, the TXC and RXC clock signals become inputs.

Since the MII interface is a standardized solution, two PHYs can be used to implement two different physical layers to realize, for example, a conversion from Fast Ethernet to 100BASE-T1 and vice versa. Another use case for such a repeater could be to double the link length up to 30 m.

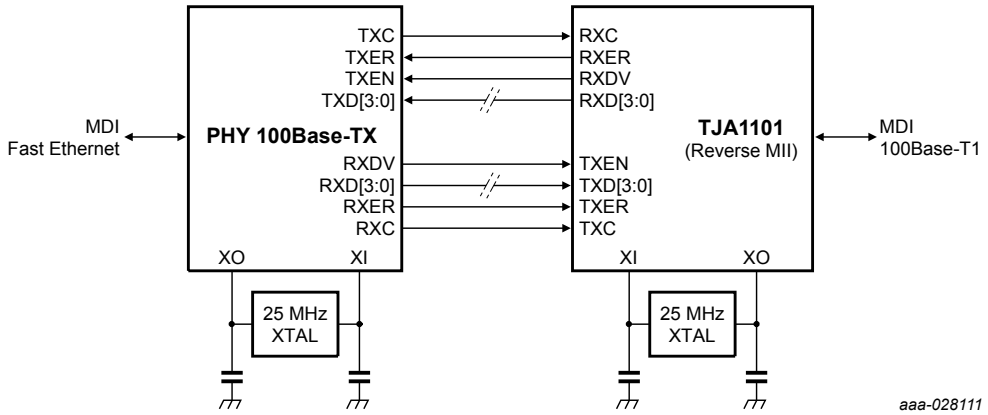


Figure 5. Fast Ethernet to 100BASE-T1 media converter with TJA1101 in Reverse MII

6 Application information

The MDI circuit for the TJA1101 is shown in Figure 6. The common mode termination depends on OEM requirements and might vary, depending on the application.

The common mode choke is expected to be compliant with the OPEN Alliance CMC specification. The 100 nF coupling capacitors should have a voltage range ≥ 50 V with 10 % (max) tolerance.

The TJA1101 provides an ESD robustness of ±6 kV according to IEC 61000-4-2 and HBM at the IC pins. With CMC and coupling capacitors, it is able to withstand ≥ ±8 kV for IEC 61000-4-2 on the connector pins.

Further information on the application of the can be found in Ref. 2

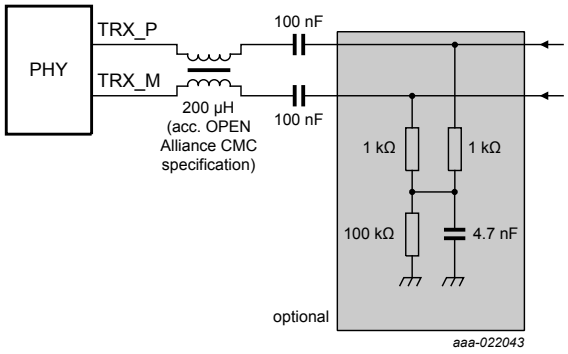


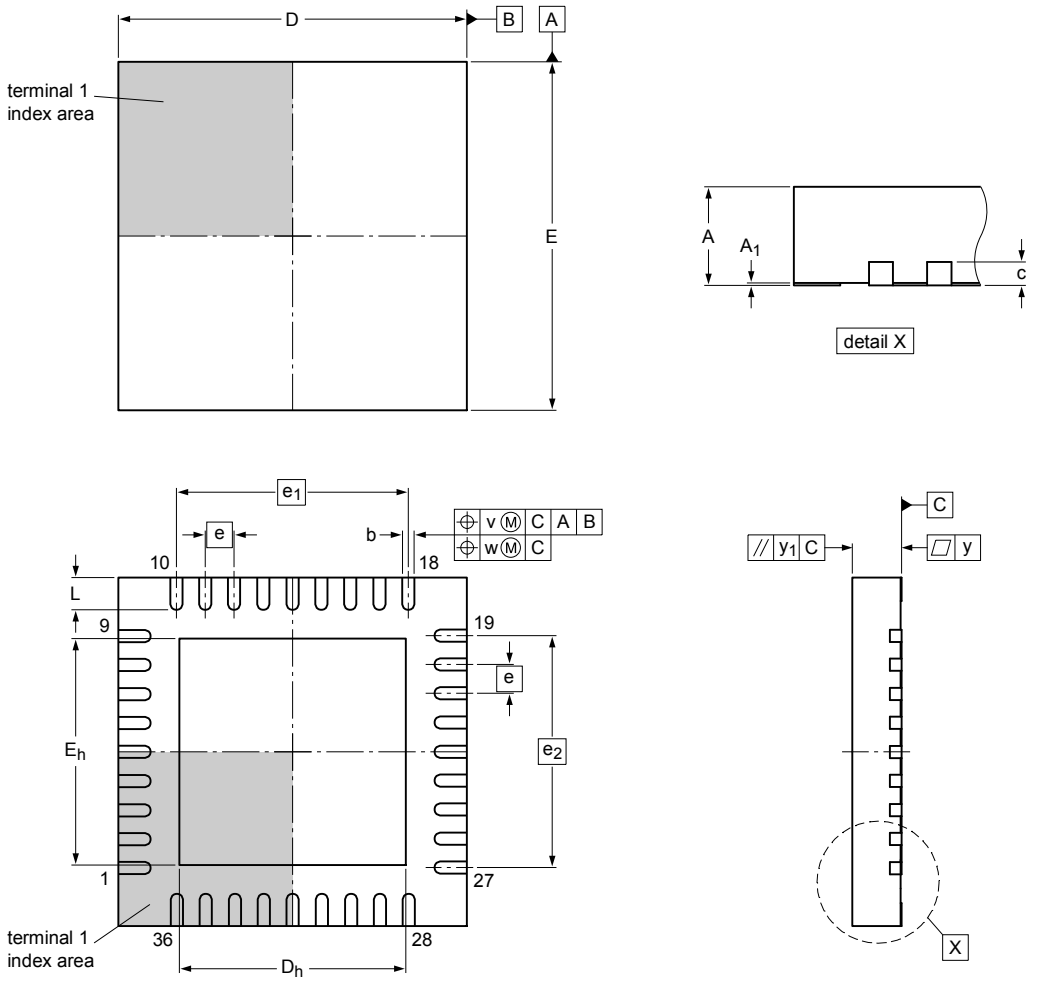
Figure 6. MDI circuit diagram

7 Package information

The TJA1101 comes in a HVQFN-36 package as shown in Figure 7. Measuring just 36 mm^2 with a pitch of 0.5 mm, it is particularly suited to PCB space-constrained applications, such as an integrated IP camera module. The package features wettable sides/flanks to allow for optical inspection of the soldering process. The exposed die pad shown in the package diagram should be connected to ground.

8 Package outline

HVQFN36: plastic thermal enhanced very thin quad flat package; no leads; 36 terminals; body 6 x 6 x 0.85 mm **SOT1092-2**



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	1.00	0.05	0.30		6.1	4.05	6.1	4.05				0.65				
	nom	0.85	0.02	0.21	0.2	6.0	3.90	6.0	3.90	0.5	4	4	0.55	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		5.9	3.75	5.9	3.75				0.45				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1092-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1092-2		---	---			~~09-02-23~~ 09-02-24

Figure 7. Package outline SOT1092-2 (HVQFN36)

9 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

9.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

9.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

9.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

9.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Fig 14) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 2 and Table 3.

Table 2. SnPb eutectic process (from J-STD-020D)

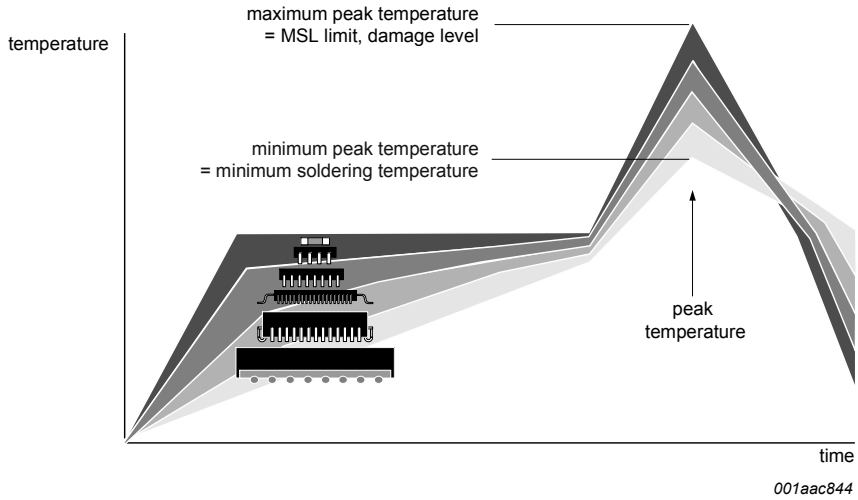
Package thickness (mm)	Package reflow temperature (°C) Volume (mm^3)	
	< 350	≥350
< 2.5	235	220
≥2.5	220	220

Table 3. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C) Volume (mm^3)		
	< 350	350 to 2000	>2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 8.



MSL: Moisture Sensitivity Level

Figure 8. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

10 References

1. IEEE Std 802.3bw-2015, 26 October 2015
2. AH1706_TJA1101 Application Hints

11 Revision history

Table 4. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1101_SDS v.1	20180426	Product short data sheet	-	-

12 Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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