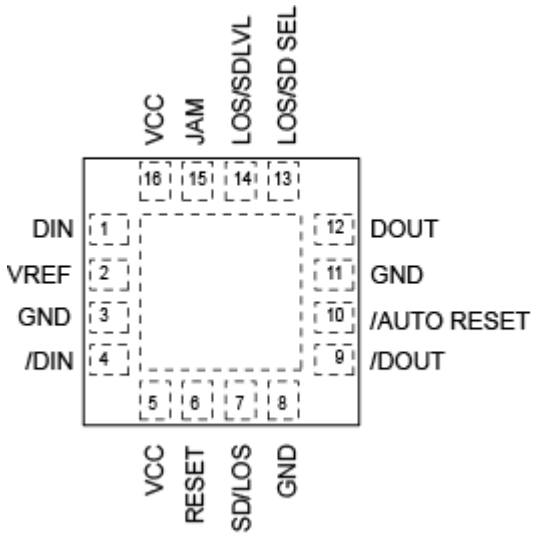
Ordering Information

Part Number	Package Type	Operating Range	Package Marking
SY88349NDLMG	Lead-Free 16-Pin 3mm × 3mm QFN	–40°C to +85°C	349N with Pb-Free Bar-Line Indicator
SY88349NDLMGTR[1]	Lead-Free 16-Pin 3mm × 3mm QFN	–40°C to +85°C	349N with Pb-Free Bar-Line Indicator

Note:

1. Tape & Reel.

Pin Configuration



16-Pin 3mm × 3mm QFN (QFN-16)

Pin Description

Pin Number	Pin Name	Pin Function
1, 4	DIN, /DIN	Data Inputs. If AC-coupled, terminate each pin to V_{REF} with 50Ω.
2	VREF	Reference Voltage Output. Typically V_{CC} – 1.3V.
3, 11, 8	GND	Device Ground.
10	/AUTO RESET	LVTTL Input. This pin is internally connected to a 25kΩ pull-up resistor and defaults to HIGH. When this pin is LOW or tied to ground, the /AUTO RESET function is enabled and SD de-asserts or LOS asserts within 100ns (typical) after the last high-to -low transition of the burst input. When this pin is left floating or not connected, the AUTO RESET function is disabled and the SD de-assert or LOS assert must be forced by using the manual RESET function.
5, 16	VCC	Positive Power Supply.

Pin Description (Continued)

Pin Number	Pin Name	Pin Function
6	RESET	LVTTL Input. Apply a high-level signal (>2V) to this pin to discharge the time constant and reset the signal de-assert time or LOS assert time within 5ns. RESET defaults to LOW if left floating. If the /AUTO RESET function is not used, this RESET function needs to be used to quickly de-assert the SD or assert LOS. This pin is internally connected to a 25kΩ pull-down resistor and defaults to LOW.
7	SD/LOS	LVTTL Output. Signal-detect (SD) asserts HIGH when the data input amplitude rises above the threshold sets by SD_{LVL}. Conversely, loss-of-signal (LOS) de-asserts LOW when the data input amplitude rises above the threshold set by LOS_{LVL}.
12, 9	DOUT, /DOUT	CML Outputs. When JAM disables the device, output DOUT is forced to logic LOW and output /DOUT is forced to logic HIGH.
13	LOS/SD SEL	Allows the user to select between whether LOS or SD is outputted on the LOS/SD pin and whether the noise discriminator is enabled or disabled. Please see Truth Table for more information. Also controls the polarity of the JAM input. When SD (regardless of the noise discriminator status) is selected, JAM is active HIGH and LOS/SD (Pin 7) operates as signal detect. Conversely, when LOS is selected, JAM is active LOW and LOS/SD operates as loss-of-signal. Pin must be tied to one of the four options and cannot be left open.
14	LOS/SDLVL	Voltage Input. Sets the Loss of Signal/Signal Detect Level. A resistor from this pin to V_{CC} sets the threshold for the data input amplitude at which LOS/SD will be asserted.
15	JAM	LVTTL Input. This JAM input acts as a squelch function and switches its polarity depending on LOS/SDSEL status. When LOS is selected, this pin is active LOW. When SD is selected, this pin is active HIGH. To create a squelch function, connect JAM to LOS/SD. When JAM disables the device, output Q is forced to logic LOW and output /Q is forced to logic HIGH Note that this input is internally connected to a 25kΩ pull-up resistor.

Truth Table for SD/LOS Select and Noise Discriminator function

LOS/SDSEL PIN	LOS/SD SELECTION	NOISE DISCRIMINATOR	INPUT TO JAM	OUTPUTS
0Ω to VCC	SD	Enabled	HIGH	Enabled
0Ω to VCC	SD	Enabled	LOW	Disabled
16KΩ to VCC	SD	Disabled	HIGH	Enabled
16KΩ to VCC	SD	Disabled	LOW	Disabled
16KΩ to GND	LOS	Disabled	HIGH	Disabled
16KΩ to GND	LOS	Disabled	LOW	Enabled
0Ω to GND	LOS	Enabled	HIGH	Disabled
0Ω to GND	LOS	Enabled	LOW	Enabled

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... -0.3V to +4.0V
Input Voltage (DIN, /DIN) ..... 0 to V_{CC}
Output Current (I_{OUT})
  Continuous ..... ±50mA
  Surge ..... ±100mA
EN Voltage ..... -0.3V to V_{CC}
V_{REF} Current ..... –800µA to +500µA
SD_{LVL} Voltage ..... V_{REF} to V_{CC}
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance[3]
  QFN (θ_{JA}) Still-Air ..... 60°C/W
  QFN (Ψ_{JB}) Junction-to-Board ..... 38°C/W

DC Electrical Characteristics

V_{CC} = 3.0 to 3.6V; T_A = –40°C to +85°C, typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Power Supply Current	No output load		90	120	mA
LOS/SD_{LVL}	LOS/SD_{LVL} Voltage		V_{REF}		V_{CC}	V
V_{OH}	CML Output HIGH Voltage	Note12	V_{CC} – 0.020	V_{CC} – 0.005	V_{CC}	V
V_{OL}	CML Output LOW Voltage	Note 12	V_{CC} – 0.475	V_{CC} – 0.4	V_{CC} – 0.350	V
V_{OFFSET}	Input Offset Voltage				±1	mV
$V_{IHCMR(Diff)}$	Common-Mode Range (Differential)	Note 4	GND +1.4		Vcc	V
$V_{IHCMR(SE)}$	Common-Mode Range (Single Ended)	Note 4	GND +1.2		V_{CC}	V
V_{REF}	Reference Voltage		V_{CC} – 1.48	V_{CC} – 1.32	V_{CC} – 1.16	V
I_{DIN}	Input Sink Current (DIN and /DIN)	Vin =VIH		8.5	20	µA

LVTTL DC Electrical Characteristics

V_{CC} = 3.0 to 3.6V; T_A = –40°C to +85°C, typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	LVTTL Input HIGH Voltage		2.0			V
V_{IL}	LVTTL Input LOW Voltage				0.8	V
I_{IH_JAM}	JAM Input HIGH Current	V_{IN} = V_{CC} V_{IN} = 2.7V			20 20	µA
I_{IL_JAM}	JAM Input LOW Current	V_{IN} = 0.5V	–0.3			mA
I_{IH_AR}	/AUTORESET Input HIGH Current	V_{IN} = V_{CC} V_{IN} = 2.7V			100 20	µA
I_{IL_AR}	/AUTORESET Input LOW Current	V_{IN} = 0.5V	–0.3			mA
I_{IH_RESET}	RESET Input HIGH Current	V_{IN} = V_{CC} V_{IN} = 2.7V			300 250	µA
I_{IL_RESET}	RESET Input LOW Current	V_{IN} = 0.5V	0			mA
V_{OH}	SD/LOS Output HIGH Level	I_{OH} = –100uA	2.1	2.7		V
V_{OL}	SD/LOS Output LOW Level	I_{OL} = 100uA		0.35	0.5	V

AC Electrical Characteristics

V_{CC} = 3.0V to 3.6V; R_L = 50Ω to V_{CC}; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_r, t_f	Output Rise/Fall Time (20% to 80%)	Note 4			150	ps
t_{JAM}	JAM Enable/Disable Time				2	ns
$t_{AUTORESET}$	SD De-Assert or LOS Assert with Auto Reset Enabled		75	120	150	ns
t_{RESET}	RESET Disable Time	Note 5			5	ns
t_{ON}	SD Assert Time/LOS De-Assert Time	Noise Discriminator Bypassed			5	ns
t_{ON_ND}	SD Assert Time/LOS De-Assert Time	Noise Discriminator Enabled			7	ns
t_{JITTER}	Deterministic	Note 6		15		ps_{PP}
	Random	Note 7		5		ps_{RMS}
V_{ID}	Differential Input Voltage Swing	Figure 1	5		1800	mV_{PP}
V_{OD}	Differential Output Voltage Swing	$V_{ID} \geq 18mV_{PP}$ Note 12	660	800	940	mV_{PP}
SD_{AL} /LOS_{DL}	Low SD Assert/LOS De-Assert Level	$R_{LOS/SDLVL}$ = 10kΩ (8, 10, 13)		9		mV_{PP}
SD_{DL}/LOS_{AL}	Low SD De-Assert/LOS Assert Level	$R_{LOS/SDLVL}$ = 10kΩ (10, 13)		4.5		mV_{PP}
HYS_L	Low SD/LOS Hysteresis	$R_{LOS/SDLVL}$ = 10kΩ (11, 13)		6		dB
SD_{AM}/LOS_{DM}	Medium SD Assert/LOS De-Assert Level	$R_{LOS/SDLVL}$ = 5kΩ (10, 13)	9.4	12.5	15.6	mV_{PP}
SD_{DM}/LOS_{AM}	Medium SD De-Assert/LOS Assert Level	$R_{LOS/SDLVL}$ = 5kΩ (10, 13)	5	7	8.6	mV_{PP}
HYS_M	Medium SD/LOS Hysteresis	$R_{LOS/SDLVL}$ = 5kΩ (11, 13)	3.5	5	7	dB
SD_{AH}/LOS_{DH}	High SD Assert/LOS De-assert Level	$R_{LOS/SDLVL}$ = 100Ω (10, 13)	27	35	45	mV_{PP}
SD_{DH}/LOS_{AH}	High SD De-Assert/ LOS Assert Level	$R_{LOS/SDLVL}$ = 100Ω (10, 13)	15	21	28	mV_{PP}
HYS_H	High SD/LOS Hysteresis	$R_{LOS/SDLVL}$ = 100Ω (11, 13)	2	4.5	6	dB
$A_{V(Diff)}$	Differential Voltage Gain			42		dB
S_{21}	Single-Ended Small-Signal Gain			36		dB

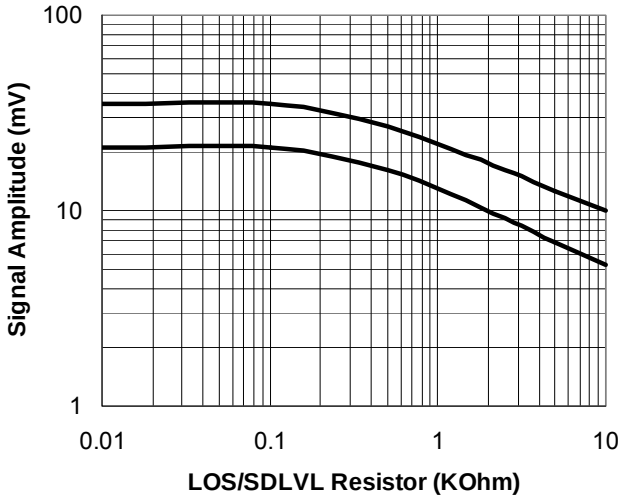
Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance assumes the use of a 4-layer PCB. Exposed pad must be soldered to the device's most negative potential on the PCB.
4. VIHCMR is defined as common mode range of the VIH level on DIN and /DIN. It is the most positive level of the differential input signal when driven differentially or is the reference level on Din\ when being driven single ended.
5. Amplifier in limiting mode. Input is a 200MHz square wave.
6. Deterministic jitter measured using 2.5Gbps K28.5 pattern, V_{ID} = $10mV_{PP}$.
7. Random jitter measured using 2.5Gbps K28.7 pattern, V_{ID} = $10mV_{PP}$.
8. SD is the opposite polarity of LOS. Therefore, an SD Assert parameter is equivalent to a LOS de-assert parameter and vice versa.
9. See "Typical Operating Characteristics" for graphs showing input signal vs. SD Assert/LOS de-assert time at various $R_{LOS/SDLVL}$ settings.
10. See "Typical Operating Characteristics" for graph showing how to choose a particular $R_{LOS/SDLVL}$ for a particular assert and its associated de-assert amplitude.
11. This specification defines electrical hysteresis as 20log(SD assert/SD de-assert). The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2 depending upon the level of received optical power and ROSA characteristics. Based upon that ratio, the optical hysteresis corresponding to the electrical hysteresis range 2dB-5dB, shown in the AC characteristics table, will be 1dB-4dB optical hysteresis.
12. V_{OL} and V_{OH} are measured with outputs loaded with 50 Ohms as shown in Figure 3b and V_{OD} is measured in accordance with Figures 3a and/or 3b.
13. All SD Assert (LOS De-Assert) level, SD De-assert (LOS Assert) level and Hysteresis specifications listed above are specified using a 1010 PON Preamble data pattern at the specified data rate of 2.488 Gbps.

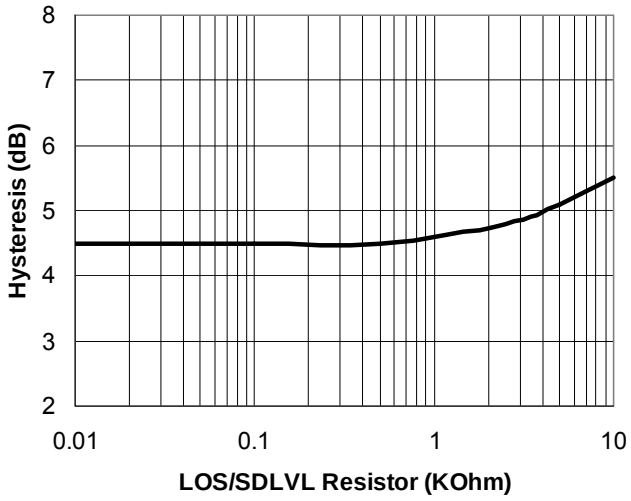
Typical Operating Characteristics

V_{CC} = 3.3V, T_A = 25°C, R_L = 50Ω to V_{CC}, unless noted.

LOS Assert/De-Assert Levels

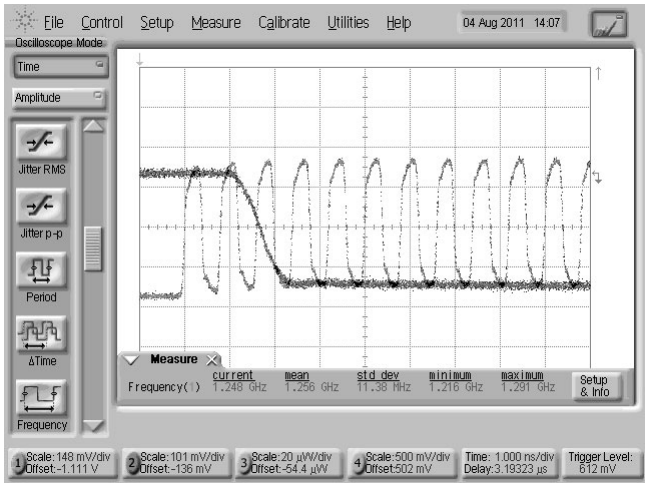


LOS/SD Hysteresis

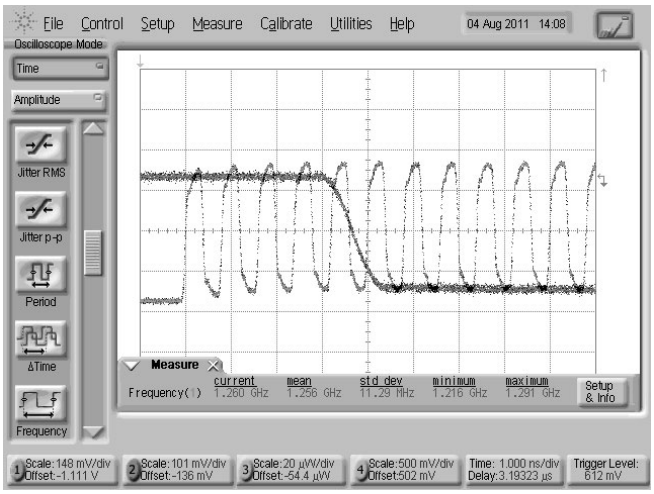


Note:

SD/LOS Sensitivity with RLOS/SD at 0Ω is the same as with 0.01 kΩ

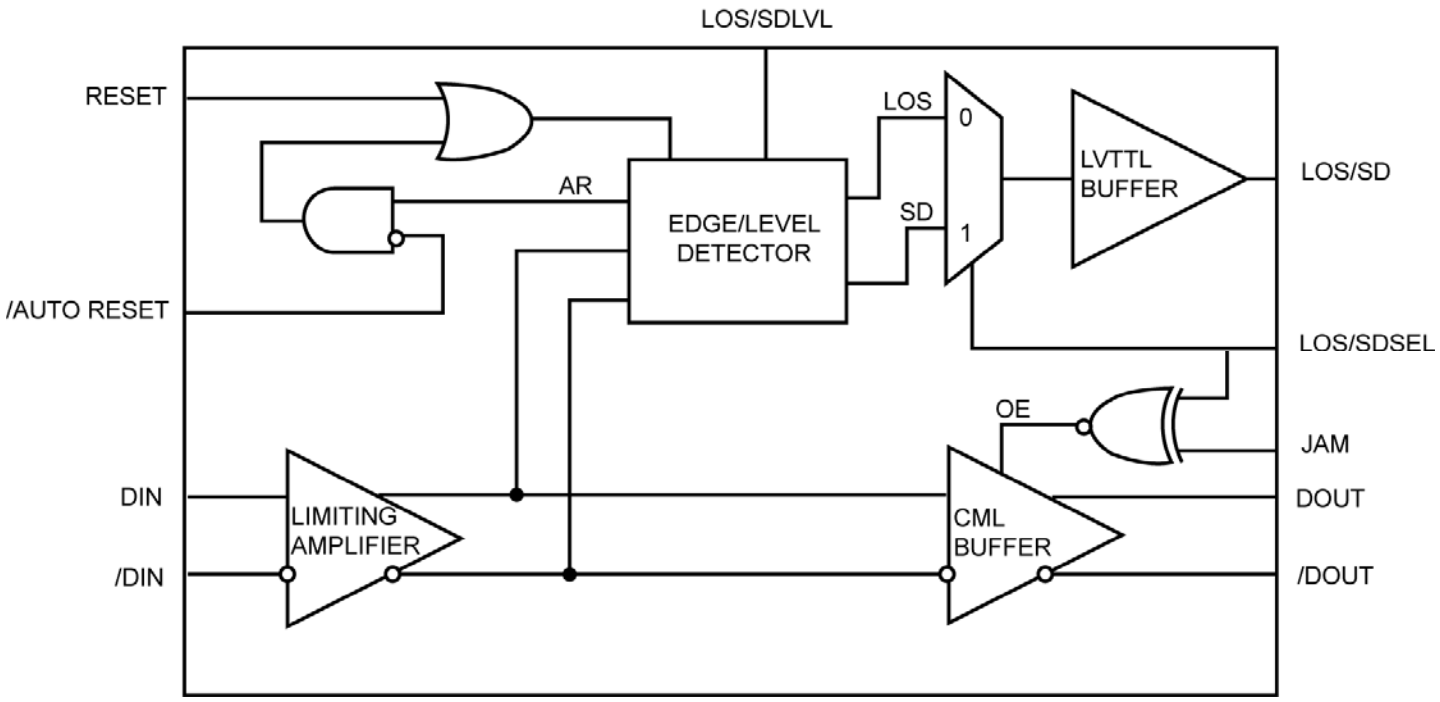


Input signal and LOS De-assert with Noise Discriminator Bypass and without Jam



Input signal and LOS with Noise Discriminator Engaged and without Jam

Functional Diagram



Detailed Description

The SY88349NDL is a high-sensitivity limiting post amplifier which operates on a +3.3V power supply over the industrial temperature range. Signals with data rates up to 2.5Gbps and as small as 5mVpp can be amplified. Depending on the LOS/SDSEL option, the SY88349NDL can generate an SD or LOS output, and allow feedback to the JAM input for output stability. LOS/SD_{LVL} sets the sensitivity of the input amplitude detection.

To satisfy the stringent timing requirements of the GPON specifications, the signal detect circuit offers 5ns SD assert (LOS de-assert) time and the option to de-assert SD (assert LOS) using the /AUTO RESET or manual RESET function. When /AUTO RESET is enabled, SD de-asserts/LOS asserts automatically within approximately 120ns after the last high-to-low transition of the input burst. When the /AUTORESET function is disabled, the SD De-assert/LOS Assert time can be reset by using the provided RESET pin.

Input Buffer

Figure 2 shows a simplified schematic of the input stage. The high sensitivity of the input amplifier allows signals as small as 5mVpp to be detected and amplified. The input buffer can allow input signals as large as 1800mVPP. Input signals are linearly amplified with a typically 48dB differential voltage gain until the outputs reach 1500mV_{PP} (typical). Applications requiring the SY88349NDL to operate with high-gain should have the upstream TIA placed as close as possible to the SY88349NDL's input pins. This ensures the best performance of the device.

Output Buffer

The SY88349NDL's CML output buffer is designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to V_{CC} for each output pin provides this. Figure 3 shows a simplified schematic of the output stage.

Loss of Signal/Signal Detect

The SY88349NDL generates a chatter-free signal-detect (SD) or LOS LVTTL output, as shown in Figure 4. A highly-sensitive signal detect circuit is used to determine that the input amplitude is too small to be considered a valid input. LOS asserts high if the input amplitude falls below the threshold sets by LOS/SDLVL and de-asserts low otherwise. SD asserts high if the input amplitude rises above threshold set by LOS/SDLVL and de-asserts low otherwise. LOS/SD can be fed back to the JAM input to maintain output stability under the absence of an invalid signal condition. Typically, a 4.5dB to 5.5dB hysteresis is provided to prevent chattering.

LOS/SD Level Set

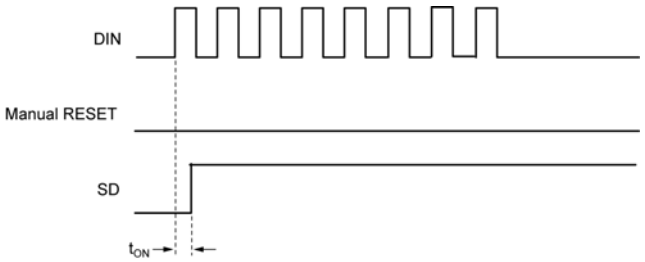
A programmable LOS/SD level pin (LOS/SD_{LVL}) sets the threshold of the input amplitude detection. Connecting an external resistor between V_{CC} and LOS/SD_{LVL} sets the voltage at LOS/SD_{LVL}. This voltage ranges from V_{CC} to V_{REF}. The external resistor creates a voltage divider between V_{CC} and V_{REF}, as shown in Figure 5. Set the LOS/SD_{LVL} voltage closer to V_{REF} or more sensitive LOS/SD detection or closer to V_{CC} for higher inputs.

Note that the SY88349NDL is designed for use in the burst mode PON application where every burst is preceded with several bytes of a 1010 PON preamble pattern. Therefore the SD Assert (LOS De-assert) is designed to trigger on the first few bits of this preamble pattern and therefore the SD/LOS thresholds outlined in the AC electrical characteristics are specified using this preamble pattern. Once the SD is Asserted (LOS De-asserted), the SD is De-asserted (LOS Asserted) only by the application of a Manual RESET or an AUTO RESET if the Auto Reset is activated, The auto reset asserts a reset approximately 120 nS after the last negative going transition of the data as explained earlier.

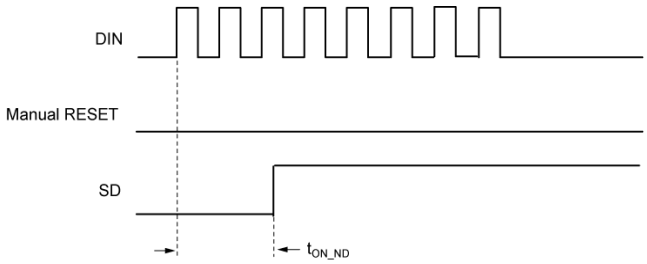
Noise Discriminator

The noise discriminator feature is intended for the high-gain burst-mode TIAs where noise can trigger a false LOS deassert or SD assert while no input data is present. The noise discriminator will filter input data through a series of specialized circuitry that will only trigger LOS/SD on the rising edge of a valid PON 2.488 Gbps preamble bit stream (10101). The SY88349NDL noise discriminator is designed to accept a 2.488 Gbps +/-300 MBPS preamble burst. Any other bit pattern will be rejected. If this part is used at any other data rate, the Noise Discriminator should be disengaged. The noise discriminator, implemented in the edge detector circuit, can be selected or bypassed by selecting the proper resistor value using the settings at LOS/SDSEL pin. Refer to the "Truth Table for SD/LOS select and Noise Discriminator function" found on page 3 for more detailed information.

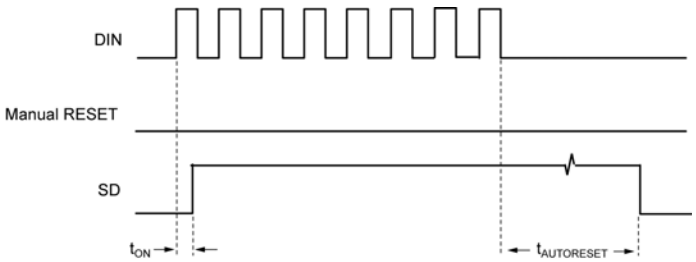
Timing Diagrams



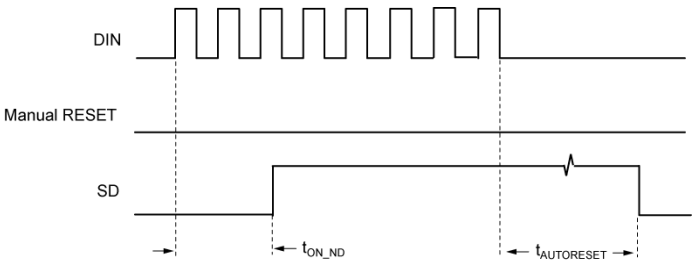
a) No Manual RESET and /AUTORESET Tied HIGH (Noise Discriminator OFF)



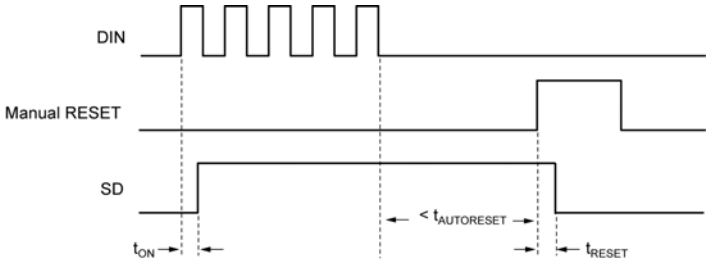
b) No Manual RESET and /AUTORESET Tied HIGH (Noise Discriminator ON)



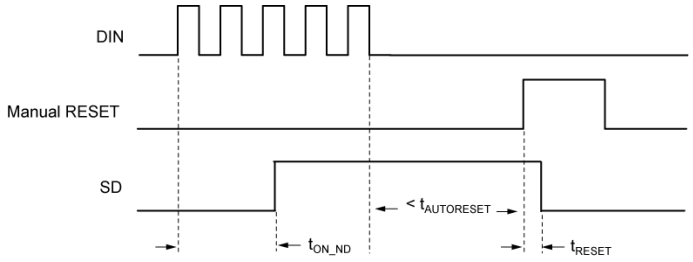
c) No Manual RESET and /AUTORESET Tied LOW (Noise Discriminator OFF)



d) No Manual RESET and /AUTORESET Tied LOW (Noise Discriminator ON)

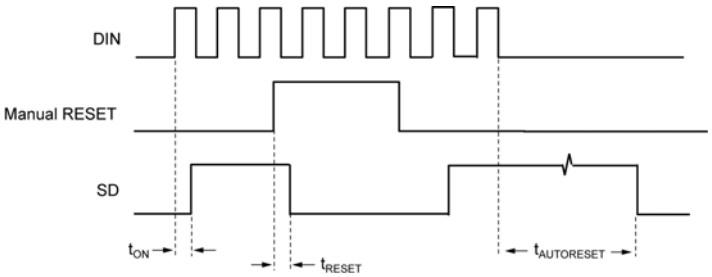


e) Manual RESET and /AUTORESET Tied HIGH or LOW (Noise Discriminator OFF)

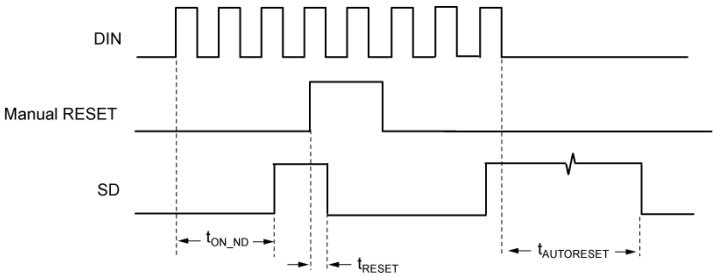


f) Manual RESET and /AUTORESET Tied HIGH or LOW (Noise Discriminator ON)

Timing Diagrams (Continued)



g) Manual RESET Pulse and /AUTORESET Tied LOW (Noise Discriminator OFF)



h) Manual RESET Pulse and /AUTORESET Tied LOW (Noise Discriminator ON)

Input Signal Amplitude

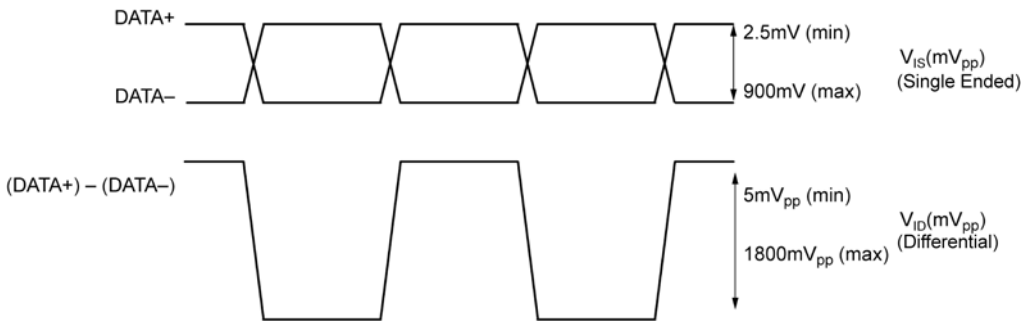


Figure 1. VIS (single ended) and VID (differential) Definition

Simplified Circuit Diagrams

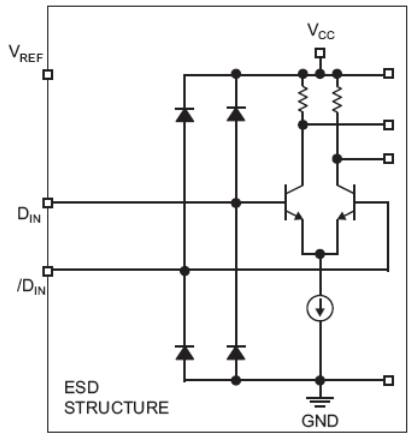


Figure 2. Simplified Input Structure

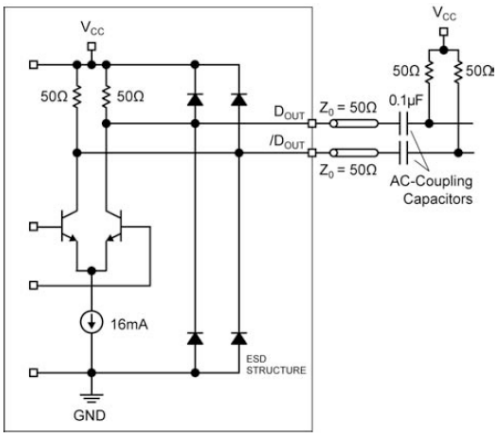


Figure 3a. Simplified Output Structure with AC-Coupled Termination

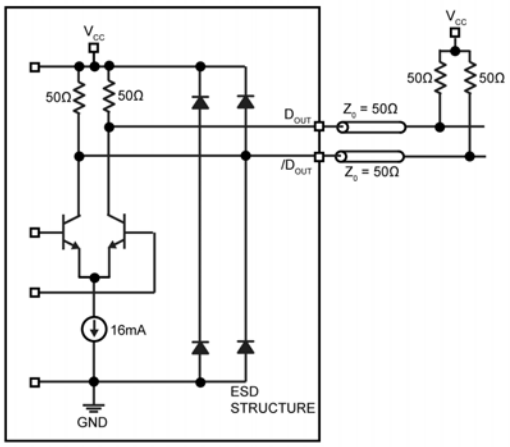


Figure 3b. Simplified Output Structure with DC-Coupled Termination

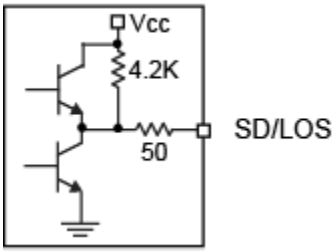


Figure 4. Simplified LOS/SD Output Structure

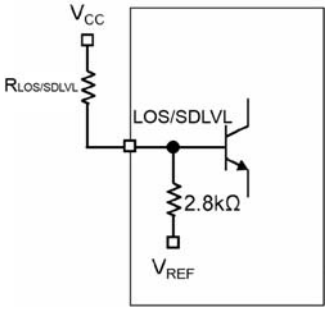
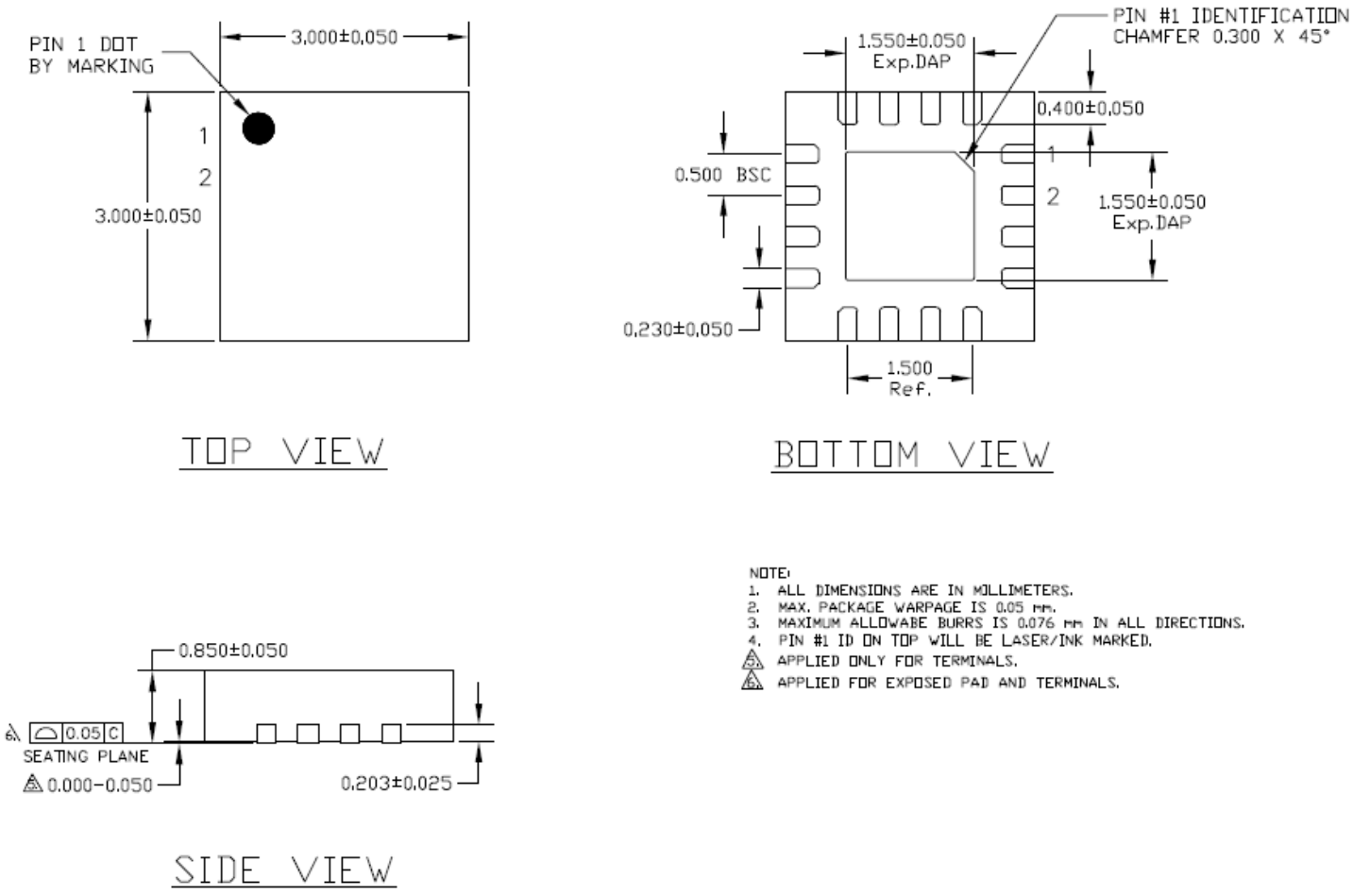


Figure 5. Simplified LOS/SD_{LVL} Setting Circuit

hbwhelp@micrel.com or (408) 955-1690

Package Information



16-Pin QFN (QFN-16)

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