STK541UC60C-E

Intelligent Power Module (IPM)
600 V, 10 A

ON Semiconductor®

www.onsemi.com

Overview

This “Inverter IPM” is highly integrated device containing all High Voltage (HV) control from HV-DC to 3-phase outputs in a single SIP module (Single-In line Package). Output stage uses IGBT / FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection (OCP) with a Fault Detection output flag. Internal Boost diodes are provided for high side gate boost drive.

Function

- Single control power supply due to Internal bootstrap circuit for high side pre-driver circuit
- All control input and status output are at low voltage levels directly compatible with microcontrollers
- Built-in cross conduction prevention

Certification

- UL Recognized (File Number : E339285)

Specifications

Absolute Maximum Ratings at Tc = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}	P to N, surge < 500 V *1	450	V
Collector-emitter voltage	V_{CE}	P to U,V,W or U,V,W to N	600	V
Output current	Io	P, N, U,V,W terminal current	±10	A
		P, N, U,V,W terminal current at Tc = 100°C	±5	A
Output peak current	Iop	P, N, U,V,W terminal current for a Pulse width of 1ms	±20	A
Pre-driver voltage	VD1, 2, 3, 4	VB1 to U, VB2 to V, VB3 to W, V_{DD} to V_{SS} *2	20	V
Input signal voltage	VIN	HIN1, 2, 3, LIN1, 2, 3	–0.3 to 7	V
FAULT terminal voltage	VFAULT	FAULT terminal	–0.3 to V_{DD}	V
Maximum power dissipation	Pd	IGBT per channel	22	W
Junction temperature	Tj	IGBT,FRD	150	°C
Storage temperature	Tstg		–40 to +125	°C
Operating substrate temperature	Tc	IPM case temperature	–40 to +100	°C
Tightening torque		Case mounting screws *3	0.9	Nm
Isolation Voltage	Vis	50 Hz sine wave AC 1 minute *4	2000	VRMS

Reference voltage is “V_{SS}” terminal voltage unless otherwise specified.

*1 : Surge voltage developed by the switching operation due to the wiring inductance between “P” and “N” terminal.
*2 : VD1 = VB1 to U, VD2 = VB2 to V, VD3 = VB3 to W, VD4 = V_{DD} to V_{SS} terminal voltage.
*3 : Flatness of the heat-sink should be less than 0.15 mm.
*4 : Test conditions : AC 2500 V, 1 second.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

Electrical Characteristics at Tc = 25°C, VD1, VD2, VD3, VD4 = 15 V

Parameter	Symbol	Conditions		Test circuit	min	typ	max	Unit
Power output section								
Collector-emitter cut-off current	I_{CE}	V_{CE} = 600 V		Fig.1	-	-	0.1	mA
Bootstrap diode reverse current	IR(BD)	VR(BD)			-	-	0.1	mA
Collector to emitter saturation voltage	V_{CE}(SAT)	Ic = 10 A Tj = 25°C	Upper side	Fig.2	-	1.4	2.3	V
			Lower side *1		-	1.7	2.6	
		Ic = 5 A Tj = 100°C	Upper side		-	1.3	-	
			Lower side *1		-	1.5	-	
Diode forward voltage	V_F	IF = 10 A Tj = 25°C	Upper side	Fig.3	-	1.3	2.2	V
			Lower side *1		-	1.6	2.5	
		IF = 5 A Tj = 100°C	Upper side		-	1.2	-	
			Lower side *1		-	1.4	-	
Junction to case thermal resistance	θj-c(T)	IGBT			-	-	5.5	°C/W
	θj-c(D)	FRD			-	-	6.5	
Control (Pre-driver) section								
Pre-driver power dissipation	ID	VD1, 2, 3 = 15 V		Fig.4	-	0.08	0.4	mA
		VD4 = 15 V			-	1.6	4.0	
High level Input voltage	Vin H	HIN1, HIN2, HIN3, LIN1, LIN2, LIN3 to V_{SS}			2.5	-	-	V
Low level Input voltage	Vin L				-	-	0.8	V
Input threshold voltage hysteresis	Vinth(hys)				0.5	0.8	-	V
Logic 0 input leakage current	I_{IN+}	VIN = +3.3 V			76	118	160	μA
Logic 1 input leakage current	I_{IN-}	VIN = 0 V			97	150	203	μA
FAULT terminal sink current	IoSD	FAULT : ON/VFAULT = 0.1 V			-	2	-	mA
FAULT clear time	FLTCLR	Fault output latch time			6	9	12	ms
V_{CC} and V_S undervoltage positive going threshold	V_{CCUP} V_{SUP}				10.5	11.1	11.7	V
V_{CC} and V_S undervoltage negative going threshold	V_{CCUN} V_{SUN}				10.3	10.9	11.5	V
V_{CC} and V_S undervoltage hysteresis	V_{CCUVH} V_{SUVH-}				0.14	0.2	-	V
Over current protection level	ISD	PW = 100 μs		Fig.5	10	-	17	A
Output level for current monitor	ISO	Io = 10 A			0.30	0.33	0.36	V

Reference voltage is "V_{SS}" terminal voltage unless otherwise specified.

*1 : The lower side's V_{CE}(SAT) and VF include a loss by the shunt resistance

Electrical Characteristics at Tc = 25°C, VD1, VD2, VD3, VD4 = 15 V, V_{CC} = 300 V, L = 3.9 mH

Parameter	Symbol	Conditions	Test circuit	min	typ	max	Unit
Switching Character							
Switching time	tON	Io = 10 A	Fig.6	0.3	0.6	1.3	μs
	tOFF			-	1.0	1.8	
Turn-on switching loss	Eon	Io = 5 A	Fig.6	-	240	-	μJ
Turn-off switching loss	Eoff			-	220	-	μJ
Total switching loss	Etot			-	460	-	μJ
Turn-on switching loss	Eon	Io = 5 A, Tc = 100°C	Fig.6	-	300	-	μJ
Turn-off switching loss	Eoff			-	260	-	μJ
Total switching loss	Etot			-	560	-	μJ
Diode reverse recovery energy	Erec	I_F = 5 A, P = 400 V, Tc = 100°C		-	17	-	μJ
Diode reverse recovery time	trr			-	62	-	ns
Reverse bias safe operating area	RBSOA	Io = 20 A, V_{CE} = 450 V		Full square			
Short circuit safe operating area	SCSOA	V_{CE} = 400 V, Tc = 100°C		4	-	-	μs

Reference voltage is "V_{SS}" terminal voltage unless otherwise specified.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Notes

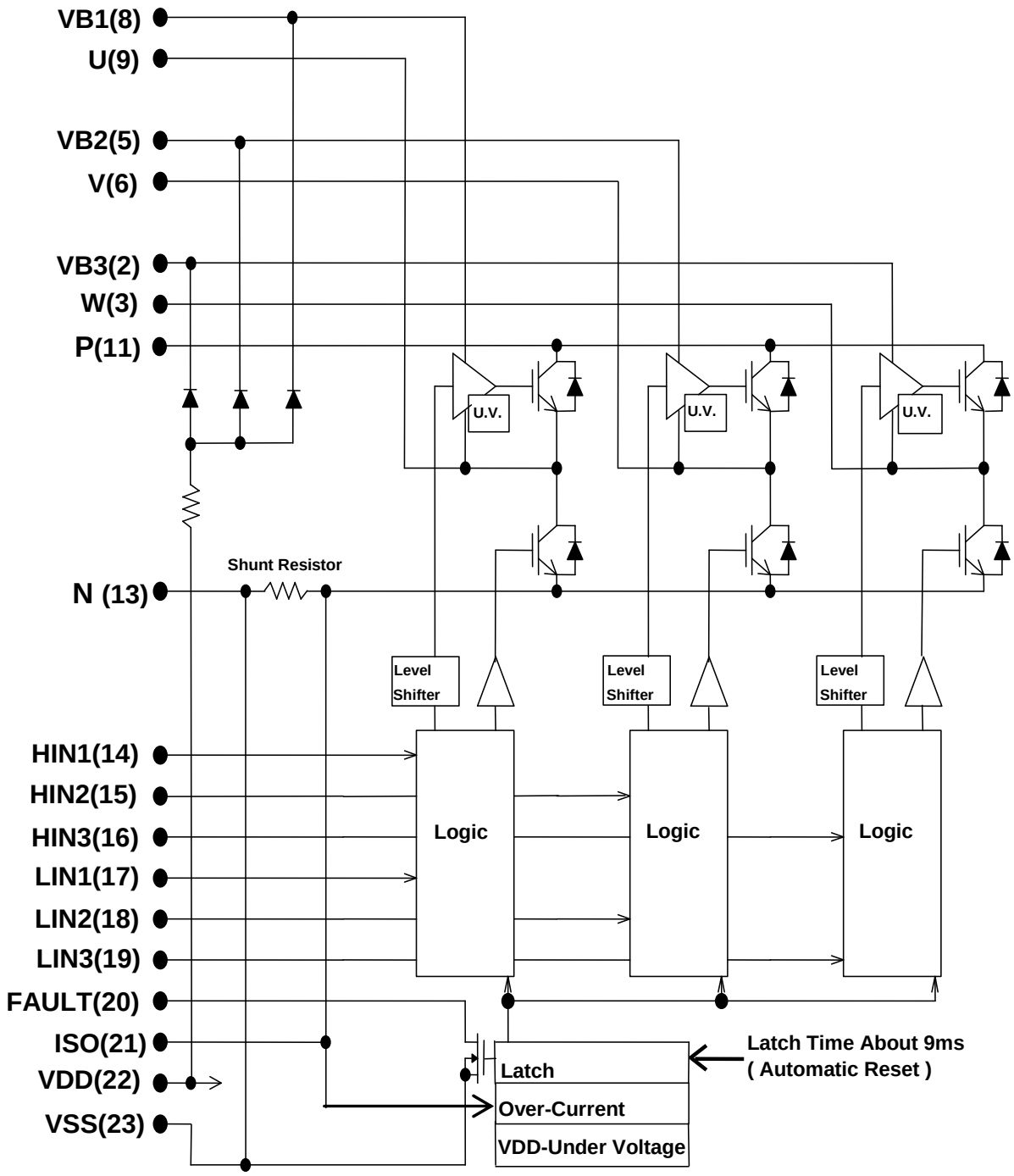
1. The pre-drive power supply low voltage protection has approximately 0.2 V of hysteresis and operates as follows.

   Upper side : The gate is turned off and will return to regular operation when recovering to the normal voltage, but the latch will continue till the input signal will turn ‘high’.

   Lower side : The gate is turned off and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.

2. The pre-drive low voltage protection is the feature to protect devices when the pre-driver supply voltage falls due to an operating malfunction.

Equivalent Block Diagram



Module Pin-Out Description

Pin	Name	Description
1	–	Without Pin
2	VB3	High Side Floating Supply Voltage 3
3	W,VS3	Output 3 - High Side Floating Supply Offset Voltage
4	–	Without Pin
5	VB2	High Side Floating Supply voltage 2
6	V,VS2	Output 2 - High Side Floating Supply Offset Voltage
7	–	Without Pin
8	VB1	High Side Floating Supply voltage 1
9	U,VS1	Output 1 - High Side Floating Supply Offset Voltage
10	–	Without Pin
11	P	Positive Bus Input Voltage
12	–	Without Pin
13	N	Negative Bus Input Voltage
14	HIN1	Logic Input High Side Gate Driver - Phase U
15	HIN2	Logic Input High Side Gate Driver - Phase V
16	HIN3	Logic Input High Side Gate Driver - Phase W
17	LIN1	Logic Input Low Side Gate Driver - Phase U
18	LIN2	Logic Input Low Side Gate Driver - Phase V
19	LIN3	Logic Input Low Side Gate Driver - Phase W
20	FAULT	Fault output
21	ISO	Current monitor output
22	VDD	+15 V Main Supply
23	VSS	Negative Main Supply

Test Circuit

The tested phase U+ shows the upper side of the U phase and U− shows the lower side of the U phase.

■ I_{CE} / IR(BD)

	U+	V+	W+	U-	V-	W-
M	11	11	11	9	6	3
N	9	6	3	13	13	13

	U(BD)	V(BD)	W(BD)
M	8	5	2
N	23	23	23

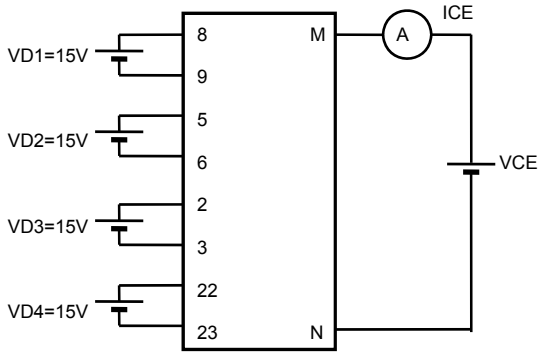


Fig.1

■ V_{CE}(SAT) (test by pulse)

	U+	V+	W+	U-	V-	W-
M	11	11	11	9	6	3
N	9	6	3	13	13	13
m	14	15	16	17	18	19

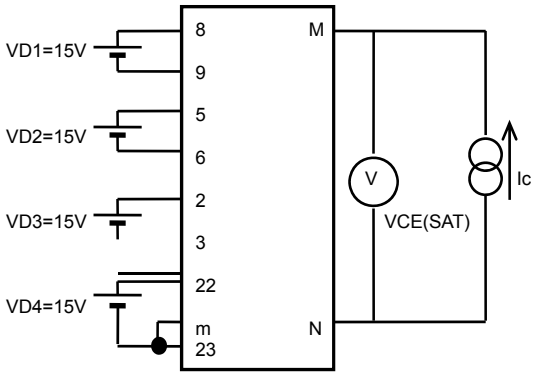


Fig.2

■ V_F (test by pulse)

	U+	V+	W+	U-	V-	W-
M	11	11	11	9	6	3
N	9	6	3	13	13	13

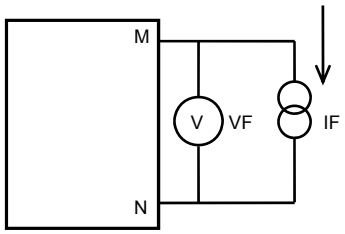


Fig.3

■ ID

	VD1	VD2	VD3	VD4
M	8	5	2	22
N	9	6	3	23

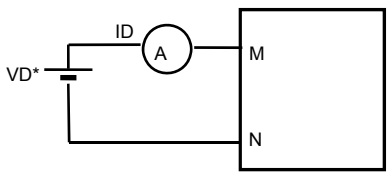


Fig.4

■ ISD

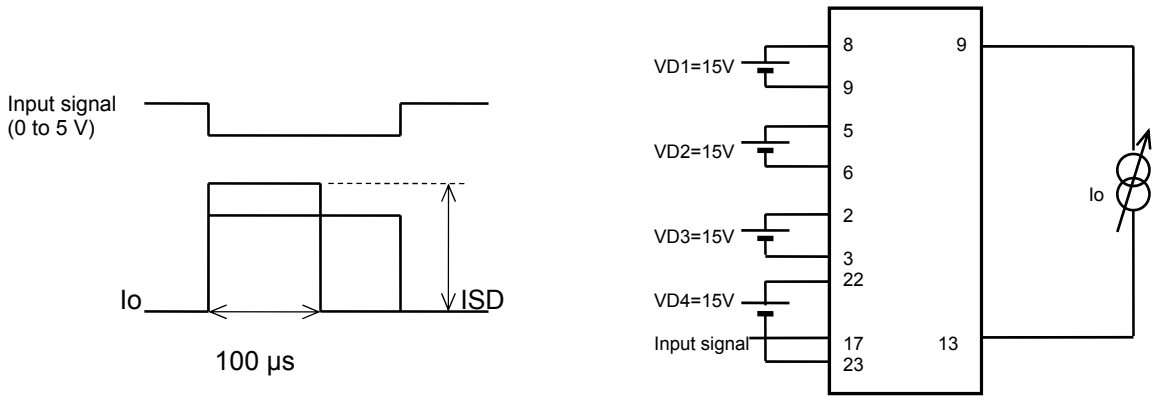


Fig.5

■ Switching time (The circuit is a representative example of the lower side U phase.)

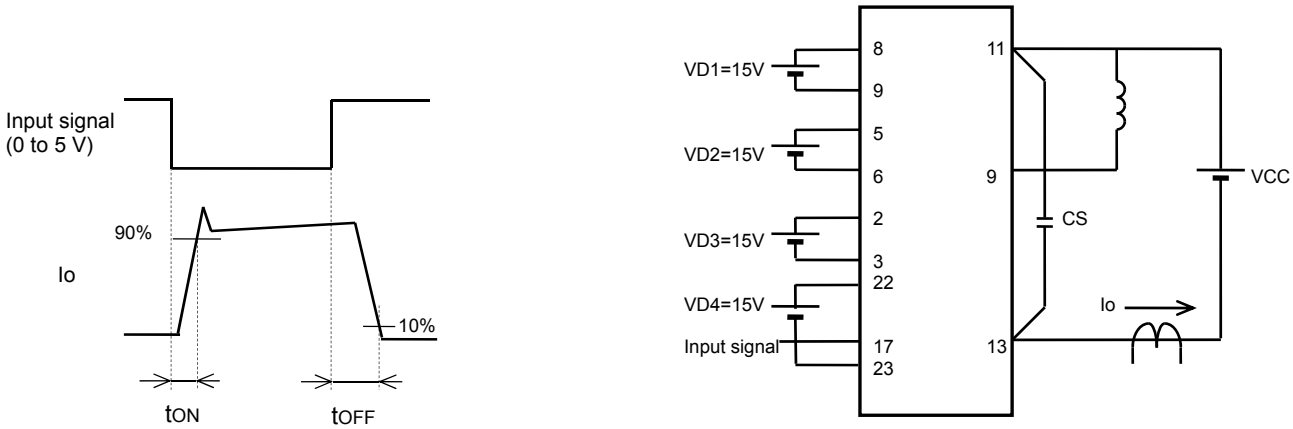


Fig.6

Input / Output Timing Chart

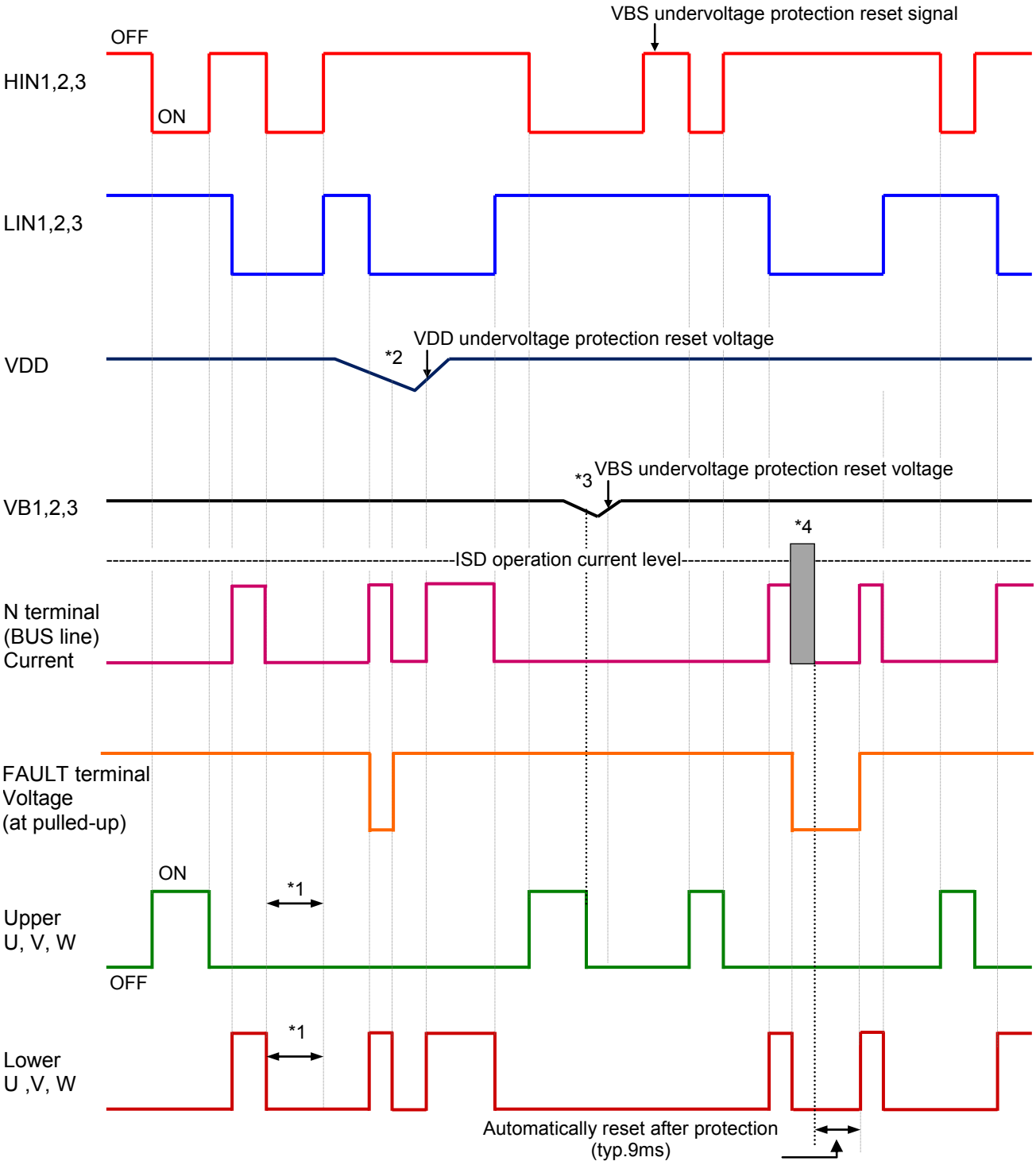


Fig.7

Notes

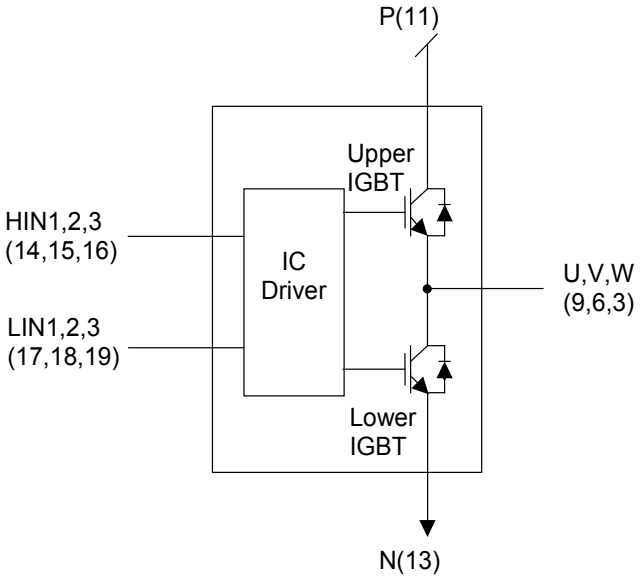
*1 : Diagram shows the prevention of shoot-through via control logic. More deadtime to account for switching delay needs to be added externally.

*2 : If lower V_{DD} drops all gate output signals will go low and cut off all of 6 IGBT outputs. part. When V_{DD} rises the operation will resume immediately.

*3 : When the upper side gate voltage at VB1, VB2 and VB3 drops only the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gat voltage rises.

*4 : In case of over current detection all IGBT's are turned off and the FAULT output is asserted. Normal operation resumes in 6 to 12 ms after the over current condition is removed.

Logic level table



INPUT			OUTPUT			
HIN	LIN	OCP	Upper IGBT	Lower IGBT	U,V,W	FAULT
H	L	OFF	OFF	ON	N	OFF
L	H	OFF	ON	OFF	P	OFF
L	L	OFF	OFF	OFF	High Impedance	OFF
H	H	OFF	OFF	OFF	High Impedance	OFF
X	X	ON	OFF	OFF	High Impedance	ON

Fig. 8

Sample Application Circuit

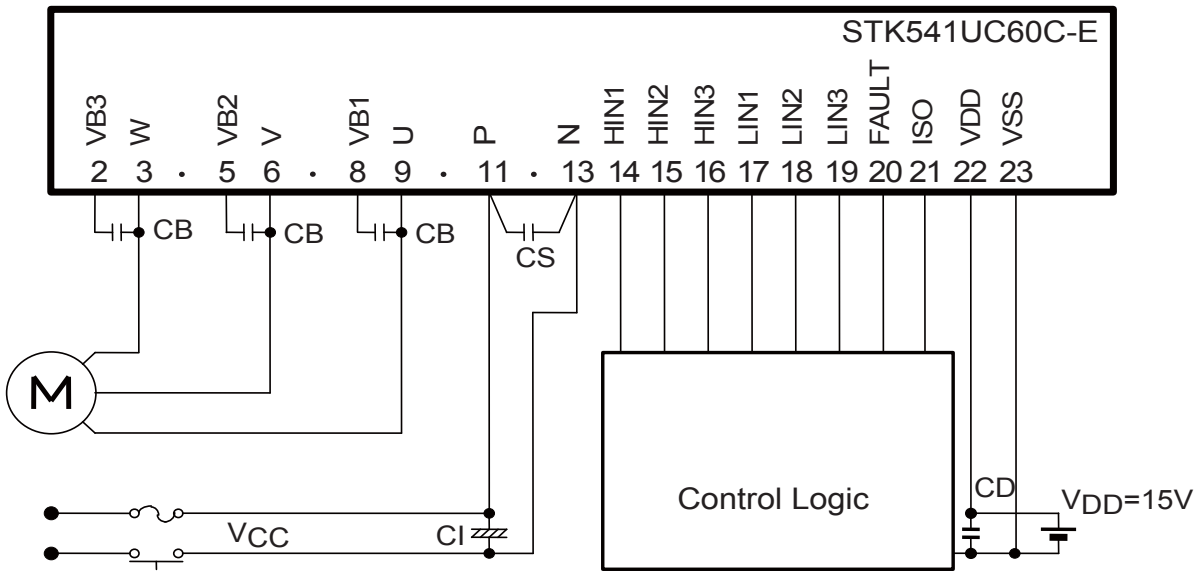


Fig. 9

Recommended Operating Conditions at Ta = 25°C

Item	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{CC}	P to N	0	280	450	V
Pre-driver supply voltage	VD1,2,3	VB1 to U,VB2 to V,VB3 to W	12.5	15	17.5	V
	VD4	V_{DD} to V_{SS} *1	13.5	15	16.5	
PWM frequency	fPWM	–	1	-	20	kHz
Dead time	DT	Turn-off to turn-on	2	-	-	μs
Allowable input pulse width	PWIN	ON and OFF	1	-	-	μs
Tightening torque	–	'M3' type screw	0.6	-	0.9	Nm

*1 : Pre-drive power supply (VD4 = 15 ±1.5 V) must have the capacity of Io = 20 mA (DC), 0.5A (Peak).

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Usage Precaution

1. This IPM includes bootstrap diode and resistors. Therefore, by adding a capacitor “CB”, a high side drive voltage is generated; each phase requires an individual bootstrap capacitor. The recommended value of CB is in the range of 1 to 47 μF, however this value needs to be verified prior to production. If selecting the capacitance more than 47 μF (±20%), connect a resistor (about 20 Ω) in series between each 3-phase upper side power supply terminals (VB1, 2, 3) and each bootstrap capacitor.
   When not using the bootstrap circuit, each upper side pre-drive power supply requires an external independent power supply.

2. It is essential that wiring length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of “CS” is in the range of 0.1 to 10 μF.

3. “ISO” (pin 21) is terminal for current monitor. High current may flow into that course when short-circuiting the “ISO” terminal and “V_{SS}” terminal. Please do not connect them.

4. “FAULT” (pin 20) is open DRAIN output terminal (Active Low). Pull up resistor is recommended more than 6.8 kΩ.

5. Pull up resistor of 100 kΩ is provided internally at the signal input terminals.

6. The over-current protection feature is not intended to protect in exceptional fault condition. An external fuse is recommended for safety.

7. When input pulse width is less than 1.0 μs, an output may not react to the pulse (Both ON signal and OFF signal).

This data shows the example of the application circuit, does not guarantee a design as the mass production set.

The characteristic of PWM switching frequency

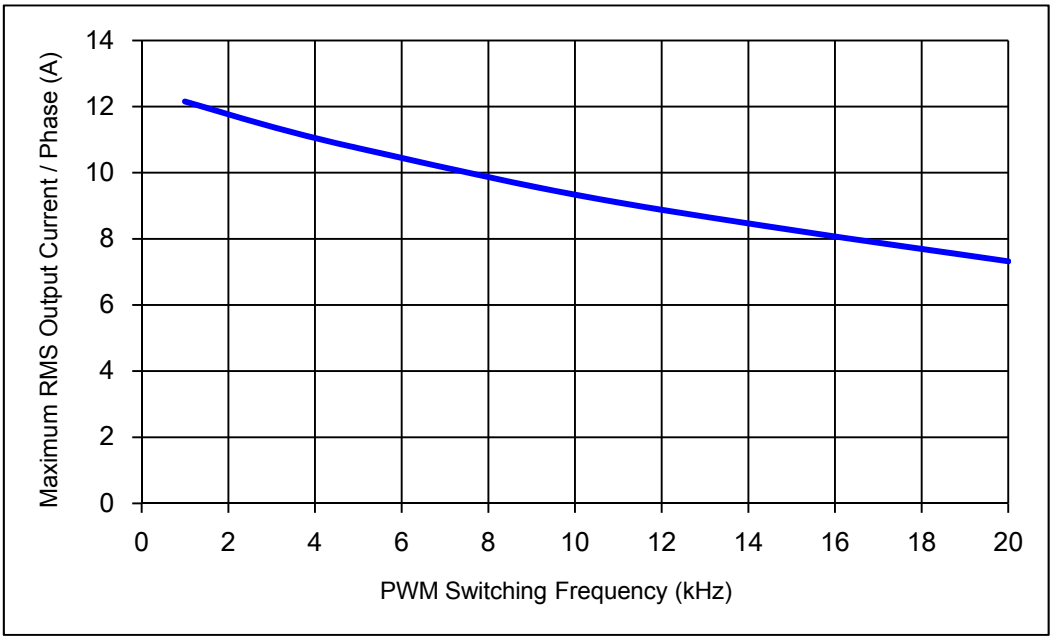


Fig. 10 Maximum sinusoidal phase current as function of switching frequency at Tc = 100°C, V_{CC} = 400 V

CB capacitor value calculation for bootstrap circuit

Calculate conditions

Parameter	Symbol	Value	Unit
Upper side power supply	VBS	15	V
Total gate charge of output power IGBT at 15 V	QG	89	nC
Upper limit power supply low voltage protection	UVLO	12	V
Upper side power dissipation	IDMAX	400	μA
ON time required for CB voltage to fall from 15V to UVLO	TONMAX	-	s

Capacitance calculation formula

Thus, the following formula are true
$VBS \times CB - QG - IDMAX \times TONMAX = UVLO \times CB$
therefore,
$CB = (QG + IDMAX \times TONMAX) / (VBS - UVLO)$

The relationship between TONMAX and CB becomes as follows. CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47 μF, however, this value needs to be verified prior to production.

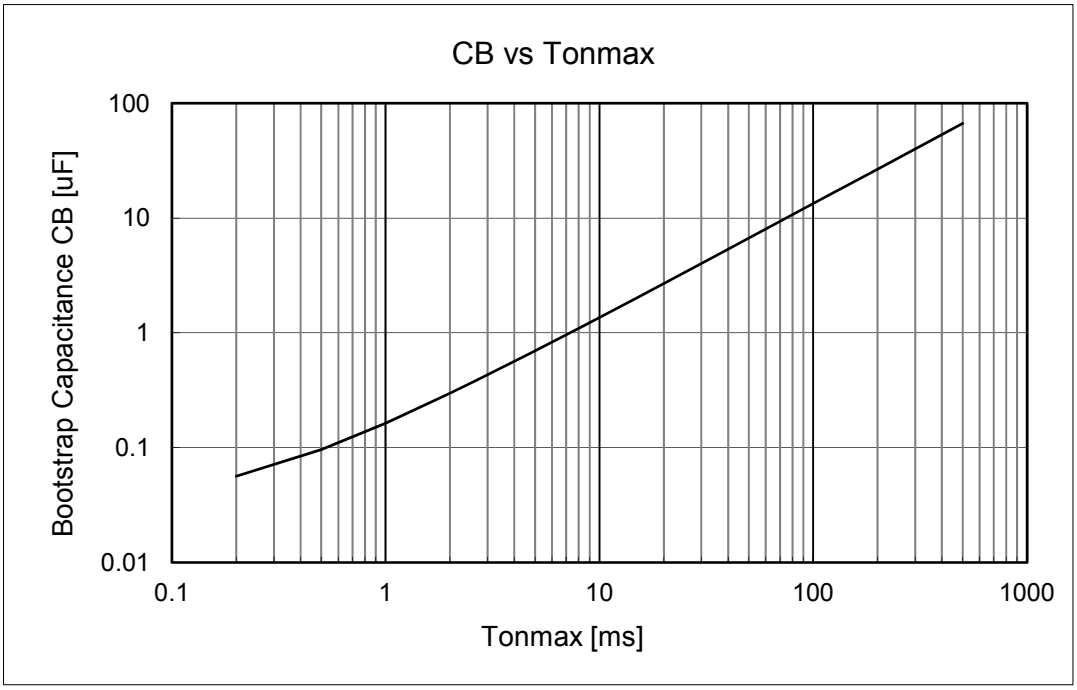
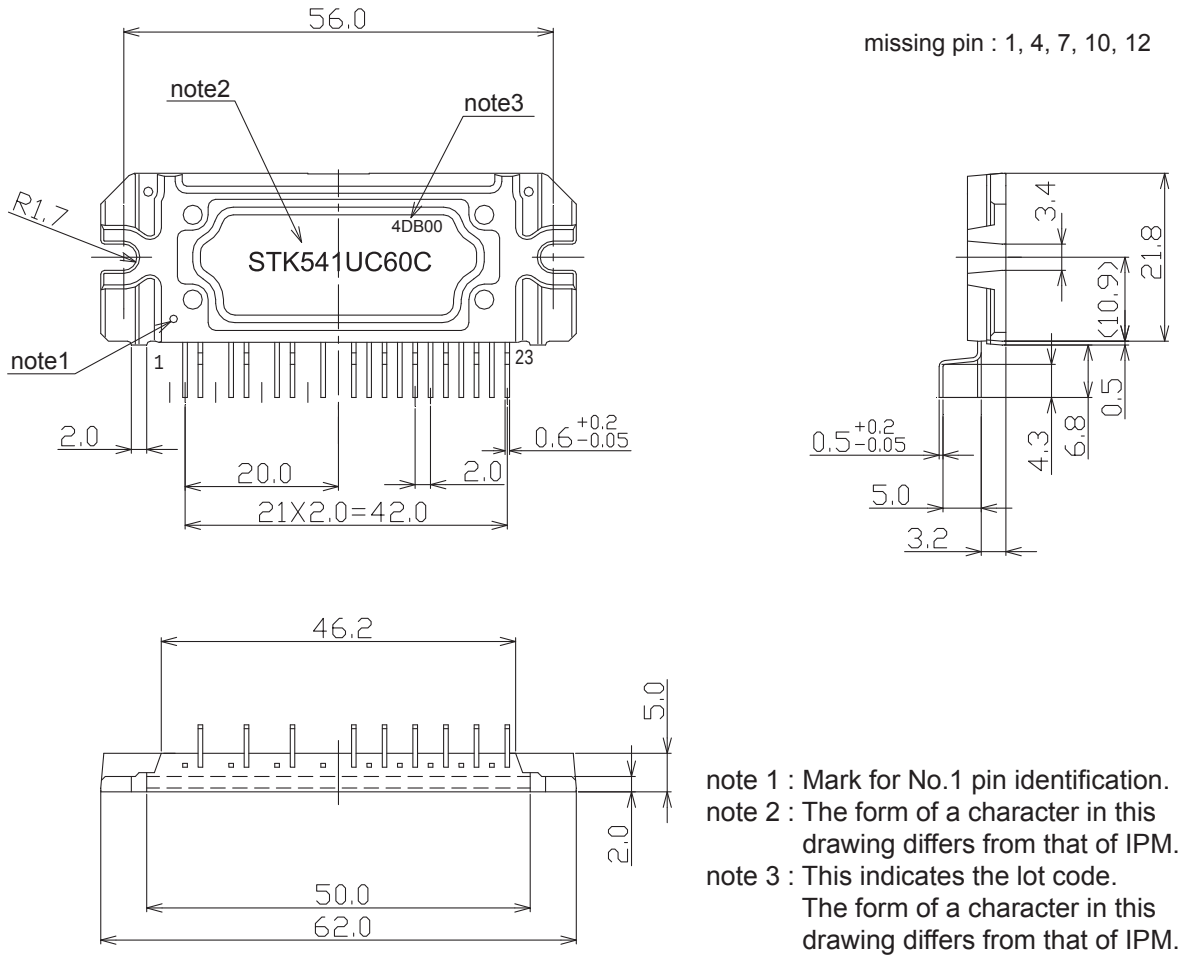


Fig. 11 Tonmax - CB characteristic

PACKAGE DIMENSIONS

unit : mm

The tolerances of length are +/− 0.5 mm unless otherwise specified.



note 1 : Mark for No.1 pin identification.
note 2 : The form of a character in this drawing differs from that of IPM.
note 3 : This indicates the lot code. The form of a character in this drawing differs from that of IPM.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK541UC60C-E	SIP23 56x21.8 (Pb-Free)	8 / Tube