1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-88662	01	X	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		32K X 8 CMOS SRAM	100 ns
02			70 ns
03			55 ns
04			45 ns
05			35 ns
06			25 ns
07			20 ns
08			15 ns
09			12 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual in-line
Y	CQCC1-N32	32	Rectangular leadless chip carrier
Z	CDFP3-F28	28	Flat pack
U	CQCC3-N28	28	Rectangular leadless chip carrier
T	CDFP4-F28	28	Flat pack
N	CDIP3-T28 or GDIP4-T28	28	Dual in-line
M	GDFP2-F28	28	Flat pack

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc 2/
Input voltage range	-0.5 V dc to +6.0 V dc
Ambient storage temperature	-65°C to +150°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+150°C 3/
Power dissipation	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc 2/
Ground voltage (V_{SS})	0 V dc
Input high voltage range (V_{IH})	2.2 V dc to V_{CC} +0.5 V dc
Input low voltage range (V_{IL})	-0.5 V dc to 0.8 V dc
Operating case temperature (T_C)	-55°C to +125°C

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin and will also be listed in MIL-HDBK-103.
2/ All voltages referenced to V_{SS}.
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Output load circuit. The output load circuit shall be as specified on figure 3.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.2.5 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.6 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V, 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input leakage current	I_{LI}	V_{CC} = maximum V_{IN} = GND to V_{CC}	1, 2, 3	All		10	µA
Output leakage current	I_{LO}	V_{CC} = maximum, $\overline{CE} \ge V_{IH}$, V_{OUT} = GND to V_{CC}, $\overline{WE} \le V_{IL}$	1, 2, 3	All		10	µA
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	All		0.4	V
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4 mA V_{IL} = 0.8 V, V_{IH} = 2.2 V	1, 2, 3	All	2.4		V
Operating supply current	I_{CC1}	V_{CC} = 5.5 V, f = f_{MAX} 1/ $\overline{CE}$ = V_{IL}, outputs open, all other inputs at V_{IL}	1, 2, 3	01, 02		105	mA
				03 - 05		150	
				06		160	
				07		170	
				08		180	
				09		190	
Standby power supply current (TTL)	I_{CC2}	$\overline{CE} \ge V_{IH}$, outputs open V_{CC} = 5.5 V	1, 2, 3	01 - 06		35	mA
				07		40	
				08		50	
				09		60	
Standby power supply current (CMOS)	I_{CC3}	$\overline{CE} \ge (V_{CC} - 0.2$ V), f = 0 MHz outputs open, V_{CC} = 5.5 V all other inputs ≤ 0.2 V or $\ge (V_{CC} - 0.2$ V)	1, 2, 3	All		20	mA
Input capacitance	C_I 2/	V_I = 5.0 V or GND f = 1 MHz, T_C = +25°C, see 4.3.1c	4	All		11	pF
Output capacitance	C_O 2/	V_O = 5.0 V or GND f = 1 MHz, T_C = +25°C, see 4.3.1c	4	All		11	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V, $4.5 \text{ V} \le V_{CC} \le 5.5$ V unless otherwise specified 3/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle time	t_{AVAV}		9, 10, 11	01	100		ns
				02	70		
				03	55		
				04	45		
				05	35		
				06	25		
				07	20		
				08	15		
				09	12		
Address access time	t_{AVQV}		9, 10, 11	01		100	ns
				02		70	
				03		55	
				04		45	
				05		35	
				06		25	
				07		20	
				08		15	
				09		12	
Chip-enable access time	t_{ELQV}		9, 10, 11	01		100	ns
				02		70	
				03		55	
				04		45	
				05		35	
				06		25	
				07		20	
				08		15	
				09		12	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V, $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified 3/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output hold from address change	t_{AVQX}		9, 10, 11	01 – 08	3		ns
				09	2		
Output enable to output valid 4/	t_{OLQV}		9, 10, 11	01		60	ns
				02,03		35	
				04,05		20	
				06		15	
				07		10	
				09		8	
				09		6	
Chip select to output in low Z	t_{ELQX} 2/ 5/		9, 10, 11	01 – 08	3		ns
				09	2		
Chip deselect to output in high Z 4/	t_{EHQZ} 2/ 5/		9, 10, 11	01 - 03, 05		35	ns
				04		20	
				06		15	
				07, 08		10	
				09		7	
Output disable to output in high Z 4/	t_{OHQZ} 2/ 5/		9, 10, 11	01 - 03, 05		35	ns
				04		20	
				06		15	
				07, 08		10	
				09		7	
Write enable to output in high Z 4/	t_{WLQZ} 2/ 5/		9, 10, 11	01		50	ns
				02,03,05		35	
				04		20	
				06		15	
				07,08		10	
				09		7	
Output enable to output in low Z	t_{OLQX} 2/ 5/		9, 10, 11	01-04, 06-09	0		ns
				05	2		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V, 4.5 V $\le V_{CC} \le$ 5.5 V unless otherwise specified 3/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data valid to end of write 4/	t_{DVWH} t_{DVEH}		9, 10, 11	01-03	70		ns
				04,05	55		
				06	45		
				07	35		
				08,09	25		
Data hold time	t_{WHDX} t_{EHDX}		9, 10, 11	01-04	3		ns
				05-09	0		
Output active from end of write	t_{WHQX} 2/ 5/		9, 10, 11	01-06	3		ns
				07-09	0		
Write cycle time	t_{AVAV}		9, 10, 11	01	100		ns
				02	70		
				03	55		
				04	45		
				05	35		
				06	25		
				07	20		
				08	15		
				09	12		
Chip select to end of write	t_{ELWH}		9, 10, 11	01	90		ns
				02	60		
				03	50		
				04	40		
				05	30		
				06	20		
				07	15		
				08	12		
				09	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified 3/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address valid to end of write	t_{AVWH}		9, 10, 11	01	85		ns
				02	60		
				03	50		
				04	40		
				05	30		
				06	20		
				07	15		
				08	12		
				09	10		
Address set-up time	t_{AVWL}		9, 10, 11	All	0		ns
Write pulse width	t_{WLWH}		9, 10, 11	01	55		ns
				02	45		
				03	40		
				04	35		
				05	30		
				06	20		
				07	15		
				08	12		
				09	10		
Write recovery time	t_{WHAX} t_{EHAX}		9, 10, 11	01-08	0		ns
				09	2		

1/ $f_{max} = 1/t_{AVAV}$ (minimum)

2/ This parameter tested initially and after any design or process change which could affect this parameter, and therefore shall be guaranteed to the limits specified in table I.

3/ For load circuits see figure 3 and for timing waveforms see figure 4.

4/ This parameter has been tightened for device type 04. Any date code product prior to the date of Revision C of this drawing may not meet this limit. See Revision B for the electrical parameter value that applies to prior date code product.

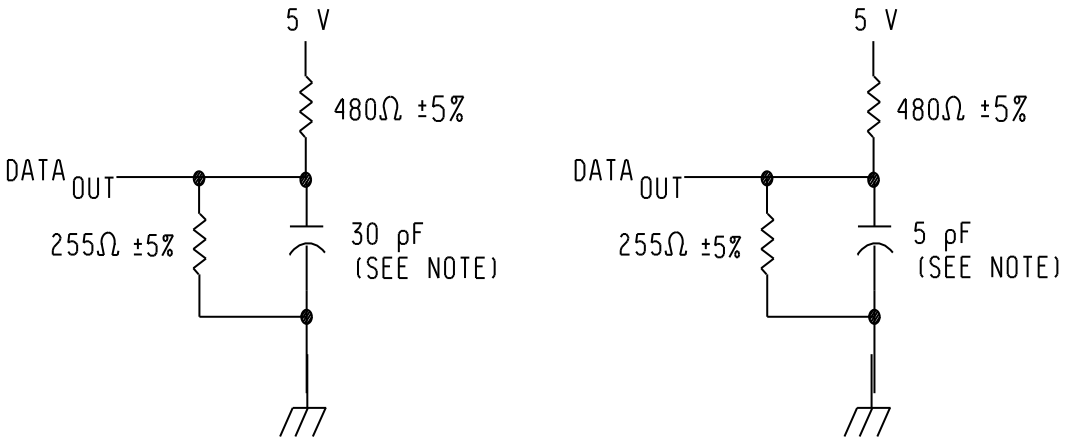
5/ Transition is measured ±500 mV from steady-state voltage.

Device types	All	
Case outlines	X, Z, U, T, N, and M	Y
Terminal number	Terminal symbol	
1	A_{14}	NC
2	A_{12}	A_{14}
3	A_7	A_{12}
4	A_6	A_7
5	A_5	A_6
6	A_4	A_5
7	A_3	A_4
8	A_2	A_3
9	A_1	A_2
10	A_0	A_1
11	I/O_1	A_0
12	I/O_2	NC
13	I/O_3	I/O_1
14	GND	I/O_2
15	I/O_4	I/O_3
16	I/O_5	GND
17	I/O_6	NC
18	I/O_7	I/O_4
19	I/O_8	I/O_5
20	$\overline{CE}$	I/O_6
21	A_{10}	I/O_7
22	$\overline{OE}$	I/O_8
23	A_{11}	$\overline{CE}$
24	A_9	A_{10}
25	A_8	$\overline{OE}$
26	A_{13}	NC
27	$\overline{WE}$	A_{11}
28	V_{CC}	A_9
29	---	A_8
30	---	A_{13}
31	---	$\overline{WE}$
32	---	V_{CC}

FIGURE 1. Terminal connections.

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Function
H	X	X	High Z	Standby (I_{CC2})
≥ V_{CC} -0.2 V	X	X	High Z	Standby (I_{CC3})
L	H	H	High Z	Output disable
L	H	L	Data out	Read
L	L	X	Data in	Write

FIGURE 2. Truth table (unprogrammed).



CIRCUIT A

Output load

CIRCUIT B

(for t_{OLQX}, t_{ELQX}, t_{OHQZ}, t_{WLQZ}, t_{EHQZ}, t_{WHQX})

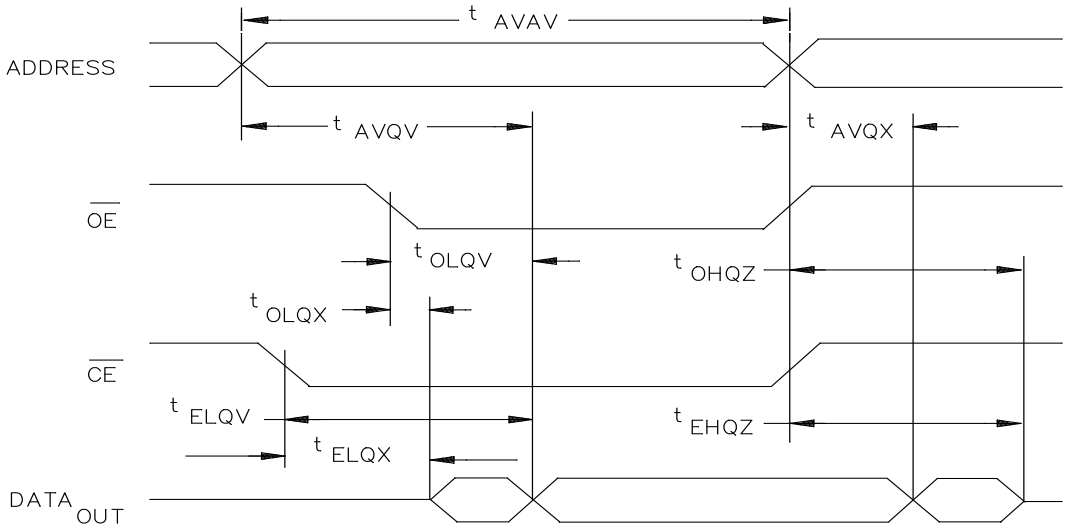
NOTE: Including scope and jig (minimum values).

AC testing conditions

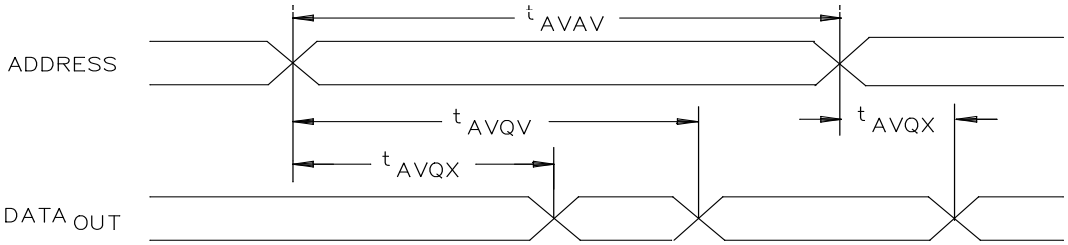
Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuit.

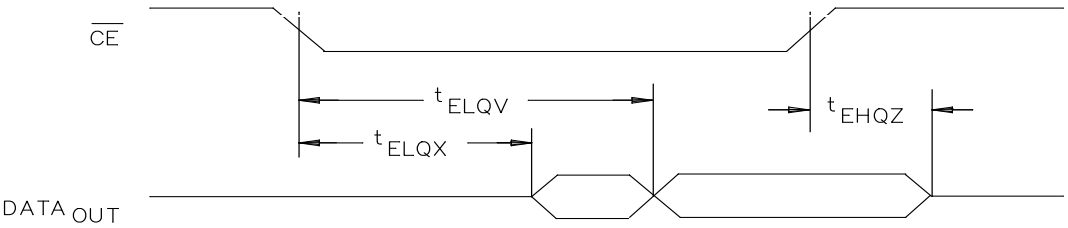
Timing waveform of read cycle no. 1 (1)



Timing waveform of read cycle no. 2 (1, 2, 4)



Timing waveform of read cycle no. 3 (1, 3, 4)

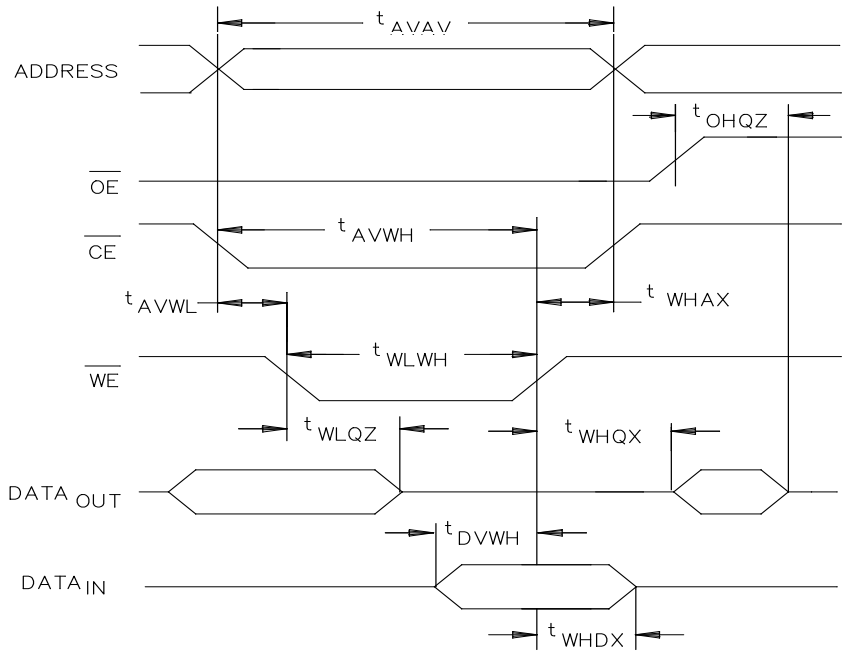


NOTES:

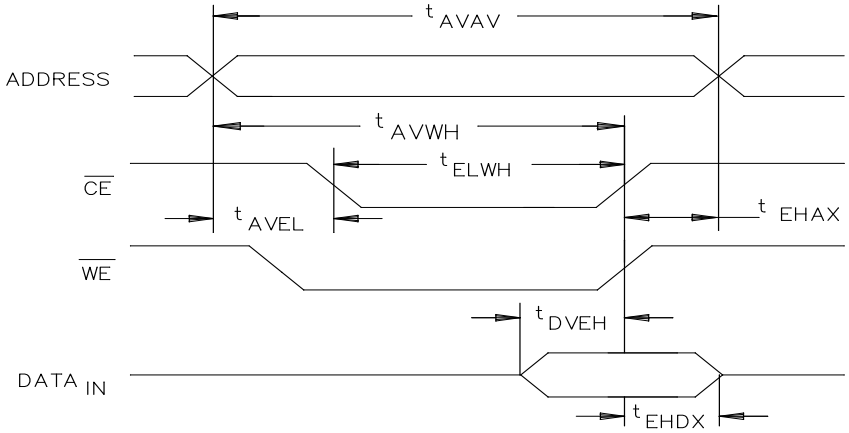
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected. $\overline{CE} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±500 mV from steady state with 5 pF load (including scope and jig).

FIGURE 4. Timing waveforms.

Timing waveform of write cycle no. 1 ($\overline{WE}$ controlled timing) (1,2,3,6,7)



Timing waveform of write cycle no. 2 ($\overline{CE}$ controlled timing) (1,2,3,5)



NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{ELWH} or t_{WLWH}) of a low $\overline{CE}$ and a low $\overline{WE}$.
3. t_{WHAX} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500 mV from steady state with a 5 pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WLWH} or (t_{WLQZ} + t_{DVWH}) to allow the I/O drivers to turn off and data to be placed on the bus for required t_{DVWH}. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WLWH}.

FIGURE 4. Timing waveforms - Continued.

TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10,11
Group A test requirements (method 5005)	1, 2, 3, 4**,7 ,8A,8B, 9, 10,11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

1/ * indicates PDA applies to subgroups 1 and 7.
2/ ** see 4.3.1c.
3/ See 4.3.1d.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures and all input and output terminals tested.

d. Subgroups 7 and 8 tests sufficient to verify the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-01-08

Approved sources of supply for SMD 5962-88662 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8866201XA	0SP21 3DTT2 3/ 0C7V7 3/ 3/	IDT71256S100DB P4C1256-100DWMB MT5C2568CW-100883C QP7C198-100DMB 6206-100/BXAJC EDH8832C-10DMHR
5962-8866201YA	3/ 3DTT2 57300 0C7V7 3/ 3/	IDT71256S100L32B P4C1256-100L32MB MT5C2568ECW-100883C QP7C198-100LMB 6206-100M/BUAJC EDH8832C-10DMHR
5962-8866201ZA	3/ 3/	IDT71256S100EB OW62256CZ3-10
5962-8866201UA	3DTT2 57300 0C7V7 3/ 3/	P4C1256-100L28MB MT5C2568EC-100883C QP7C199-100LMB IDT71256S100L28B EDI8834C100L28B
5962-8866201TA	3DTT2 57300 0C7V7 3/	P4C1256-100FSMB MT5C2568F-100883C QP7C199-100FMB EDI8834C100FB
5962-8866201NA	0SP21 3DTT2 57300 0C7V7 60264 3/	IDT71256S100TDB P4C1256-100DMB MT5C2568C-70883C QP7C199-100DMB MS132K8C100CN EDI8834C100QB
5962-8866201NC	3DTT2	P4C1256-100CMB
5962-8866201MA	3DTT2 0C7V7 3/	P4C1256-100FMB QP7C199-100KMB IDT71256S100XEB
5962-8866202XA	0SP21 3DTT2 0EU86 0C7V7 3/ 3/	IDT71256S70DB P4C1256-70DWMB MT5C2568CW-70883C QP7C198-70DMB 6206-70/BXAJC EDI8834C70CB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8866202YA	3/ 3DTT2 57300 0C7V7 3/ 3/	IDT71256S70L32B P4C1256-70L32MB MT5C2568ECW-70883C QP7C198-70LMB 6206-70M/BUAJC EDI8834C70LB
5962-8866202ZA	3/ 3/	IDT71256S70EB OW62256CZ3-70
5962-8866202UA	3DTT2 57300 0C7V7 3/ 3/	P4C1256-70L28MB MT5C2568EC-70883C QP7C199-70LMB IDT71256S70L28B EDI8834C70L28B
5962-8866202TA	3DTT2 57300 0C7V7 3/	P4C1256-70FSMB MT5C2568F-70883C QP7C199-70FMB EDI8834C70FB
5962-8866202NA	0SP21 3DTT2 0C7V7 60264 57300 3/	IDT71256S70TDB P4C1256-70DMB QP7C199-70DMB MS132K8C70CN MT5C2568C-70883C EDI8834C70QB
5962-8866202NC	3DTT2	P4C1256-70CMB
5962-8866202MA	3DTT2 0C7V7 3/	P4C1256-70FMB QP7C199-70KMB IDT71256S70XEB
5962-8866203XA	0SP21 3DTT2 3/ 0C7V7 3/ 3/ 3/	IDT71256S55DB P4C1256-55DWMB MT5C2568CW-55883C QP7C198-55DMB 6206-55/BXAJC EDI8834C55CB L7C199HMB55
5962-8866203YA	3/ 3DTT2 57300 0C7V7 3/ 3/ 3/ 3/	IDT71256S55L32B P4C1256-55L32MB MT5C2568ECW-55883C QP7C198-55LMB 6206-55M/BUAJC EDI8834C55LB L7C199TMB55 PDM41256S55L32B
5962-8866203ZA	3/ 3/	IDT71256S55EB OW62256CZ3-55

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8866203UA	3DTT2 57300 0C7V7 3/ 3/ 3/ 3/ 3/	P4C1256-55L28MB MT5C2568EC-55883C QP7C199-55LMB IDT71256S55L28B EDI8834C55L28B IDT71256S55L28B PDM41256S55L28B L7C199KMB55
5962-8866203TA	3DTT2 57300 0C7V7 3/ 3/	P4C1256-55FSMB MT5C2568F-55883C QP7C199-55FMB EDI8833C55FB L7C199FMB55
5962-8866203NA	0SP21 3DTT2 0C7V7 60264 57300 3/ 3/ 3/	IDT71256S55TDB P4C1256-55DMB QP7C199-55DMB MS132K8C55CN MT5C2568C-55883C EDI8834C55QB L7C199DMB55 PDM41256S55DB
5962-8866203NC	3DTT2	P4C1256-55CMB
5962-8866203MA	3DTT2 0C7V7 3/ 3/	P4C1256-55FMB QP7C199-55KMB IDT71256S55XEB PDM41256S55EB
5962-8866204XA	0SP21 0C7V7 3/ 3DTT2 3/ 3/ 3/	IDT71256S45DB QP7C198-45DMB MT5C2568CW-45883C P4C1256-45DWMB 6206-45/BXAJC L7C199HMB45 EDI8834C45CB
5962-8866204YA	3/ 3DTT2 57300 0C7V7 3/ 3/ 3/ 3/	IDT71256S45L32B P4C1256-45L32MB MT5C2568ECW-45883C QP7C198-45LMB 6206-45M/BUAJC EDI8834C45LB L7C199TMB45 PDM41256S45L32B
5962-8866204ZA	3/ 3/	IDT71256S45EB OW62256CZ3-45

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8866204UA	3DTT2 57300 0C7V7 3/ 3/ 3/ 3/	P4C1256-45L28MB MT5C2568EC-45883C QP7C199-45LMB IDT71256S45L28B EDI8834C45L28B PDM41256S45L28B L7C199KMB-45
5962-8866204TA	3DTT2 57300 0C7V7 3/ 3/	P4C1256-45FSMB MT5C2568F-45883C QP7C199-45FMB EDI8833C45FB L7C199FMB-45
5962-8866204NA	0SP21 3DTT2 0C7V7 60264 57300 3/ 3/ 3/	IDT71256S45TDB P4C1256-45DMB QP7C199-45DMB MS132K8C45CN MT5C2568C-45883C EDI8834C45QB PDM41256S45DB L7C199DMB-45
5962-8866204NC	3DTT2	P4C1256-45CMB
5962-8866204MA	3DTT2 0C7V7 3/ 3/ 3/	P4C1256-45FMB QP7C199-45KMB IDT71256S45XEB PDM41256S55EB L7C199FMB45
5962-8866205XA	0SP21 3DTT2 3/ 0C7V7 3/	IDT71256S35DB P4C1256-35DWMB MT5C2568CW-35883C QP7C198-35DMB L7C199HMB35
5962-8866205YA	3/ 3DTT2 57300 0C7V7 3/ 3/	IDT71256S35L32B P4C1256-35L32MB MT5C2568ECW-35883C QP7C198-35LMB L7C199TMB35 PDM41256S35L32B
5962-8866205UA	3DTT2 57300 0C7V7 3/ 3/ 3/	P4C1256-35L28MB MT5C2568EC-35883C QP7C199-35LMB IDT71256S35L28B PDM41256S35L28B L7C199KMB35

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8866205TA	3DTT2 57300 0C7V7 3/	P4C1256-35FSMB MT5C2568F-35883C QP7C199-35FMB L7C199FMB35
5962-8866205NA	0SP21 3DTT2 0C7V7 60264 57300 3/ 3/	IDT71256S35TDB P4C1256-35DMB QP7C199-35DMB MS132K8C35CN MT5C2568C-35883C PDM41256S35DB L7C199FMB35
5962-8866205NC	3DTT2	P4C1256-35CMB
5962-8866205MA	3DTT2 0C7V7 3/ 3/	P4C1256-35FMB QP7C199-35KMB IDT71256S35XEB PDM41256S35EB
5962-8866206XA	0SP21 3DTT2 3/ 0C7V7 3/	IDT71256S25DB P4C1256-25DWMB MT5C2568CW-25883C QP7C198-25DMB L7C199HMB25
5962-8866206YA	3/ 3DTT2 57300 0C7V7 3/ 3/	IDT71256S25L32B P4C1256-25L32MB MT5C2568ECW-25883C QP7C198-25LMB L7C199TMB25 PDM41256S25L32B
5962-8866206UA	3DTT2 57300 0C7V7 3/ 3/ 3/	P4C1256-25L28MB MT5C2568EC-25883C QP7C199-25LMB IDT71256S25L28B PDM41256S25L28B L7C199KMB25
5962-8866206TA	3DTT2 57300 0C7V7 3/	P4C1256-25FSMB MT5C2568F-25883C QP7C199-25FMB L7C199FMB25
5962-8866206NA	0SP21 3DTT2 0C7V7 60264 57300 3/ 3/	IDT71256S25TDB P4C1256-25DMB QP7C199-25DMB MS132K8C25CN MT5C2568C-25883C PDM41256S25DB L7C199FMB25

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8866206NC	3DTT2	P4C1256-25CMB
5962-8866206MA	3DTT2 0C7V7 3/ 3/	P4C1256-25FMB QP7C199-25KMB IDT71256S25XEB PDM41256S25EB
5962-8866207XA	3/ 3DTT2 3/ 0C7V7	IDT71256S20DB P4C1256-20DWMB MT5C2568CW-20883C QP7C198-20DMB
5962-8866207YA	3/ 3DTT2 57300 0C7V7 3/	IDT71256S20L32B P4C1256-20L32MB MT5C2568ECW-20883C QP7C198-20LMB PDM41256S20L32B
5962-8866207UA	3DTT2 57300 0C7V7 3/	P4C1256-20L28MB MT5C2568EC-20883C QP7C199-20LMB PDM41256S20L28B
5962-8866207TA	3DTT2 57300 0C7V7	P4C1256-20FSMB MT5C2568F-20883C QP7C199-20FMB
5962-8866207NA	3DTT2 0C7V7 60264 57300 3/	P4C1256-20DMB QP7C199-20DMB MS132K8C20CN MT5C2568C-20883C PDM41256S20DB
5962-8866207NC	3DTT2	P4C1256-20CMB
5962-8866207MA	3DTT2 0C7V7 3/	P4C1256-20FMB QP7C199-20KMB PDM41256S20EB
5962-8866208XA	3DTT2 3/ 0C7V7	P4C1256-15DWMB MT5C2568CW-15883C QP7C198-15DMB
5962-8866208YA	3DTT2 57300 0C7V7 3/	P4C1256-15L32MB MT5C2568ECW-15883C QP7C198-15LMB PDM41256S15L32B
5962-8866208UA	3DTT2 57300 0C7V7 3/	P4C1256-15L28MB MT5C2568EC-15883C QP7C199-15LMB PDM41256S15L28B

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8866208TA	3DTT2 57300 0C7V7	P4C1256-15FSMB MT5C2568F-15883C QP7C199-15FMB
5962-8866208NA	3DTT2 0C7V7 60264 57300 3/	P4C1256-15DMB QP7C199-15DMB MS132K8C15CN MT5C2568C-15883C PDM41256S15DB
5962-8866208MA	3DTT2 0C7V7 3/	P4C1256-15FMB QP7C199-15KMB PDM41256S15EB
5962-8866209XA	3DTT2 3/ 0C7V7	P4C1256-12DWMB MT5C2568CW-12883C QP7C198-12DMB
5962-8866209YA	3DTT2 57300 0C7V7	P4C1256-12L32MB MT5C2568ECW-12883C QP7C198-12LMB
5962-8866209UA	3DTT2 57300 0C7V7	P4C1256-12L28MB MT5C2568EC-12883C QP7C199-12LMB
5962-8866209TA	3DTT2 57300 0C7V7	P4C1256-12FSMB MT5C2568F-12883C QP7C199-12FMB
5962-8866209NA	3DTT2 0C7V7 60264 57300	P4C1256-12DMB QP7C199-12DMB MS132K8C12CN MT5C2568C-12883C
5962-8866209MA	3DTT2 0C7V7	P4C1256-12FMB QP7C199-12KMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
0SP21	Integrated Device Technology, Inc. 6024 Silver Creek Valley Road San Jose, CA 95138
0C7V7	e2v, Inc. dba QP Semiconductor, Inc. 765 Sycamore Drive Milpitas, CA 95035
57300	Micross Components 7725 N. Orange Blossom Trail Orlando, FL 32810-2696
3DTT2	Pyramid Semiconductor Corporation 1249 Reamwood Avenue Sunnyvale, CA 94089
60264	Minco Technology Labs, Inc. 1805 Rutherford Lane Austin, TX 78754-5101

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