Single Chip 96-Port STS-1/STM-0 Cross-Connect

- Provides 13 software configurable delay registers for delay management blocks 1 through 13 to allow arbitrary alignment of egress frames to the device frame timing when DMO is allocated to an egress port or group of ports.

PROTECTION SWITCHING

- Implements Message Assisted Protection Switching (MAPS) enabling hardware based protection decisions and switching.

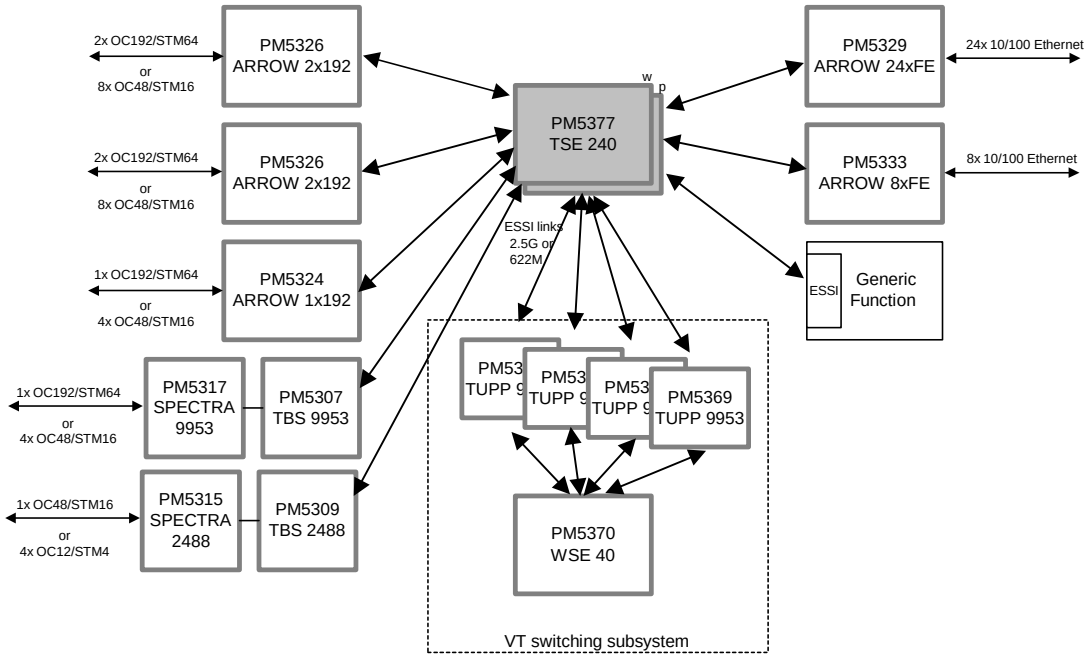
GENERAL

- RASIO 3G high-speed serial ingress and egress links.
- Low-power 1.2 V CMOS core logic with 2.5V digital outputs and 3.3V tolerant 2.5V digital inputs.
- 1152-pin FCBGA, 35 x 35 mm.
- Driven by a 155.52 MHz reference clock.
- Provides a standard five signal IEEE 1149.1 JTAG test port for boundary scan board test.
- Provides a generic 16-bit microprocessor bus interface for configuration, control, and status monitoring.
- 23 W typical power consumption when all features and links @ 2.488 Gbit/s are enabled and active.

APPLICATIONS

- SDH/SONET ADM
- MSPP
- Terminal Multiplexers
- Digital Cross-Connects

TYPICAL APPLICATION



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