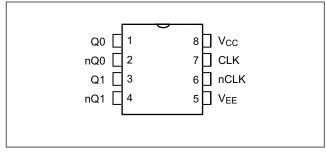


A product Line of Diodes Incorporated

PI6C485311

Pin Configuration



Pin Description

Name	Pin #	Туре	Description	
V _{EE}	5	Р	onnect to Negative power supply	
CLK	7	I_PD	n-inverting differential clock input	
nCLK	6	I_PU	verting differential clock input	
V _{CC}	8	Р	nnect to 3.3V.	
Q ₁ , _n Q ₁	3.4	0	fferential output pair, LVPECL interface level.	
Q ₀ , _n Q ₀	1,2	0	Differential output pair, LVPECL interface level.	

Note:

1. $I = Input, O = Output, P = Power supply connection, I_PD = Input with pull down, I_PU = Input with pull up$

Pin Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
C _{IN}	Input Capacitance				4	pF
R_pullup	Input Pullup Resistance			50		КО
R_pulldown	Input Pulldown Resistance			50		KΩ

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Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Storage Temperature
Supply Voltage to Ground Potential (V _{DD} , V _{DDO})0.5 to +4.6V
Inputs (Referenced to GND)0.5 to V _{DD} +0.5V
Clock Output (Referenced to GND)0.5 to V _{DD} +0.5V
Latch up
ESD Protection (Input) 2000V min (HBM)
Junction Temperature

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
V _{CC}	Power Supply Voltage		3.0	3.3	3.6	V
T _A	Ambient Temperature		-40		85	°C
I _{EE}	Power Supply Current	500 MHz			60	mA

Differential DC Input Characteristics ($T_A = -40^{\circ}C$ to $85^{\circ}C$, $V_{CC} = 3.0V$ to 3.6V unless otherwise stated.)

Symbol	Parar	neter	Conditions	Min.	Тур.	Max.	Units
т	Input High	nCLK	$V_{IN} = V_{CC} = 3.6V$			5	uA
I _{IH}	Current	CLK	$V_{IN} = V_{CC} = 3.6V$			150	uA
IIL	Input Low Current	nCLK	$V_{\rm CC} = 3.6 V, V_{\rm IN} = 0 V$	-150			uA
		CLK	$V_{\rm CC} = 3.6 V, V_{\rm IN} = 0 V$	-5			uA
V _{PP}	Peak-to-peak Voltag	ge		0.15		1.3	V
V _{CMR}	Common Mode Input Voltage ^(1, 2)			V _{EE} +0.5		V _{CC} - 0.85V	V

Notes:

For single ended applications, the maximum input voltage for CLK and nCLK is V_{CC}+0.3V 1

Common mode voltage is defined as VIH. 2.

LVPECL DC Characteristics

 $(T_A = -40^{\circ}C \text{ to } 85^{\circ}C, V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}, R_I = 50\Omega \text{ to } V_{CC} - 2 \text{ V}, \text{ unless otherwise stated below.})$

Symbol	Parameter		Conditions	Min.	Тур.	Max.	Units
т	Input High	nCLK	$V_{IN} = V_{CC} = 3.6V$			5	
I _{IH}	Current	CLK	$V_{\rm IN} = V_{\rm CC} = 3.6 V$			150	۸
I	Input Low	nCLK	$V_{\rm CC} = 3.6 V, V_{\rm IN} = 0 V$	-150			μΑ
I_{IL}	Current	CLK	$V_{CC} = 3.6 V, V_{IN} = 0 V$	-5			
V _{PP}	Peak-to-peak Voltage			0.3		1	
V _{CMR}	Common Mode Input Voltage; Note ^(1,2)			V _{EE} +1.5		V _{CC}	
V _{OH}	Output High Volta	age		V _{CC} -1.4		V _{CC} -0.9	V
V _{OL}	Output Low Voltage			V _{CC} -2.0		V _{CC} -1.6	
VSWING	Peak-to-peak Out	put Voltage Swing		0.6		1.0	

Notes:

For single ended applications, the maximum input voltage for PCLK and _nPCLK is V_{CC}+0.3V. 1.

2. Common mode voltage is defined as VIH.





AC Characteristics⁽¹⁾ ($T_A = -40^{\circ}$ C to 85°C, $V_{CC} = 3.0$ V to 3.6V, $R_L = 50\Omega$ to $V_{CC} - 2$ V, unless otherwise stated below.)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
f _{max}	Output Frequency				800	MHz
t _{Pd}	Propagation Delay ⁽²⁾		1.0		2.0	ns
Tsk(o)	Output-to-output Skew ⁽³⁾				100	
Tsk(pp)	Part-to-part Skew ⁽⁴⁾				150	ps
t _r /t _f	Output Rise/Fall time	20% - 80%	75		300	
odc	Output duty cycle		40		60	%

Notes:

Measured from the $V_{CC}/2$ of the input to the differential output crossing point 2.

Defined as skew between outputs at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point. 3

4. Defined as skew between outputs on different parts operating at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.

All parameters are measured at 500MHz unless noted otherwise 1.





Applications Information

Wiring the differential input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R1/R2 = 0.609.

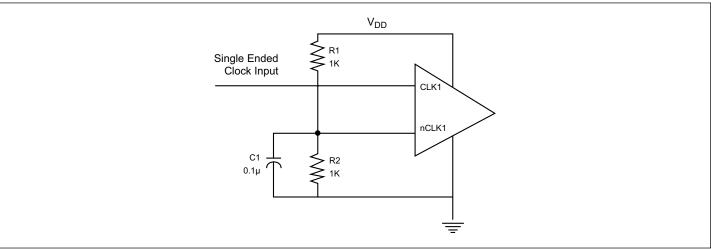


Figure 1: Single-ended Signal Driving Differential Input

Part Marking W Package



A: Die Rev YW: Year & Workweek 1st X: Assembly Code 2nd X: Fab Code

U Package

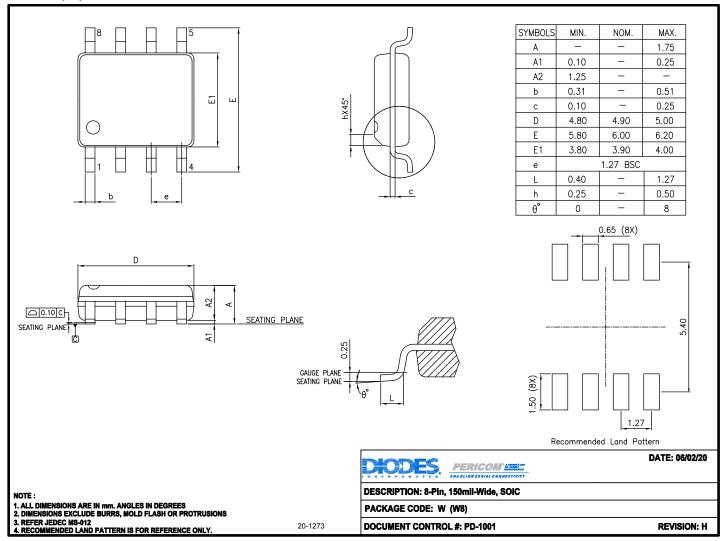
Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.





Packaging Mechanical

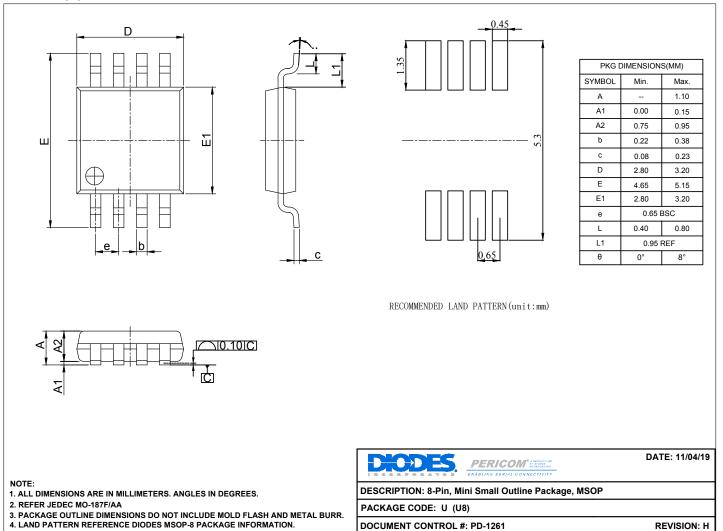
8-SOIC (W)







8-MSOP(U)



For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Description
PI6C485311WEX	W	8-pin, 150mil-Wide (SOIC)
PI6C485311UEX	U	8-pin, Mini Small Outline Package (MSOP)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.

2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

4. E = Pb-free and Green

5. X suffix = Tape/Reel

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