ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate−Source Breakdown Voltage (I_G = 1.0 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	30	−	Vdc
Gate Reverse Current		I_{GSS}			
(V_{GS} = 15 Vdc, V_{DS} = 0, T_A = 25°C)			−	1.0	nAdc
(V_{GS} = 15 Vdc, V_{DS} = 0, T_A = 100°C)			−	0.20	μAdc
Gate−Source Cutoff Voltage		$V_{GS(off)}$			Vdc
(V_{DS} = 15 Vdc, I_D = 10 nAdc)	MMBF4391LT1		−4.0	−10	
	MMBF4392LT1		−2.0	−5.0	
	MMBF4393LT1		−0.5	−3.0	
Off−State Drain Current		$I_{D(off)}$			
(V_{DS} = 15 Vdc, V_{GS} = −12 Vdc)			−	1.0	nAdc
(V_{DS} = 15 Vdc, V_{GS} = −12 Vdc, T_A = 100°C)			−	1.0	μAdc
ON CHARACTERISTICS					
Zero−Gate−Voltage Drain Current		I_{DSS}			mAdc
(V_{DS} = 15 Vdc, V_{GS} = 0)	MMBF4391LT1		50	150	
	MMBF4392LT1		25	75	
	MMBF4393LT1		5.0	30	
Drain−Source On−Voltage		$V_{DS(on)}$			Vdc
(I_D = 12 mAdc, V_{GS} = 0)	MMBF4391LT1		−	0.4	
(I_D = 6.0 mAdc, V_{GS} = 0)	MMBF4392LT1		−	0.4	
(I_D = 3.0 mAdc, V_{GS} = 0)	MMBF4393LT1		−	0.4	
Static Drain−Source On−Resistance		$r_{DS(on)}$			Ω
(I_D = 1.0 mAdc, V_{GS} = 0)	MMBF4391LT1		−	30	
	MMBF4392LT1		−	60	
	MMBF4393LT1		−	100	
SMALL−SIGNAL CHARACTERISTICS					
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	−	14	pF
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 12 Vdc, f = 1.0 MHz)		C_{rss}	−	3.5	pF

ORDERING INFORMATION

Device	Marking	Package	Shipping†
MMBF4391LT1	6J	SOT−23	3000 / Tape & Reel
MMBF4391LT1G	6J	SOT−23 (Pb−Free)	
MMBF4392LT1	6K	SOT−23	
MMBF4392LT1G	6K	SOT−23 (Pb−Free)	
MMBF4393LT1	6G	SOT−23	
MMBF4393LT1G	6G	SOT−23 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

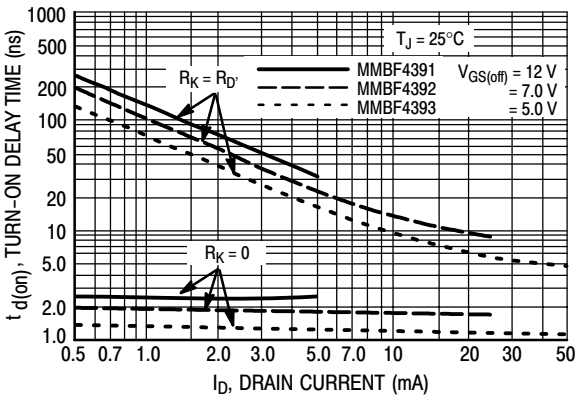


Figure 1. Turn−On Delay Time

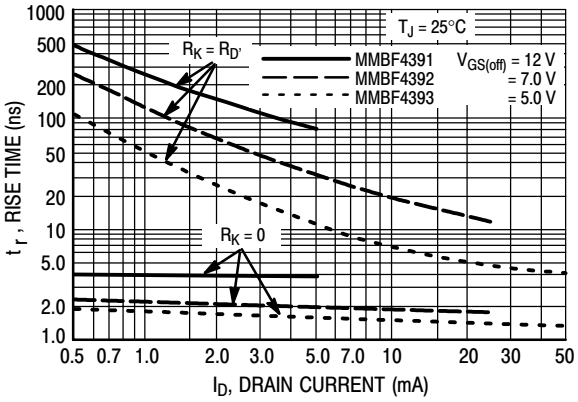


Figure 2. Rise Time

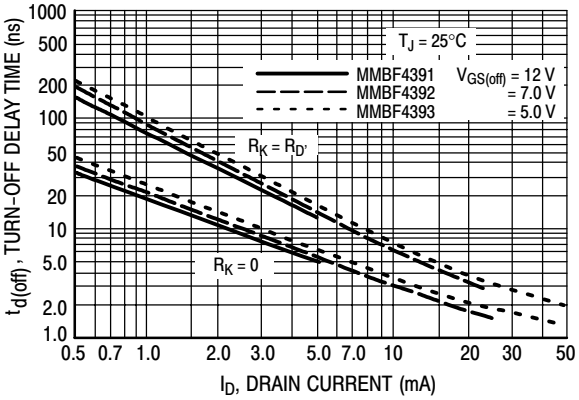


Figure 3. Turn−Off Delay Time

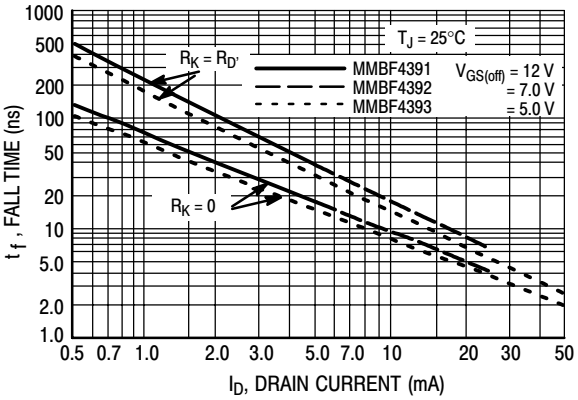


Figure 4. Fall Time

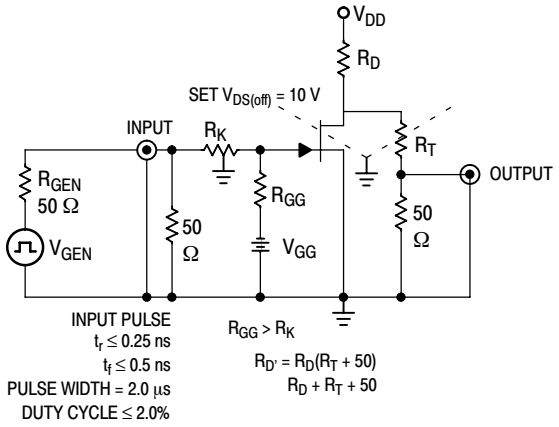


Figure 5. Switching Time Test Circuit

NOTE 1

The switching characteristics shown above were measured using a test circuit similar to Figure 5. At the beginning of the switching interval, the gate voltage is at Gate Supply Voltage ($-V_{GG}$). The Drain−Source Voltage (V_{DS}) is slightly lower than Drain Supply Voltage (V_{DD}) due to the voltage divider. Thus Reverse Transfer Capacitance (C_{rss}) of Gate−Drain Capacitance (C_{gd}) is charged to $V_{GG} + V_{DS}$.

During the turn−on interval, Gate−Source Capacitance (C_{gs}) discharges through the series combination of R_{Gen} and R_K. C_{gd} must discharge to $V_{DS(on)}$ through R_G and R_K in series with the parallel combination of effective load impedance (R'_D) and Drain−Source Resistance (r_{DS}). During the turn−off, this charge flow is reversed.

Predicting turn−on time is somewhat difficult as the channel resistance r_{DS} is a function of the gate−source voltage. While C_{gs} discharges, V_{GS} approaches zero and r_{DS} decreases. Since C_{gd} discharges through r_{DS}, turn−on time is non−linear. During turn−off, the situation is reversed with r_{DS} increasing as C_{gd} charges.

The above switching curves show two impedance conditions; 1) R_K is equal to $R_{D'}$ which simulates the switching behavior of cascaded stages where the driving source impedance is normally the load impedance of the previous stage, and 2) R_K = 0 (low impedance) the driving source impedance is that of the generator.

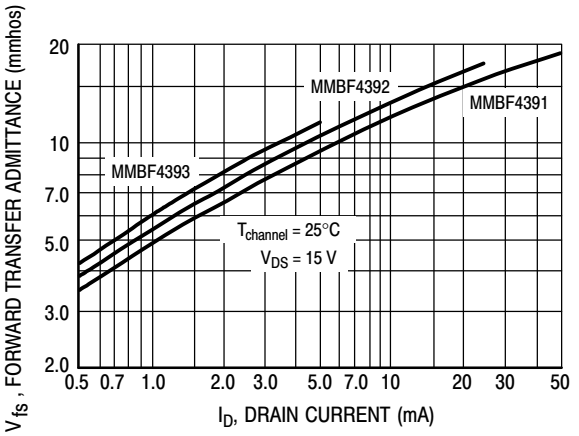


Figure 6. Typical Forward Transfer Admittance

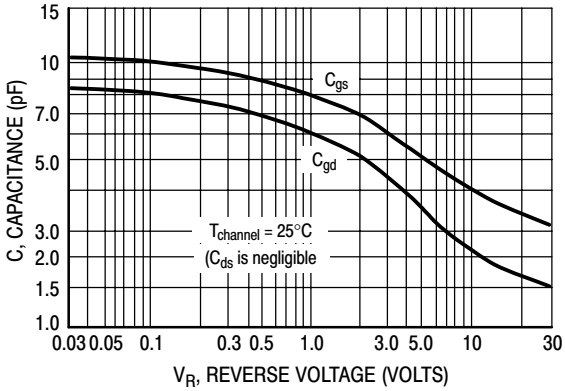


Figure 7. Typical Capacitance

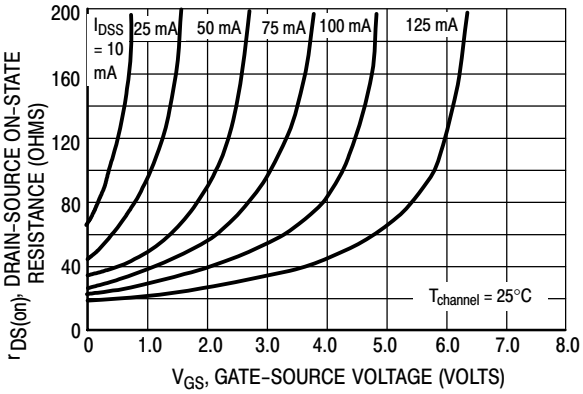


Figure 8. Effect of Gate−Source Voltage on Drain−Source Resistance

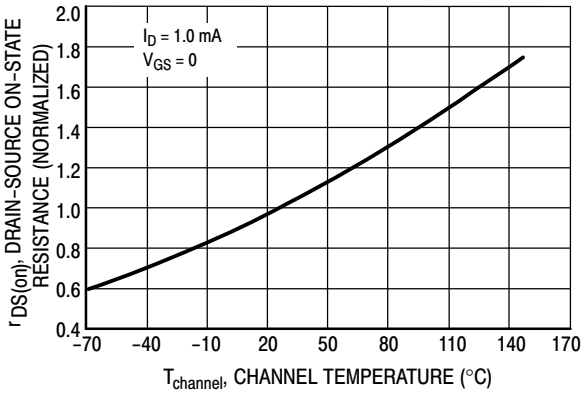


Figure 9. Effect of Temperature on Drain−Source On−State Resistance

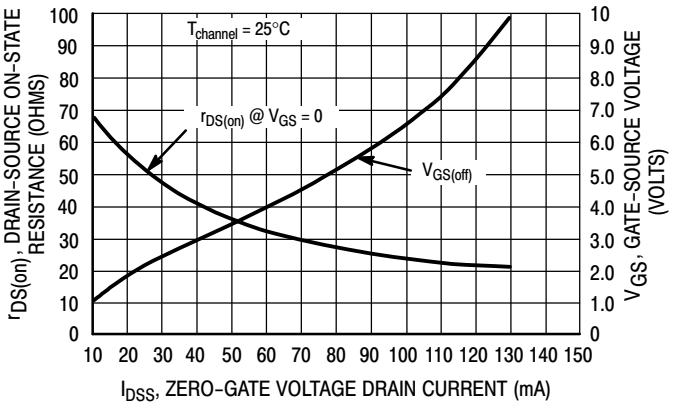


Figure 10. Effect of I_{DSS} on Drain−Source Resistance and Gate−Source Voltage

NOTE 2

The Zero−Gate−Voltage Drain Current (I_{DSS}) is the principle determinant of other J−FET characteristics. Figure 10 shows the relationship of Gate−Source Off Voltage ($V_{GS(off)}$) and Drain−Source On Resistance ($r_{DS(on)}$) to I_{DSS}. Most of the devices will be within ±10% of the values shown in Figure 10. This data will be useful in predicting the characteristic variations for a given part number.

For example:

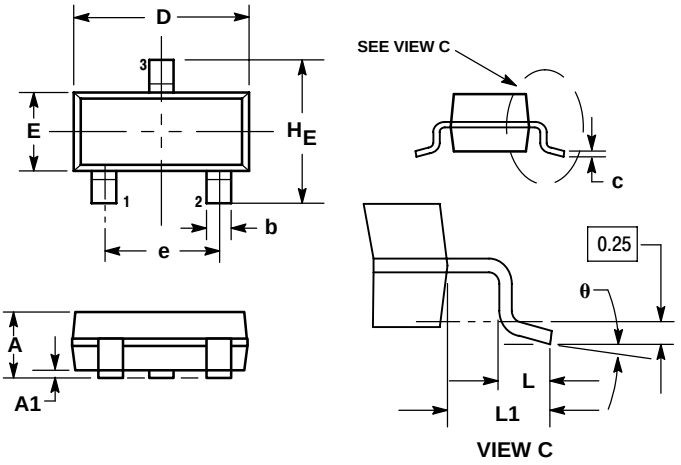
Unknown

$r_{DS(on)}$ and V_{GS} range for an MMBF4392

The electrical characteristics table indicates that an MMBF4392 has an I_{DSS} range of 25 to 75 mA. Figure 10 shows $r_{DS(on)}$ = 52 Ω for I_{DSS} = 25 mA and 30 Ω for I_{DSS} = 75 mA. The corresponding V_{GS} values are 2.2 V and 4.8 V.

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AN

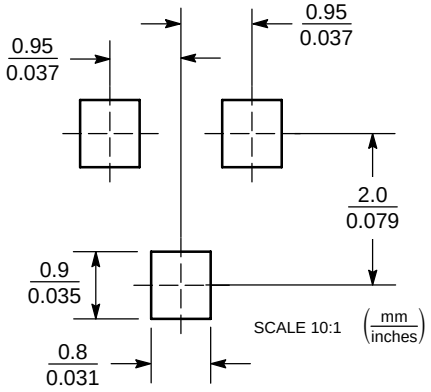


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01 THRU −07 AND −09 OBSOLETE, NEW STANDARD 318−08.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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