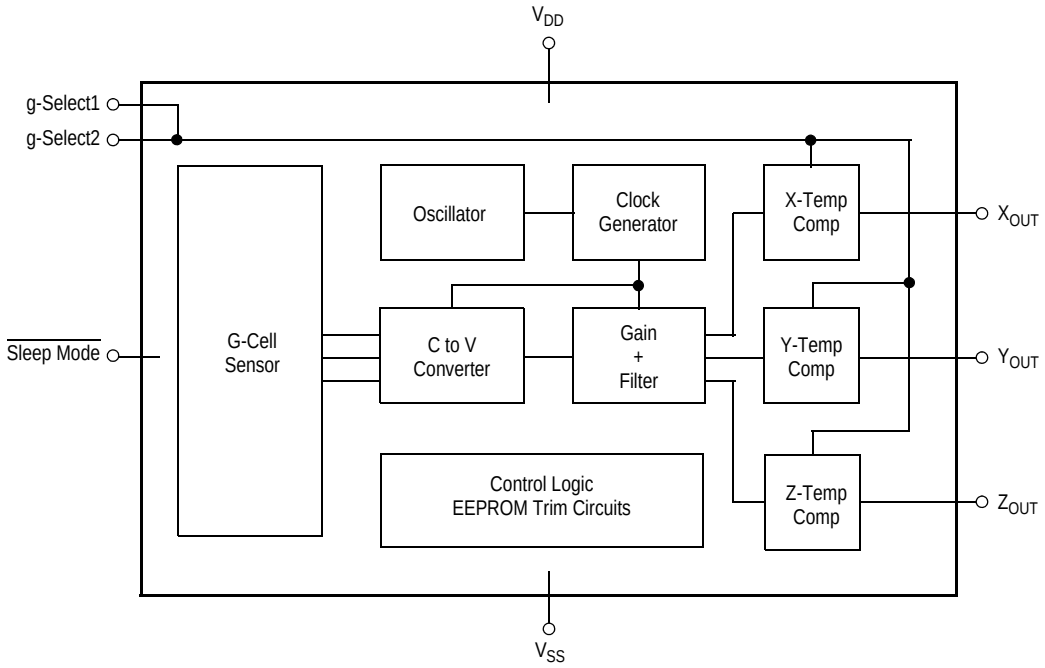


Figure 2. Simplified Accelerometer Functional Block Diagram

Table 1. Maximum Ratings
(Maximum ratings are the limits to which the device can be exposed without causing permanent damage.)

Rating	Symbol	Value	Unit
Maximum Acceleration (all axis)	g_{max}	±5000	g
Supply Voltage	V_{DD}	–0.3 to +3.6	V
Drop Test(1)	D_{drop}	1.8	m
Storage Temperature Range	T_{stg}	–40 to +125	°C

1. Dropped onto concrete surface from any axis.

ELECTRO STATIC DISCHARGE (ESD)

WARNING: This device is sensitive to electrostatic discharge.

Although the Freescale accelerometer contains internal 2000 volts ESD protection circuitry, extra precaution must be taken by the user to protect the chip from ESD. A charge of over 2000 volts can accumulate on the human body or associated test equipment. A charge of this magnitude can alter the performance or cause failure of the chip. When handling the accelerometer, proper ESD precautions should be followed to avoid exposing the device to discharges which may be detrimental to its performance.

Table 2. Operating Characteristics

Unless otherwise noted: –40°C ≤ T_A ≤ 105°C, 2.2 V ≤ V_{DD} ≤ 3.6 V, Acceleration = 0g, Loaded output[1]

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Range[2]					
Supply Voltage[3]	V_{DD}	2.2	3.3	3.6	V
Supply Current	I_{DD}	—	500	800	μA
Supply Current at Sleep Mode[4]	I_{DD}	—	3.0	10	μA
Operating Temperature Range	T_A	–40	—	+105	°C
Acceleration Range, X-Axis, Y-Axis, Z-Axis					
g-Select1 & 2: 00	g_{FS}	—	±1.5	—	g
g-Select1 & 2: 10	g_{FS}	—	±2.0	—	g
g-Select1 & 2: 01	g_{FS}	—	±4.0	—	g
g-Select1 & 2: 11	g_{FS}	—	±6.0	—	g
Output Signal					
Zero-g (T_A = 25°C, V_{DD} = 3.3 V)[5]	V_{OFF}	1.485	1.65	1.815	V
Zero-g[4]	V_{OFF}, T_A				mg/°C
X-axis		±2.6[6]	±0.6	±3.8[7]	
Y-axis		±5.8[6]	±5.8	±5.9[7]	
Z-axis		±1.0[6]	±0.8	±0.8[7]	
Sensitivity (T_A = 25°C, V_{DD} = 3.3 V)					
1.5g	$S_{1.5g}$	740	800	860	mV/g
2g	S_{2g}	555	600	645	mV/g
4g	S_{4g}	277.5	300	322.5	mV/g
6g	S_{6g}	185	200	215	mV/g
Sensitivity[4]	S,T_A				%/°C
X-axis		±0.02[6]	±0.02	±0.02[7]	
Y-axis		±0.01[6]	±0.01	±0.01[7]	
Z-axis		±0.01[6]	±0.00	±0.01[7]	
Bandwidth Response					
XY	f_{-3dB}	—	350	—	Hz
Z	f_{-3dB}	—	150	—	Hz
Noise					
RMS (0.1 Hz – 1 kHz)[4]	n_{RMS}	—	4.7	—	mVrms
Power Spectral Density RMS (0.1 Hz – 1 kHz)[4]	n_{PSD}	—	350	—	$\mu g/\sqrt{Hz}$
Control Timing					
Power-Up Response Time[8]	$t_{RESPONSE}$	—	1.0	2.0	ms
Enable Response Time[9]	t_{ENABLE}	—	0.5	2.0	ms
Sensing Element Resonant Frequency					
XY	f_{GCELL}	—	6.0	—	kHz
Z	f_{GCELL}	—	3.4	—	kHz
Internal Sampling Frequency	f_{CLK}	—	11	—	kHz
Output Stage Performance			—		
Full-Scale Output Range (I_{OUT} = 30 μA)	V_{FSO}	V_{SS}+0.25		V_{DD}–0.25	V
Nonlinearity, X_{OUT}, Y_{OUT}, Z_{OUT}	NL_{OUT}	–1.0	—	+1.0	%FSO
Cross-Axis Sensitivity[10]	$V_{XY, XZ, YZ}$	—	—	5.0	%
Ratiometric Error[11]	error	—	—	—	%

1. For a loaded output, the measurements are observed after an RC filter consisting of a 1.0 kΩ resistor and a 0.1 μF capacitor on V_{DD}-GND.
2. These limits define the range of operation for which the part will meet specification.
3. Within the supply range of 2.2 and 3.6 V, the device operates as a fully calibrated linear accelerometer. Beyond these supply limits the device may operate as a linear device but is not guaranteed to be in calibration.
4. This value is measured with g-Select in 1.5g mode.
5. The device can measure both + and – acceleration. With no input acceleration the output is at midsupply. For positive acceleration the output will increase above V_{DD}/2. For negative acceleration, the output will decrease below V_{DD}/2.
6. These values represent the 10th percentile, not the minimum.
7. These values represent the 90th percentile, not the maximum.
8. The response time between 10% of full scale V_{DD} input voltage and 90% of the final operating output voltage.
9. The response time between 10% of full scale Sleep Mode input voltage and 90% of the final operating output voltage.
10. A measure of the device's ability to reject an acceleration applied 90 from the true axis of sensitivity.
11. Zero-g offset ratiometric error can be typically >20% at V_{DD} = 2.2 V. Sensitivity ratiometric error can be typically >3% at V_{DD} = 2.2. Consult factory for additional information

PRINCIPLE OF OPERATION

The Freescale accelerometer is a surface-micromachined integrated-circuit accelerometer.

The device consists of two surface micromachined capacitive sensing cells (g-cell) and a signal conditioning ASIC contained in a single integrated circuit package. The sensing elements are sealed hermetically at the wafer level using a bulk micromachined cap wafer.

The g-cell is a mechanical structure formed from semiconductor materials (polysilicon) using semiconductor processes (masking and etching). It can be modeled as a set of beams attached to a movable central mass that move between fixed beams. The movable beams can be deflected from their rest position by subjecting the system to an acceleration (Figure 3).

As the beams attached to the central mass move, the distance from them to the fixed beams on one side will increase by the same amount that the distance to the fixed beams on the other side decreases. The change in distance is a measure of acceleration.

The g-cell beams form two back-to-back capacitors (Figure 3). As the center beam moves with acceleration, the distance between the beams changes and each capacitor's value will change, ($C = A\varepsilon/D$). Where A is the area of the beam, ε is the dielectric constant, and D is the distance between the beams.

The ASIC uses switched capacitor techniques to measure the g-cell capacitors and extract the acceleration data from the difference between the two capacitors. The ASIC also signal conditions and filters (switched capacitor) the signal, providing a high level output voltage that is ratiometric and proportional to acceleration.

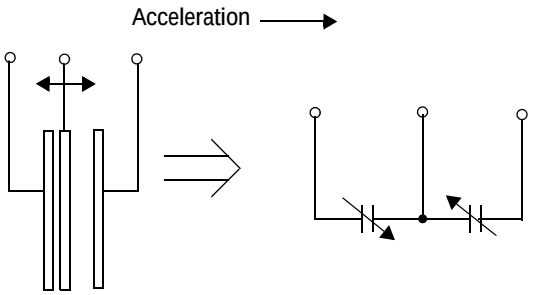


Figure 3. Simplified Transducer Physical Model

SPECIAL FEATURES

g-Select

The g-Select feature allows for the selection among 4 sensitivities present in the device. Depending on the logic input placed on pins 1 and 2, the device internal gain will be changed allowing it to function with a 1.5g, 2g, 4g, or 6g sensitivity (Table 3). This feature is ideal when a product has applications requiring different sensitivities for optimum performance. The sensitivity can be changed at anytime during the operation of the product. The g-Select1 and g-Select2 pins can be left unconnected for applications requiring only a 1.5g sensitivity as the device has an internal pull-down to keep it at that sensitivity (800mV/g).

Table 3. g-Select Pin Descriptions

g-Select2	g-Select1	g-Range	Sensitivity
0	0	1.5g	800 mV/g
0	1	2g	600 mV/g
1	0	4g	300 mV/g
1	1	6g	200 mV/g

Sleep Mode

The 3 axis accelerometer provides a Sleep Mode that is ideal for battery operated products. When Sleep Mode is active, the device outputs are turned off, providing significant reduction of operating current. A low input signal on pin 12 (Sleep Mode) will place the device in this mode and reduce the current to 3 μA typ. For lower power consumption, it is recommended to set g-Select1 and g-Select2 to 1.5g mode. By placing a high input signal on pin 12, the device will resume to normal mode of operation.

Filtering

The 3 axis accelerometer contains onboard single-pole switched capacitor filters. Because the filter is realized using switched capacitor techniques, there is no requirement for external passive components (resistors and capacitors) to set the cut-off frequency.

Ratiometricity

Ratiometricity simply means the output offset voltage and sensitivity will scale linearly with applied supply voltage. That is, as supply voltage is increased, the sensitivity and offset increase linearly; as supply voltage decreases, offset and sensitivity decrease linearly. This is a key feature when interfacing to a microcontroller or an A/D converter because it provides system level cancellation of supply induced errors in the analog to digital conversion process. Offset ratiometric error can be typically >20% at V_{DD} = 2.2 V. Sensitivity ratiometric error can be typically >3% at V_{DD} = 2.2 V. Consult factory for additional information.

Pin Descriptions

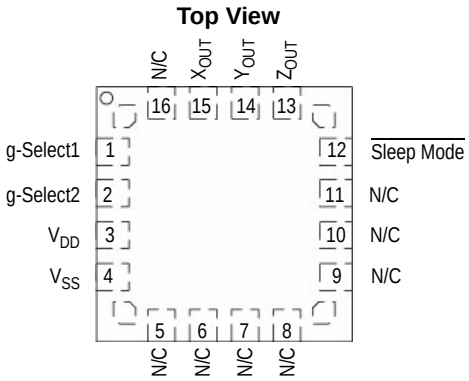


Figure 4. Pinout Description

Table 4. Pin Descriptions

Pin No.	Pin Name	Description
1	g-Select1	Logic input pin to select g level.
2	g-Select2	Logic input pin to select g level.
3	V_{DD}	Power Supply Input
4	V_{SS}	Power Supply Ground
5 - 7	N/C	No internal connection. Leave unconnected.
8 - 11	N/C	Unused for factory trim. Leave unconnected.
12	$\overline{\text{Sleep Mode}}$	Logic input pin to enable product or Sleep Mode.
13	Z_{OUT}	Z direction output voltage.
14	Y_{OUT}	Y direction output voltage.
15	X_{OUT}	X direction output voltage.
16	N/C	No internal connection. Leave unconnected.

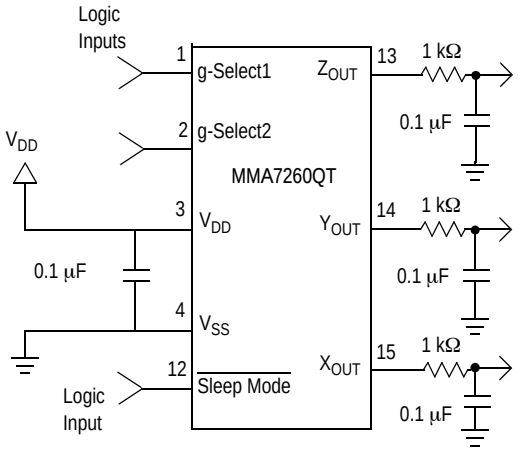


Figure 5. Accelerometer with Recommended Connection Diagram

PCB Layout

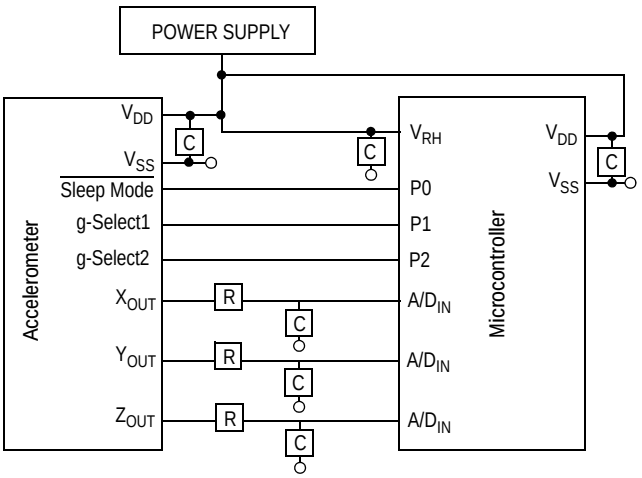
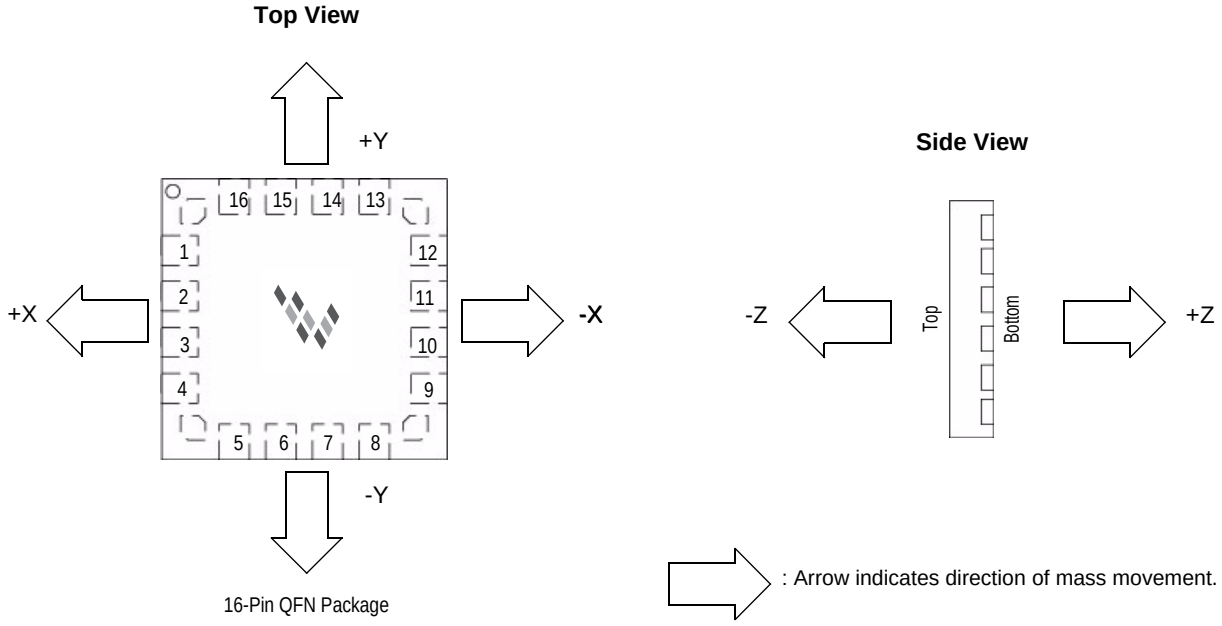


Figure 6. Recommended PCB Layout for Interfacing Accelerometer to Microcontroller

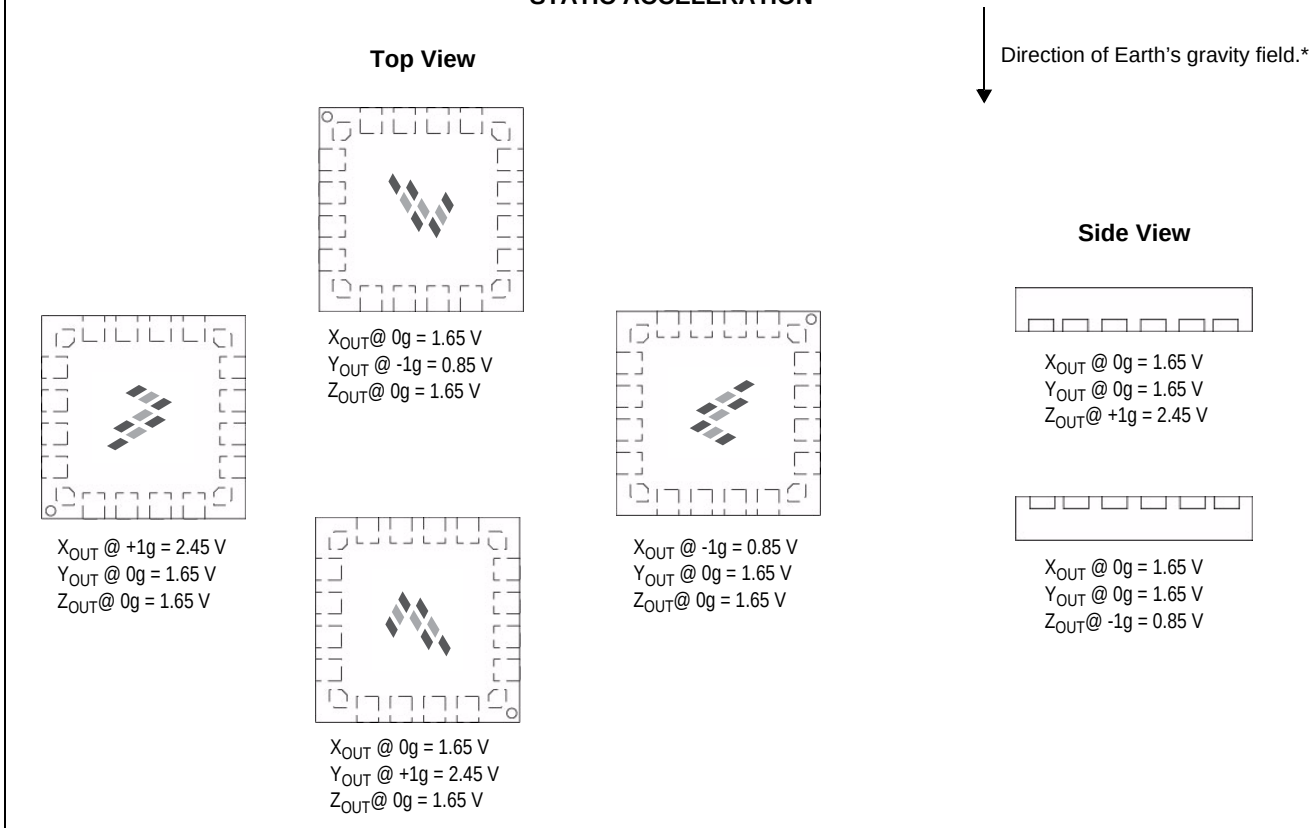
NOTES:

1. Verify V_{DD} line has the ability to reach 2.2 V in ≤ 0.1 ms as measured on the device at the V_{DD} pin. Rise times greater than this most likely will prevent start up operation.
2. Physical coupling distance of the accelerometer to the microcontroller should be minimal.
3. The flag underneath the package is internally connected to ground. It is not recommended for the flag to be soldered down.
4. Place a ground plane beneath the accelerometer to reduce noise, the ground plane should be attached to all of the open ended terminals shown in Figure 6.
5. Use an RC filter with 1.0 kΩ and 0.1 µF on the outputs of the accelerometer to minimize clock noise (from the switched capacitor filter circuit).
6. PCB layout of power and ground should not couple power supply noise.
7. Accelerometer and microcontroller should not be a high current path.
8. A/D sampling rate and any external power supply switching frequency should be selected such that they do not interfere with the internal accelerometer sampling frequency (11 kHz for the sampling frequency). This will prevent aliasing errors.
9. PCB layout should not run traces or vias under the QFN part. This could lead to ground shorting to the accelerometer flag.

DYNAMIC ACCELERATION



STATIC ACCELERATION



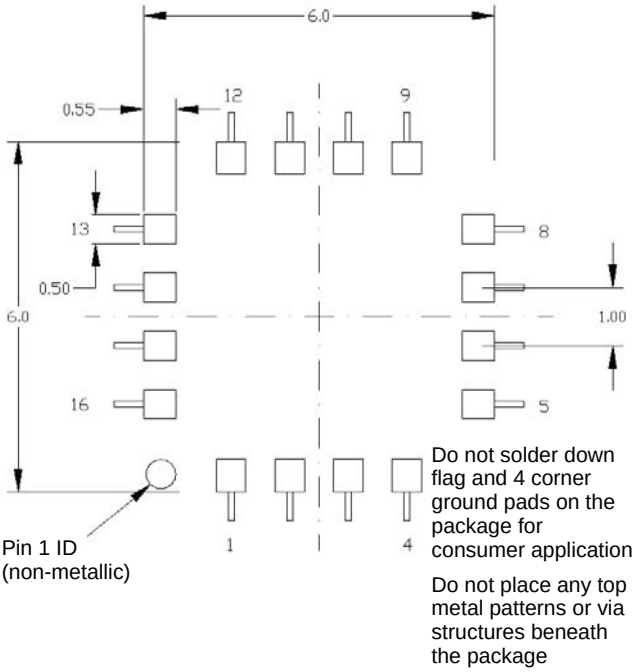
* When positioned as shown, the Earth's gravity will result in a positive 1g output.

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package.

With the correct footprint, the packages will self-align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.

The flag underneath the package is internally connected to ground. It is not recommended for the flag to be soldered down.



Note: The die pad (flag) is not generally recommended to be soldered down for consumer product application. All dimensions are in mm.

Figure 7. PCB Footprint for 16-Lead QFN, 6x6 mm for Consumer Grade Products and Applications

PCB DESIGN GUIDELINES

The following are the recommended guidelines to follow for mounting QFN sensors for either automotive or consumer applications.

1. NSMD (Non Solder Mask Defined) is shown in Figure 8.
2. Solder mask opening = PCB land pad +0.1 mm.
3. Stencil aperture size = PCB land pad –0.025mm, as shown in Figure 9 with a 6mil stencil.
4. Do not place insertion components or vias at a distance less than 2mm from the package land area.
5. Signal trace connected to pads should be as symmetric as possible. Put dummy traces if there is NC pads, in order to have same length of exposed trace for all pads. Signal traces with 0.1mm width and min. 0.5mm length for all PCB land pad near package are recommended as shown in Figure 8 and Figure 9. Wider trace can be continued after the 0.5mm zone.
6. Use a standard pick and place process and equipment (no hand soldering process).
7. It is recommended to use a cleanable solder paste with an additional cleaning step after SMT mount
8. It is recommended to avoid screwing down the PCB to fix it into an enclosure since this may cause the PCB to bend.
9. PC boards should be rated for multiple reflow of lead-free conditions with 260°C maximum temperature.

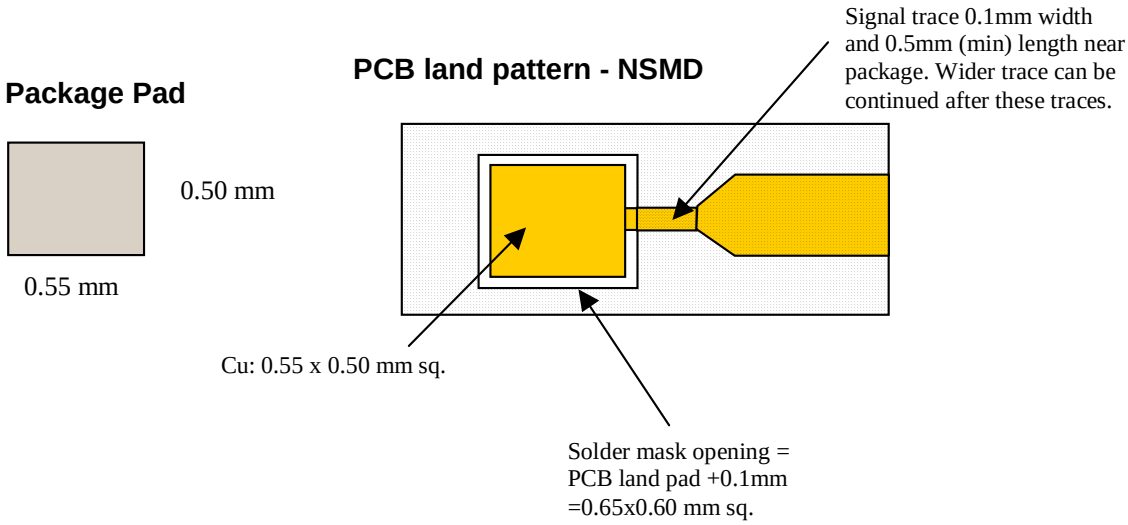


Figure 8. NSMD Solder Mask Design Guidelines

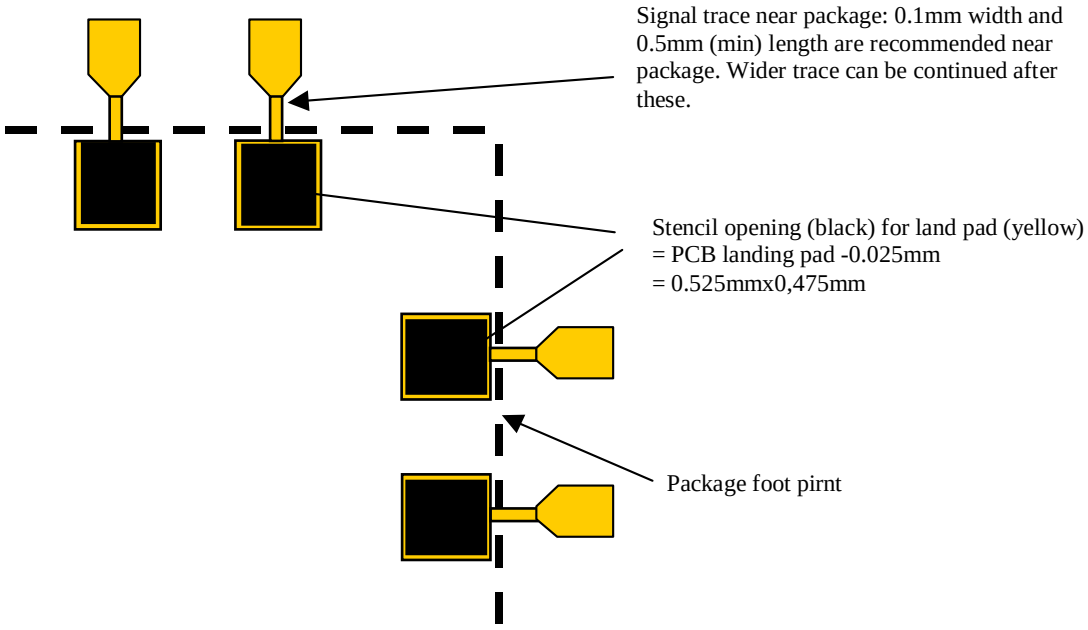
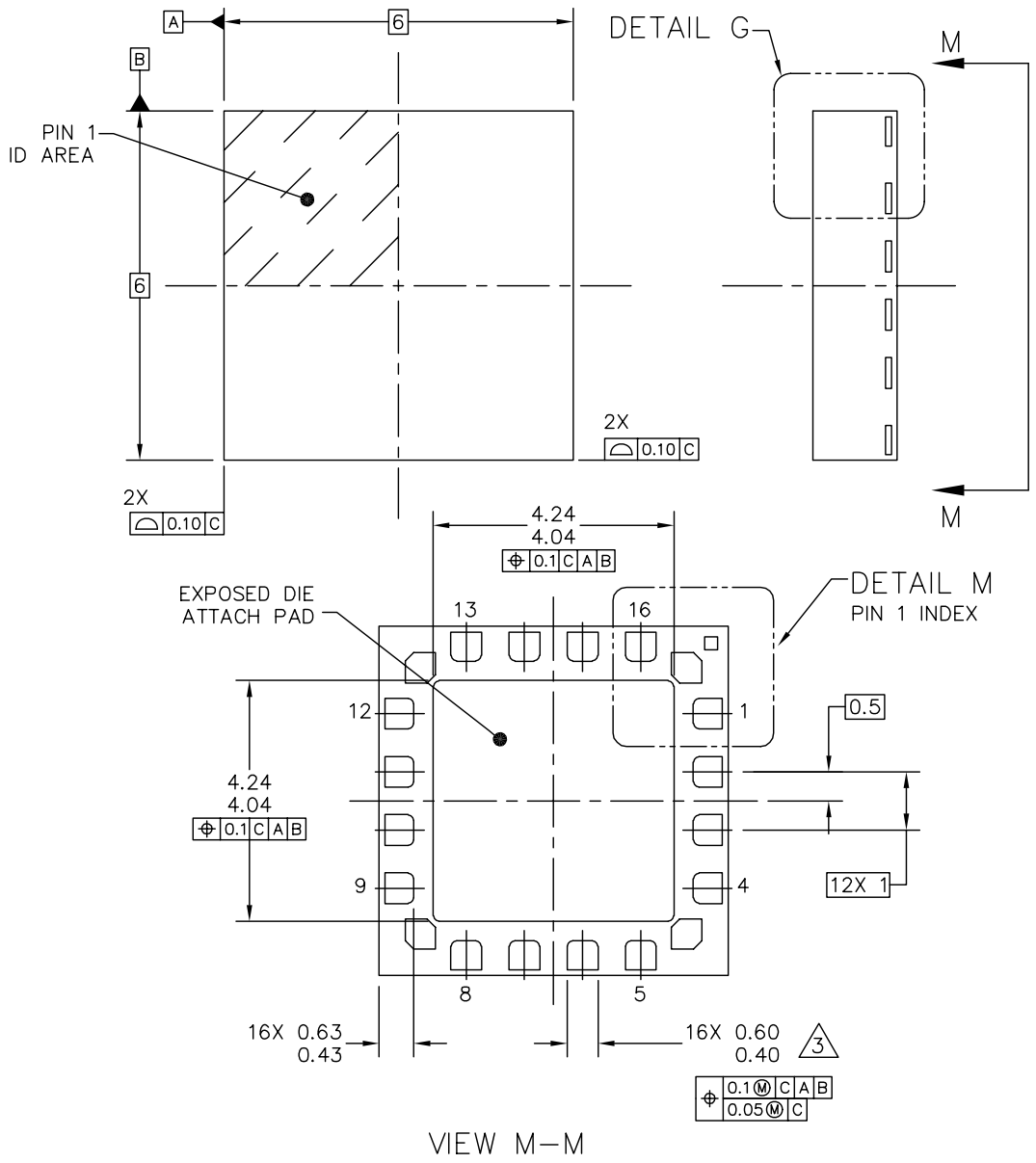


Figure 9. Stencil Design Guidelines

PACKAGE DIMENSIONS



VIEW M–M

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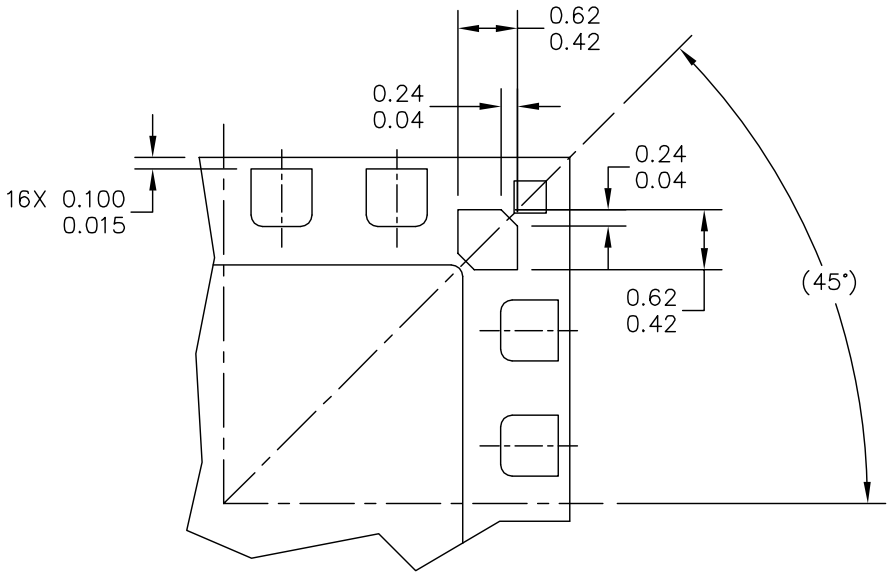
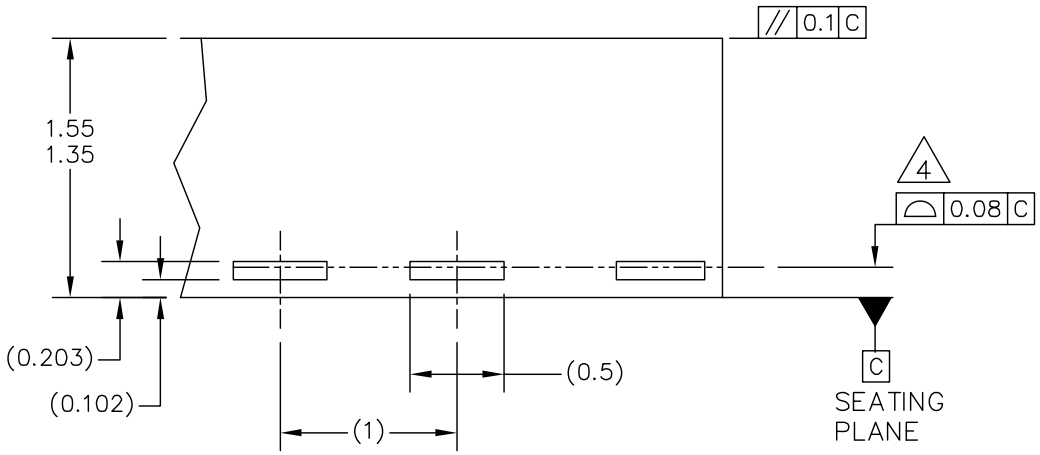
	CASE NUMBER: 1622–02	27 SEP 2006
	STANDARD: NON–JEDEC	

CASE 1622-02
ISSUE B
16-LEAD QFN

PACKAGE DIMENSIONS



DETAIL M



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PACKAGE DIMENSIONS

NOTES:

1. ALL DIMENSIONS ARE IN MILLMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THIS DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25MM AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG, TERMINALS AND CORNER PADS.
5. RADIUS ON TERMINAL IS OPTIONAL.
6. MINIMUM METAL GAP SHOULD BE 0.2MM EXCEPT GAP BETWEEN CORNER PADS AND THE EXPOSED HEAT SLUG.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

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CASE 1622-02
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