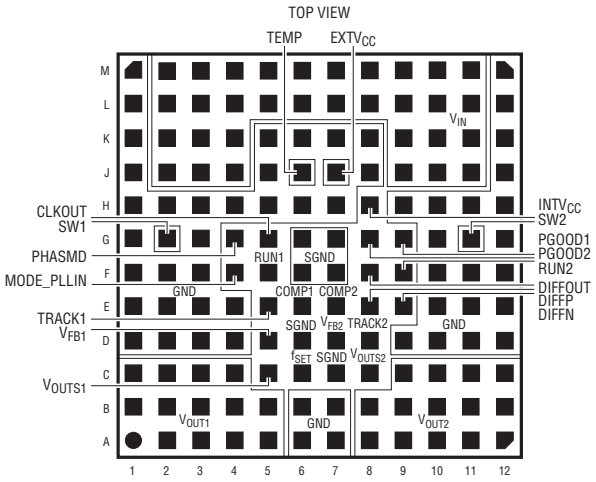
ABSOLUTE MAXIMUM RATINGS (Note 1)

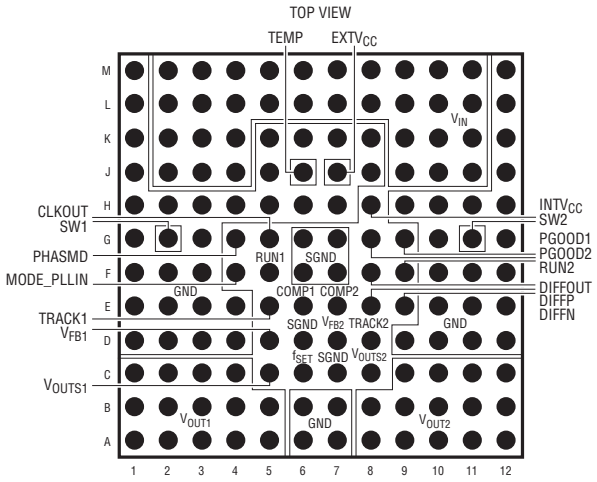
V_{IN} (Note 8).....–0.3V to 18V
V_{SW1}, V_{SW2}.....–1V to 18V
PGOOD1, PGOOD2, RUN1, RUN2,
$INTV_{CC}$, $EXTV_{CC}$ ..... –0.3V to 6V
MODE_PLLIN, f_{SET}, TRACK1, TRACK2,
DIFFOUT, PHASMD .....–0.3V to $INTV_{CC}$
V_{OUT1}, V_{OUT2}, V_{OUTS1}, V_{OUTS2} ..... –0.3V to 6V
DIFFP, DIFFN .....–0.3V to $INTV_{CC}$
COMP1, COMP2, V_{FB1}, V_{FB2} (Note 6)..... –0.3V to 2.7V
$INTV_{CC}$ Peak Output Current.....100mA
Internal Operating Temperature Range (Note 2)
E- and I-Grade ..... –40°C to 125°C
MP-Grade ..... –55°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Package Body Temperature
(Mount on Top Side of PCB Only) ..... 245°C

PIN CONFIGURATION



LGA PACKAGE
144-LEAD (15mm × 15mm × 4.41mm)

T_{JMAX} = 125°C, θ_{JA} = 7°C/W, $\theta_{JCbottom}$ = 1.5°C/W,
θ_{JCtop} = 3.7°C/W, θ_{JB} + θ_{BA} ≅ 7°C/W
θ VALUES DEFINED PER JESD 51-12
WEIGHT = 3.037g



BGA PACKAGE
144-LEAD (15mm × 15mm × 5.01mm)

T_{JMAX} = 125°C, θ_{JA} = 7°C/W, $\theta_{JCbottom}$ = 1.5°C/W,
θ_{JCtop} = 3.7°C/W, θ_{JB} + θ_{BA} ≅ 7°C/W
θ VALUES DEFINED PER JESD 51-12
WEIGHT = 3.232g

ORDER INFORMATION

http://www.linear.com/product/LTM4620A#orderinfo

PART NUMBER	PAD OR BALL FINISH	PART MARKING* DEVICE	PART MARKING* FINISH CODE	PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 2)
LTM4620AEV#PBF	Au (RoHS)	LTM4620AV	e4	LGA	3	–40°C to 125°C
LTM4620AIV#PBF	Au (RoHS)	LTM4620AV	e4	LGA	3	–40°C to 125°C
LTM4620AEY#PBF	SAC305 (RoHS)	LTM4620AY	e1	BGA	3	–40°C to 125°C
LTM4620AIY#PBF	SAC305 (RoHS)	LTM4620AY	e1	BGA	3	–40°C to 125°C
LTM4620AIY	SnPb (63/37)	LTM4620AY	e0	BGA	3	–40°C to 125°C
LTM4620AMPY#PBF	SAC305 (RoHS)	LTM4620AY	e1	BGA	3	–55°C to 125°C
LTM4620AMPY	SnPb (63/37)	LTM4620AY	e0	BGA	3	–55°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Terminal Finish Part Marking:
  www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures:
  www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings:
  www.linear.com/packaging

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel. T_A = 25°C (Note 2), V_{IN} = 12V and V_{RUN1}, V_{RUN2} at 5V unless otherwise noted. Per the typical application in Figure 26.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage		●	4.5		16	V
V_{OUT}	Output Voltage	(Note 8)	●	0.6		5.3	V
$V_{OUT1(DC)}$, $V_{OUT2(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 22µF × 3, C_{OUT} = 100µF × 1 Ceramic, 220µF POSCAP	●	1.477	1.5	1.523	V
Input Specifications							
V_{RUN1}, V_{RUN2}	RUN Pin On/Off Threshold	RUN Rising		1.1	1.25	1.40	V
$V_{RUN1HYS}$, $V_{RUN2HYS}$	RUN Pin On Hysteresis				150		mV
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	I_{OUT} = 0A, C_{IN} = 22µF ×3, C_{SS} = 0.01µF, C_{OUT} = 100µF ×3, V_{OUT1} = 1.5V, V_{OUT2} = 1.5V, V_{IN} = 12V			1		A
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 12V, V_{OUT} = 1.5V, Burst Mode Operation V_{IN} = 12V, V_{OUT} = 1.5V, Pulse-Skipping Mode V_{IN} = 12V, V_{OUT}= 1.5V, Switching Continuous Shutdown, RUN = 0, V_{IN} = 12V			5 15 65 50		mA mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 13A V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 13A			4.6 1.853		A A
Output Specifications							
$I_{OUT1(DC)}$, $I_{OUT2(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 1.5V (Notes 7, 8)		0		13	A
$\Delta V_{OUT1(LINE)}/V_{OUT1}$ $\Delta V_{OUT2(LINE)}/V_{OUT2}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} from 4.75V to 16V I_{OUT} = 0A for Each Output,	●		0.01	0.025	%/V
$\Delta V_{OUT1}/V_{OUT1}$ $\Delta V_{OUT2}/V_{OUT2}$	Load Regulation Accuracy	For Each Output, V_{OUT} = 1.5V, 0A to 13A V_{IN} = 12V (Note 7)	●		0.35	0.5	%
$V_{OUT1(AC)}$, $V_{OUT2(AC)}$	Output Ripple Voltage	For Each Output, I_{OUT} = 0A, C_{OUT} = 100µF ×3/ X7R/Ceramic, 470µF POSCAP, V_{IN} = 12V, V_{OUT} = 1.5V, Frequency = 400kHz			15		mV_{P-P}
f_S (Each Channel)	Output Ripple Voltage Frequency	V_{IN} = 12V, V_{OUT} = 1.5V, f_{SET} = 1.25V (Note 4)			500		kHz
f_{SYNC} (Each Channel)	SYNC Capture Range			400		780	kHz
$\Delta V_{OUTSTART}$ (Each Channel)	Turn-On Overshoot	C_{OUT} = 100µF/X5R/Ceramic, 470µF POSCAP, V_{OUT} = 1.5V, I_{OUT} = 0A V_{IN} = 12V			10 10		mV mV
t_{START} (Each Channel)	Turn-On Time	C_{OUT} = 100µF/X5R/Ceramic, 470µF POSCAP, No Load, TRACK/SS with 0.01µF to GND, V_{IN} = 12V			5 5		ms ms
$\Delta V_{OUT(LS)}$ (Each Channel)	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load C_{OUT} = 22µF ×3/X5R/Ceramic, 470µF POSCAP V_{IN} = 12V, V_{OUT} = 1.5V			30		mV
t_{SETTLE} (Each Channel)	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, V_{IN} = 12V, C_{OUT} = 100µF, 470µF POSCAP			20		µs
$I_{OUT(PK)}$ (Each Channel)	Output Current Limit	V_{IN} = 12V, V_{OUT} = 1.5V			20		A
Control Section							
V_{FB1}, V_{FB2}	Voltage at V_{FB} Pins	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.592	0.600	0.606	V
I_{FB}		(Note 6)			–5	–20	nA
V_{OVL}	Feedback Overvoltage Lockout		●	0.64	0.66	0.68	V

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel. T_A = 25°C (Note 2), V_{IN} = 12V and VRUN1, VRUN2 at 5V unless otherwise noted. Per the typical application in Figure 26.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TRACK1 (I), TRACK2 (I)	Track Pin Soft-Start Pull-Up Current	TRACK1 (I),TRACK2 (I) Start at 0V		1	1.25	1.5	µA
UVLO	Undervoltage Lockout	V_{IN} Falling V_{IN} Rising			3.3 3.9		V V
UVLO Hysteresis					0.6		V
$t_{ON(MIN)}$	Minimum On-Time	(Note 6)			90		ns
R_{FBHI1}, R_{FBHI2}	Resistor Between V_{OUTS1}, V_{OUTS2} and V_{FB1}, V_{FB2} Pins for Each Output			59.90	60.4	60.75	kΩ
V_{PGOOD1}, V_{PGOOD2} Low	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±5	µA
V_{PGOOD}	PGOOD Trip Level	V_{FB} with Respect to Set Output Voltage V_{FB} Ramping Negative V_{FB} Ramping Positive			 –10 10		 % %
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 16V		4.8	5	5.2	V
V_{INTVCC} Load Regulation	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA			0.5	2	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive		4.5	4.7		V
$V_{EXTVCC(DROP)}$	$EXTV_{CC}$ Dropout	I_{CC} = 20mA, V_{EXTVCC} = 5V			50	100	mV
$V_{EXTVCC(HYST)}$	$EXTV_{CC}$ Hysteresis				200		mV
Oscillator and Phase-Locked Loop							
Frequency Nominal	Nominal Frequency	f_{SET} = 1.2V		450	500	550	kHz
Frequency Low	Lowest Frequency	f_{SET} = 0V (Note 5)		210	250	290	kHz
Frequency High	Highest Frequency	f_{SET} > 2.4V, Up to $INTV_{CC}$		700	780	860	kHz
f_{SET}	Frequency Set Current			9	10	11	µA
R_{MODE_PLLIN}	MODE_PLLIN Input Resistance				250		kΩ
CLKOUT	Phase (Relative to V_{OUT1})	PHASMD = GND PHASMD = Float PHASMD = $INTV_{CC}$			60 90 120		Deg Deg Deg
CLK High CLK Low	Clock High Output Voltage Clock Low Output Voltage			2		 0.2	V V
Differential Amplifier							
A_V Differential Amplifier	Gain				1		V
R_{IN}	Input Resistance	Measured at DIFFP Input			80		kΩ
V_{OS}	Input Offset Voltage	V_{DIFFP} = $V_{DIFFOUT}$ = 1.5V, $I_{DIFFOUT}$ = 100µA				3	mV
PSRR Differential Amplifier	Power Supply Rejection Ratio	5V < V_{IN} < 16V			90		dB
I_{CL}	Maximum Output Current				2		mA
$V_{OUT(MAX)}$	Maximum Output Voltage	$I_{DIFFOUT}$ = 300µA		$INTV_{CC}$ – 1.4			V

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel. T_A = 25°C (Note 2), V_{IN} = 12V and VRUN1, VRUN2 at 5V unless otherwise noted. Per the typical application in Figure 26.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GBW	Gain Bandwidth Product				3		MHz
V_{TEMP}	Diode Connected PNP	I = 100µA			0.598		V
TC	Temperature Coefficient		●		2.0		mV/C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4620A is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4620AE is guaranteed to meet specifications from 0°C to 125°C internal temperature. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4620AI is guaranteed over the full –40°C to 125°C internal operating temperature range. The LTM4620AMP is tested and guaranteed over the –55°C to 125°C operating temperature range. For output current derating at high temperature, please refer to thermal conditions and output current derating discussion. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: Two outputs are tested separately and the same testing condition is applied to each output.

Note 4: The switching frequency is programmable from 400kHz to 750kHz.

Note 5: The LTM4620A is designed to operate from 400kHz to 750kHz

Note 6: These parameters are tested at wafer sort.

Note 7: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

Note 8: Output current limitations. For 10V ≤ V_{IN} ≤ 16V, the 5V output current needs to be limited to 12A/channel, switching frequency = 750kHz. Derating curves apply. For 7V ≤ V_{IN} ≤ 9V, the 5V output current needs to be limited to 13A/channel, switching frequency = 750kHz. Derating curves apply. All other input and output combinations are 13A/channel with recommended switching frequency included in the efficiency graphs. Derating curves apply.

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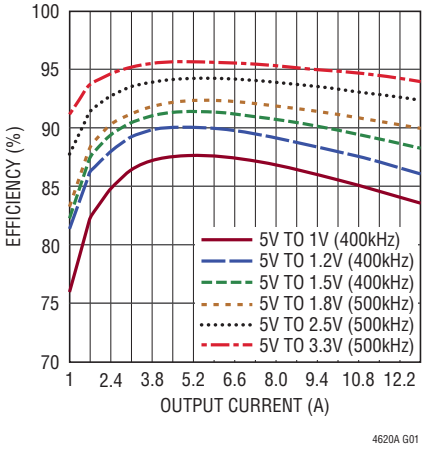
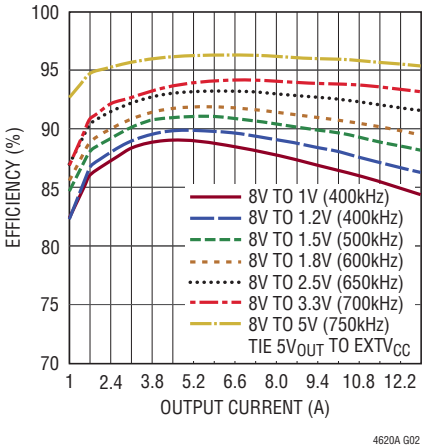
TYPICAL PERFORMANCE CHARACTERISTICS

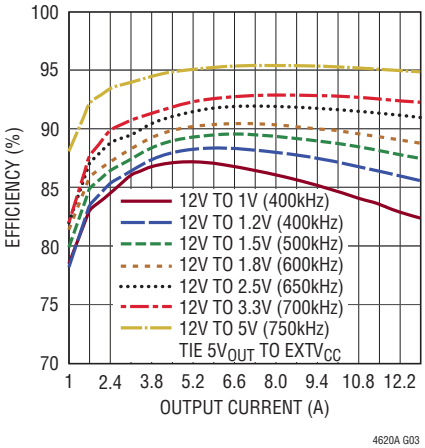
Efficiency vs Output Current, V_{IN} = 5V



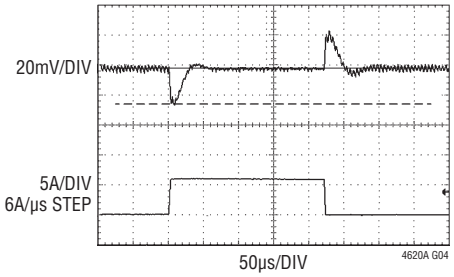
Efficiency vs Output Current, V_{IN} = 8V



Efficiency vs Output Current, V_{IN} = 12V

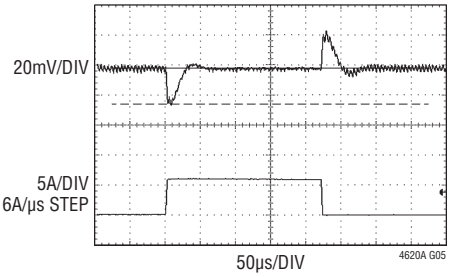


12V to 1V Load Step Response



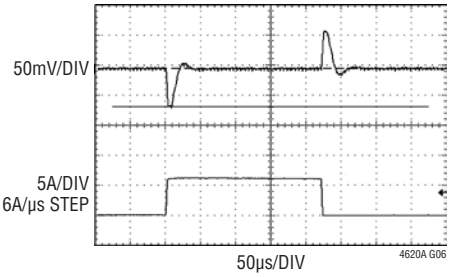
C_{FF} = 150pF
C_{OUT} = 2 × 470µF 9mΩ EACH POSCAP
1 × 100µF CERAMIC

12V to 1.2V Load Step Response



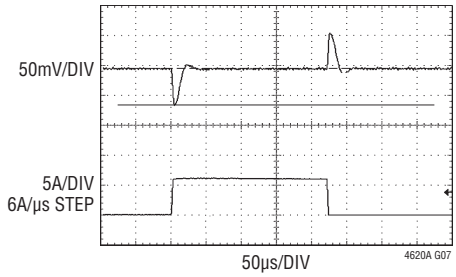
C_{FF} = 150pF
C_{OUT} = 2 × 470µF 9mΩ EACH POSCAP
1 × 100µF CERAMIC

12V to 1.5V Load Step Response



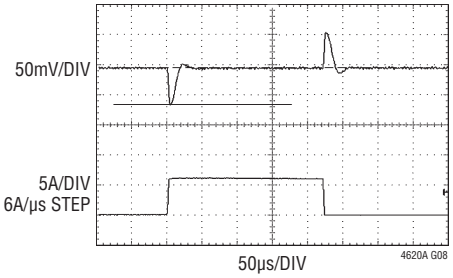
C_{FF} = 47pF
C_{OUT} = 220µF 9mΩ POSCAP
100µF CERAMIC

12V to 1.8V Load Step Response



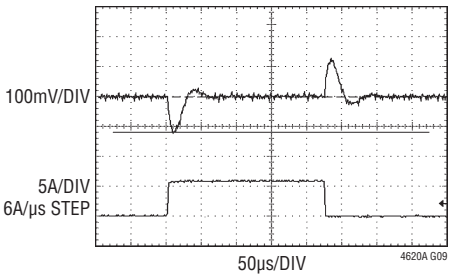
C_{FF} = 33pF
C_{OUT} = 220µF 9mΩ POSCAP
100µF CERAMIC

12V to 2.5V Load Step Response



C_{FF} = 100pF
C_{OUT} = 220µF 9mΩ POSCAP
100µF CERAMIC

12V to 3.3V Load Step Response



C_{FF} = 33pF
C_{OUT} = 100µF 15mΩ POSCAP
100µF CERAMIC

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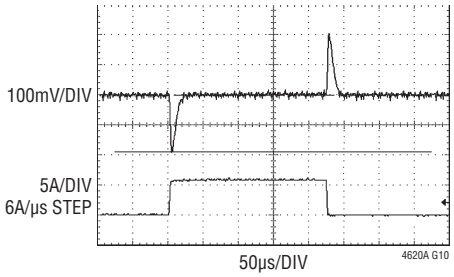
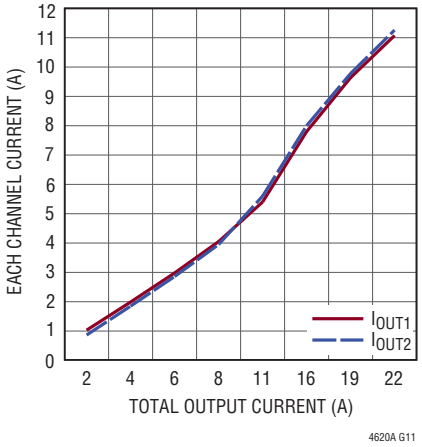
TYPICAL PERFORMANCE CHARACTERISTICS

12V to 5V Load Step Response

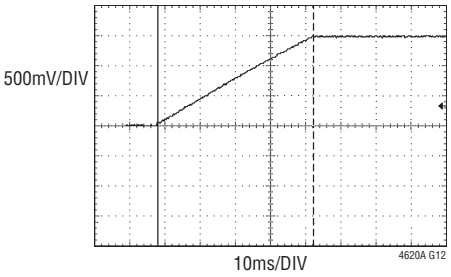


C_{FF} = 47pF
C_{OUT} = 100µF CERAMIC X7R

Output Current Sharing

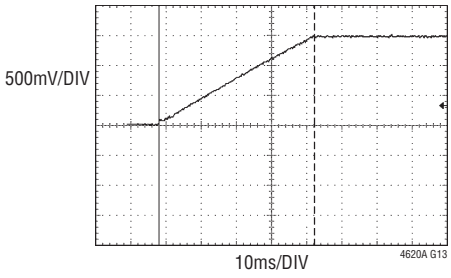


12V to 1.5V Start-Up, No Load



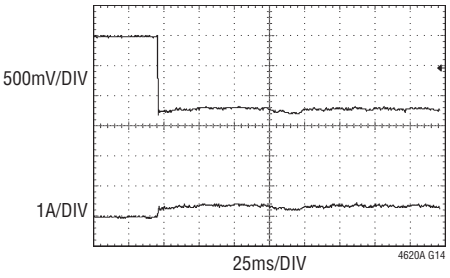
$12V_{IN}$, $1.5V_{OUT}$ AT NO LOAD
C_{OUT} = 2 × 470µF, 4V SANYO POSCAP,
1 × 100µF, 6.3V CERAMIC
SOFT-START CAPACITOR = 0.01µF
USE RUN PIN TO CONTROL START-UP

Single Phase Start-Up, 13A Load



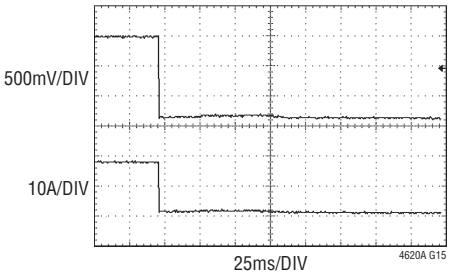
$12V_{IN}$, $1.5V_{OUT}$ AT 13A LOAD
C_{OUT} = 2 × 470µF, 4V SANYO POSCAP,
1 × 100µF, 6.3V CERAMIC
SOFT-START CAPACITOR = 0.01µF
USE RUN PIN TO CONTROL START-UP

12V to 1.5V, 0A Load Short-Circuit Testing



$12V_{IN}$, $1.5V_{OUT}$ AT 0A LOAD
C_{OUT} = 2 × 470µF, 4V SANYO POSCAP,
1 × 100µF, 6.3V X5R CERAMIC
SOFT-START CAPACITOR = 0.01µF
USE RUN PIN TO CONTROL START-UP

12V to 1.5V, 13A No Load Short-Circuit Testing



$12V_{IN}$, $1.5V_{OUT}$ AT 13A LOAD
C_{OUT} = 2 × 470µF, 4V SANYO POSCAP,
1 × 100µF, 6.3V X5R CERAMIC
SOFT-START CAPACITOR = 0.01µF
USE RUN PIN TO CONTROL START-UP

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PIN FUNCTIONS (Recommended to Use Test Points to Monitor Signal Pin Connections.)

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{OUT1} (A1-A5, B1-B5, C1-C4): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. Review Table 5. See Note 8 in the Electrical Characteristics section for output current guideline.

GND (A6-A7, B6-B7, D1-D4, D9-D12, E1-E4, E10-E12, F1-F3, F10-F12, G1, G3, G10, G12, H1-H7, H9-H12, J1, J5, J8, J12, K1, K5-K8, K12, L1, L12, M1 , M12): Power Ground Pins for Both Input and Output Returns.

V_{OUT2} (A8-A12, B8-B12, C9-C12): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. Review Table 5. See Note 8 in the Electrical Characteristics section for output current guideline.

V_{OUTS1}, V_{OUTS2} (C5, C8): This pin is connected to the top of the internal top feedback resistor for each output. The pin can be directly connected to its specific output, or connected to DIFFOUT when the remote sense amplifier is used. In paralleling modules, one of the V_{OUTS} pins is connected to the DIFFOUT pin in remote sensing or directly to V_{OUT} with no remote sensing. It is very important to connect these pins to either the DIFFOUT or V_{OUT} since this is the feedback path, and cannot be left open. See the Applications Information section.

f_{SET} (C6): Frequency Set Pin. A 10µA current is sourced from this pin. A resistor from this pin to ground sets a voltage that in turn programs the operating frequency. Alternatively, this pin can be driven with a DC voltage that can set the operating frequency. See the Applications Information section.

SGND (C7, D6, G6-G7, F6-F7): Signal Ground Pin. Return ground path for all analog and low power circuitry. Tie a single connection to the output capacitor GND in the application. See layout guidelines in Figure 25.

V_{FB1}, V_{FB2} (D5, D7): The Negative Input of the Error Amplifier for Each Channel. Internally, this pin is connected to V_{OUTS1} or V_{OUTS2} with a 60.4kΩ precision resistor. Different output voltages can be programmed with an additional resistor between V_{FB} and GND pins. In PolyPhase® operation, tying the V_{FB} pins together allows for parallel operation. See the Applications Information section for details.

TRACK1, TRACK2 (E5, D8): Output Voltage Tracking Pin and Soft-Start Inputs. Each channel has a 1.3µA pull-up current source. When one channel is configured to be master of the two channels, then a capacitor from this pin to ground will set a soft-start ramp rate. The remaining channel can be set up as the slave, and have the master's output applied through a voltage divider to the slave output's track pin. This voltage divider is equal to the slave output's feedback divider for coincidental tracking. See the Applications Information section.

COMP1, COMP2 (E6, E7): Current control threshold and error amplifier compensation point for each channel. The current comparator threshold increases with this control voltage. Tie the COMP pins together for parallel operation. The device is internal compensated.

DIFFP (E8): Positive input of the remote sense amplifier. This pin is connected to the remote sense point of the output voltage. Diffamp can be used for ≤3.3V outputs. See the Applications Information section.

DIFFN (E9): Negative input of the remote sense amplifier. This pin is connected to the remote sense point of the output GND. Diffamp can be used for ≤3.3V outputs. See the Applications Information section.

MODE_PLLIN (F4): Force Continuous Mode, Burst Mode Operation, or Pulse-Skipping Mode Selection Pin and External Synchronization Input to Phase Detector Pin. Connect this pin to SGND to force both channels into force continuous mode of operation. Connect to $INTV_{CC}$ to enable pulse-skipping mode of operation. Leaving the pin floating will enable Burst Mode operation. A clock on the pin will force both channels into continuous mode of operation and synchronized to the external clock applied to this pin.

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PIN FUNCTIONS (Recommended to Use Test Points to Monitor Signal Pin Connections.)

RUN1, RUN2 (F5, F9): Run Control Pin. A voltage above 1.25V will turn on each channel in the module. A voltage below 1.25V on the RUN pin will turn off the related channel. Each RUN pin has a 1µA pull-up current, once the RUN pin reaches 1.2V an additional 4.5µA pull-up current is added to this pin.

DIFFOUT (F8): Internal Remote Sense Amplifier Output. Connect this pin to V_{OUTS1} or V_{OUTS2} depending on which output is using remote sense. In parallel operation connect one of the V_{OUTS} pin to DIFFOUT for remote sensing. Diffamp can be used for ≤3.3V outputs.

SW1, SW2 (G2, G11): Switching node of each channel that is used for testing purposes. Also an R-C snubber network can be applied to reduce or eliminate switch node ringing, or otherwise leave floating. See the Applications Information section.

PHASMD (G4): Connect this pin to SGND, $INTV_{CC}$, or floating this pin to select the phase of CLKOUT to 60 degrees, 120 degrees, and 90 degrees respectively.

CLKOUT (G5): Clock output with phase control using the PHASMD pin to enable multiphase operation between devices. See the Applications Information section.

PGOOD1, PGOOD2 (G9, G8): Output Voltage Power Good Indicator. Open drain logic output that is pulled to ground when the output voltage is not within ±7.5% of the regulation point.

$INTV_{CC}$ (H8): Internal 5V Regulator Output. The control circuits and internal gate drivers are powered from this voltage. Decouple this pin to PGND with a 4.7µF low ESR tantalum or ceramic. $INTV_{CC}$ is activated when either RUN1 or RUN2 is activated.

TEMP (J6): Onboard Temperature Diode for Monitoring the VBE Junction Voltage Change with Temperature. See the Applications Information section.

$EXTV_{CC}$ (J7): External power input that is enabled through a switch to $INTV_{CC}$ whenever $EXTV_{CC}$ is greater than 4.7V. Do not exceed 6V on this input, and connect this pin to V_{IN} when operating V_{IN} on 5V. An efficiency increase will occur that is a function of the (V_{IN} – $INTV_{CC}$) multiplied by power MOSFET driver current. Typical current requirement is 30mA. V_{IN} must be applied before $EXTV_{CC}$, and $EXTV_{CC}$ must be removed before V_{IN}. A 5V output can be tied to this pin to increase efficiency. See Applications Information section.

V_{IN} (M2-M11, L2-L11, J2-J4, J9-J11, K2-K4, K9-K11): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

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SIMPLIFIED BLOCK DIAGRAM

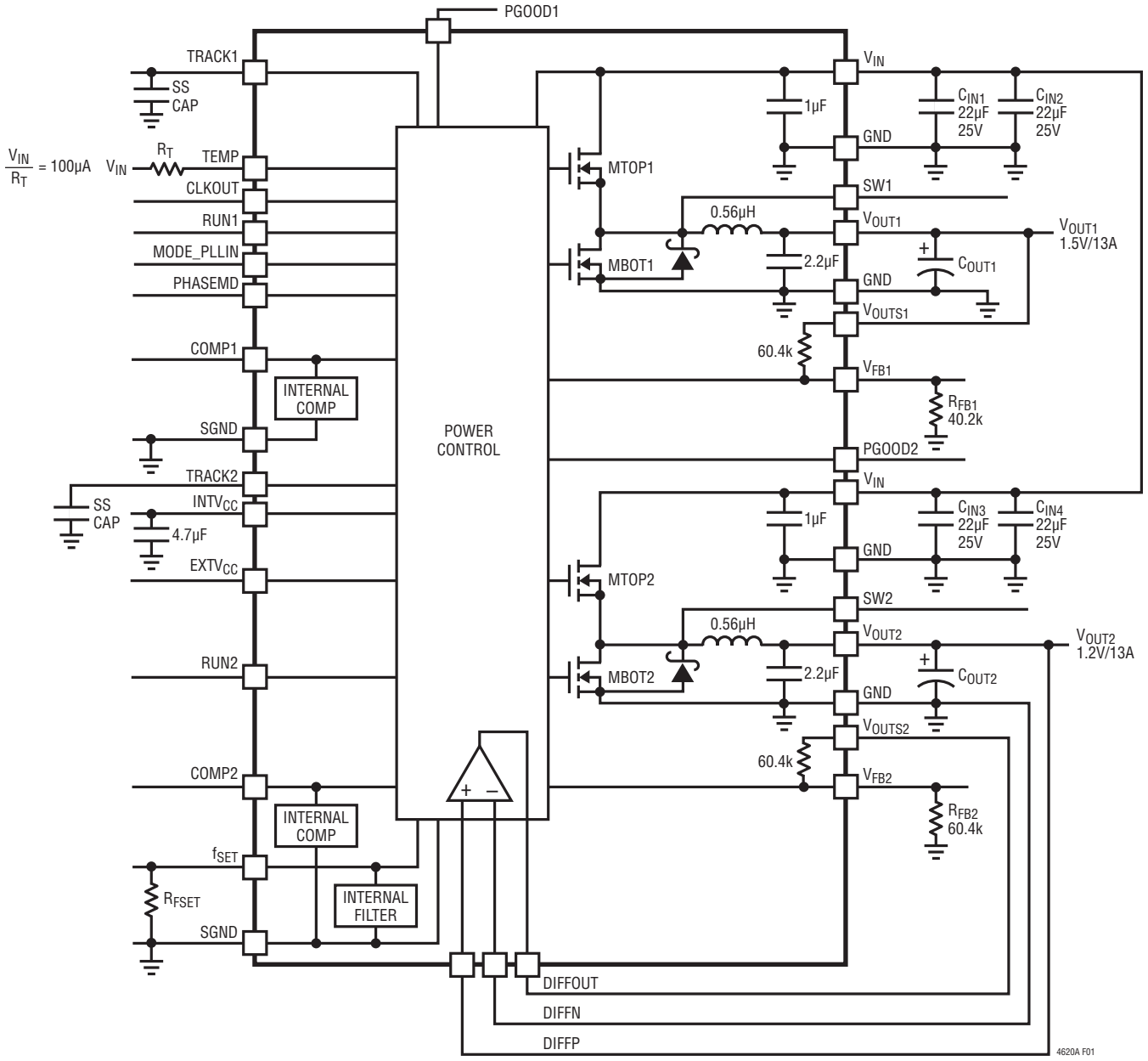

Figure 1. Simplified LTM4620A Block Diagram

DECOUPLING REQUIREMENTS

T_A = 25°C. Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN1}, C_{IN2} C_{IN3}, C_{IN4}	External Input Capacitor Requirement (V_{IN1} = 4.75V to 16V, V_{OUT1} = 1.5V) (V_{IN2} = 4.75V to 16V, V_{OUT2} = 1.2V)	 I_{OUT1} = 13A I_{OUT2} = 13A (Note 8)		 22 22		 µF µF
C_{OUT1} C_{OUT2}	External Output Capacitor Requirement (V_{IN1} = 4.75V to 16V, V_{OUT1} = 1.5V) (V_{IN2} = 4.75V to 16V, V_{OUT2} = 1.2V)	 I_{OUT1} = 13A I_{OUT2} = 13A (Note 8)		 300 300		 µF µF

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OPERATION

Power Module Description

The LTM4620A is a dual-output standalone nonisolated switching mode DC/DC power supply. It can provide two 13A outputs with few external input and output capacitors and setup components. This module provides precisely regulated output voltages programmable via external resistors from $0.6V_{DC}$ to $5.3V_{DC}$ over 4.5V to 16V input voltages. The typical application schematic is shown in Figure 26. See Note 8 in the Electrical Characteristics section for output current guideline.

The LTM4620A has dual integrated constant-frequency current mode regulators and built-in power MOSFET devices with fast switching speed. The typical switching frequency is 500kHz. For switching-noise sensitive applications, it can be externally synchronized from 400kHz to 780kHz. A resistor can be used to program a free run frequency on the f_{SET} pin. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4620A module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit and foldback current limit in an overcurrent condition. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD outputs low if the output feedback voltage exits a ±10% window around the regulation point. As the output voltage exceeds 10% above regulation, the bottom MOSFET will turn on to clamp the output voltage. The top MOSFET will be turned off. This overvoltage protect is feedback voltage referred.

Pulling the RUN pins below 1.1V forces the regulators into a shutdown state, by turning off both MOSFETs. The TRACK pins are used for programming the output voltage ramp and voltage tracking during start-up or used for soft-starting the regulator. See the Applications Information section.

The LTM4620A is internally compensated to be stable over all operating conditions. Table 5 provides a guide line for input and output capacitances for several operating conditions. LTpowerCAD® is available for transient and stability analysis. The V_{FB} pin is used to program the output voltage with a single external resistor to ground. A differential remote sense amplifier is available for sensing the output voltage accurately on one of the outputs at the load point, or in parallel operation sensing the output voltage at the load point.

Multiphase operation can be easily employed with the MODE_PLLIN, PHASMD, and CLKOUT pins. Up to 12 phases can be cascaded to run simultaneously with respect to each other by programming the PHMODE pin to different levels. See the Applications Information section.

High efficiency at light loads can be accomplished with selectable Burst Mode operation or pulse-skipping operation using the MODE pin. These light load features will accommodate battery operation. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics section. See the Applications Information section for details.

A TEMP pin is provided to allow the internal device temperature to be monitored using an onboard diode connected PNP transistor. This diode connected PNP transistor is grounded in the module and can be used as a general temperature monitor using a device that is designed to monitor the single-ended connection.

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APPLICATIONS INFORMATION

The typical LTM4620A application circuit is shown in Figure 26. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 5 for specific external capacitor requirements for particular applications.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} and V_{OUT} step-down ratio that can be achieved for a given input voltage. Each output of the LTM4620A is capable of 95% duty cycle at 500kHz, but the V_{IN} to V_{OUT} minimum drop-out is still shown as a function of its load current and will limit output current capability related to high duty cycle on the top side switch. Minimum on-time $t_{ON(MIN)}$ is another consideration in operating at a specified duty cycle while operating at a certain frequency due to the fact that $t_{ON(MIN)} < D/f_{SW}$, where D is duty cycle and f_{SW} is the switching frequency. $t_{ON(MIN)}$ is specified in the electrical parameters as 90ns. See Note 8 in the Electrical Characteristics section for output current guideline.

Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 60.4kΩ internal feedback resistor connects between the V_{OUTS1} to V_{FB1} and V_{OUTS2} to V_{FB2}. It is very important that these pins be connected to their respective outputs for proper feedback regulation. Overvoltage can occur if these V_{OUTS1} and V_{OUTS2} pins are left floating when used as individual regulators, or at least one of them is used in paralleled regulators. The output voltage will default to 0.6V with no feedback resistor on either V_{FB1} or V_{FB2}. Adding a resistor R_{FB} from V_{FB} pin to GND programs the output voltage:

$$V_{OUT} = 0.6V \bullet \frac{60.4k + R_{FB}}{R_{FB}}$$

Table 1. V_{FB} Resistor Table vs Various Output Voltages

V_{OUT}	0.6V	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V	5V
R_{FB}	Open	90.9k	60.4k	40.2k	30.2k	19.1k	13.3k	8.25k

For parallel operation of multiple channels the same feedback setting resistor can be used for the parallel design. This is done by connecting the V_{OUTS1} to the output as shown in Figure 2, thus tying one of the internal 60.4k resistors to the output. All of the V_{FB} pins tie together with one programming resistor as shown in Figure 2.

In parallel operation, the V_{FB} pins have an I_{FB} current of 20nA maximum each channel. To reduce output voltage error due to this current, an additional V_{OUTS} pin can be tied to V_{OUT}, and an additional R_{FB} resistor can be used to lower the total Thevenin equivalent resistance seen by this current. For example in Figure 2, the total Thevenin equivalent resistance of the V_{FB} pin is (60.4k//R_{FB}), which is 30.2k where R_{FB} is equal to 60.4k for a 1.2V output. Four phases connected in parallel equates to a worse case feedback current of 4 • I_{FB} = 80nA maximum. The voltage error is 80nA • 30.2k = 2.4mV. If V_{OUTS2} is connected, as shown in Figure 2, to V_{OUT}, and another 60.4k resistor is connected from V_{FB2} to ground, then the voltage error is reduced to 1.2mV. If the voltage error is acceptable then no additional connections are necessary. The onboard 60.4k resistor is 0.5% accurate and the V_{FB} resistor can be chosen by the user to be as accurate as needed. All COMP pins are tied together for current sharing between the phases. The TRACK pins can be tied together and a single soft-start capacitor can be used to soft-start the regulator. The soft-start equation will need to have the soft-start current parameter increased by the number of paralleled channels. See TRACK/Soft-Start Pin section.

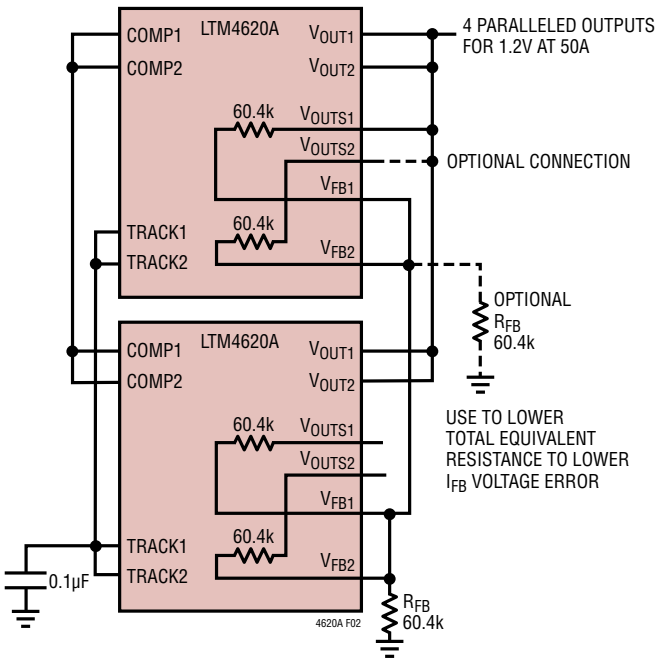

Figure 2. 4-Phase Parallel Configurations

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APPLICATIONS INFORMATION

Input Capacitors

The LTM4620A module should be connected to a low AC-impedance DC source. For the regulator input four 22µF input ceramic capacitors are used for RMS ripple current. A 47µF to 100µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty-cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor current ripple, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

In the above equation, η% is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor, Polymer capacitor.

Output Capacitors

The LTM4620A is designed for low output voltage ripple noise and good transient response. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, the low ESR polymer capacitor or ceramic capacitor. The typical output capacitance range for each output is from 200µF to 470µF. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 5 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 7A/µs transient. The table optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 5 matrix, and the LTpowerCAD will be provided for stability analysis. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. The LTpowerCAD can calculate the output ripple reduction as the number of implemented phases increases by N times. A small value 10Ω to 50Ω resistor can be place in series from V_{OUT} to the V_{OUTS} pin to allow for a bode plot analyzer to inject a signal into the control loop and validate the regulator stability. The same resistor could be place in series from V_{OUT} to DIFFP and a bode plot analyzer could inject a signal into the control loop and validate the regulator stability.

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APPLICATIONS INFORMATION

Burst Mode Operation

The LTM4620A is capable of Burst Mode operation on each regulator in which the power MOSFETs operate intermittently based on load demand, thus saving quiescent current. For applications where maximizing the efficiency at very light loads is a high priority, Burst Mode operation should be applied. Burst Mode operation is enabled with the MODE/PLLIN pin floating. During this operation, the peak current of the inductor is set to approximately one third of the maximum peak current value in normal operation even though the voltage at the COMP pin indicates a lower value. The voltage at the COMP pin drops when the inductor's average current is greater than the load requirement. As the COMP voltage drops below 0.5V, the BURST comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs.

In sleep mode, the internal circuitry is partially turned off, reducing the quiescent current to about 450µA for each output[22]. The load current is now being supplied from the output capacitors. When the output voltage drops, causing COMP to rise above 0.5V, the internal sleep line goes low, and the LTM4620A resumes normal operation. The next oscillator cycle will turn on the top power MOSFET and the switching cycle repeats. Either regulator can be configured for Burst Mode operation.

Pulse-Skipping Mode Operation

In applications where low output ripple and high efficiency at intermediate currents are desired, pulse-skipping mode should be used. Pulse-skipping operation allows the LTM4620A to skip cycles at low output loads, thus increasing efficiency by reducing switching loss. Tying the MODE/PLLIN pin to $INTV_{CC}$ enables pulse-skipping operation. At light loads the internal current comparator may remain tripped for several cycles and force the top MOSFET to stay off for several cycles, thus skipping cycles. The inductor current does not reverse in this mode. This mode will maintain higher effective frequencies thus lower output ripple and lower noise than Burst Mode operation. Either regulator can be configured for pulse-skipping mode.

Forced Continuous Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE/PLLIN pin to GND. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4620A's output voltage is in regulation. Either regulator can be configured for force continuous mode.

Multiphase Operation

For output loads that demand more than 13A of current, two outputs in LTM4620A or even multiple LTM4620As can be paralleled to run out of phase to provide more output current without increasing input and output voltage ripples. The MODE/PLLIN pin allows the LTM4620A to synchronize to an external clock (between 400kHz and 780kHz) and the internal phase-locked-loop allows the LTM4620A to lock onto an incoming clock phase as well. The CLKOUT signal can be connected to the MODE/PLLIN pin of the following stage to line up both the frequency and the phase of the entire system. Tying the PHMODE pin to $INTV_{CC}$, SGND, or (floating) generates a phase difference (between MODE/PLLIN and CLKOUT) of 120 degrees, 60 degrees, or 90 degrees respectively. A total of 12 phases can be cascaded to run simultaneously with respect to each other by programming the PHMODE pin of each LTM4620A channel to different levels. Figure 3 shows a 2-phase design, 4-phase design and a 6-phase design example for clock phasing with the PHASMD table.

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage

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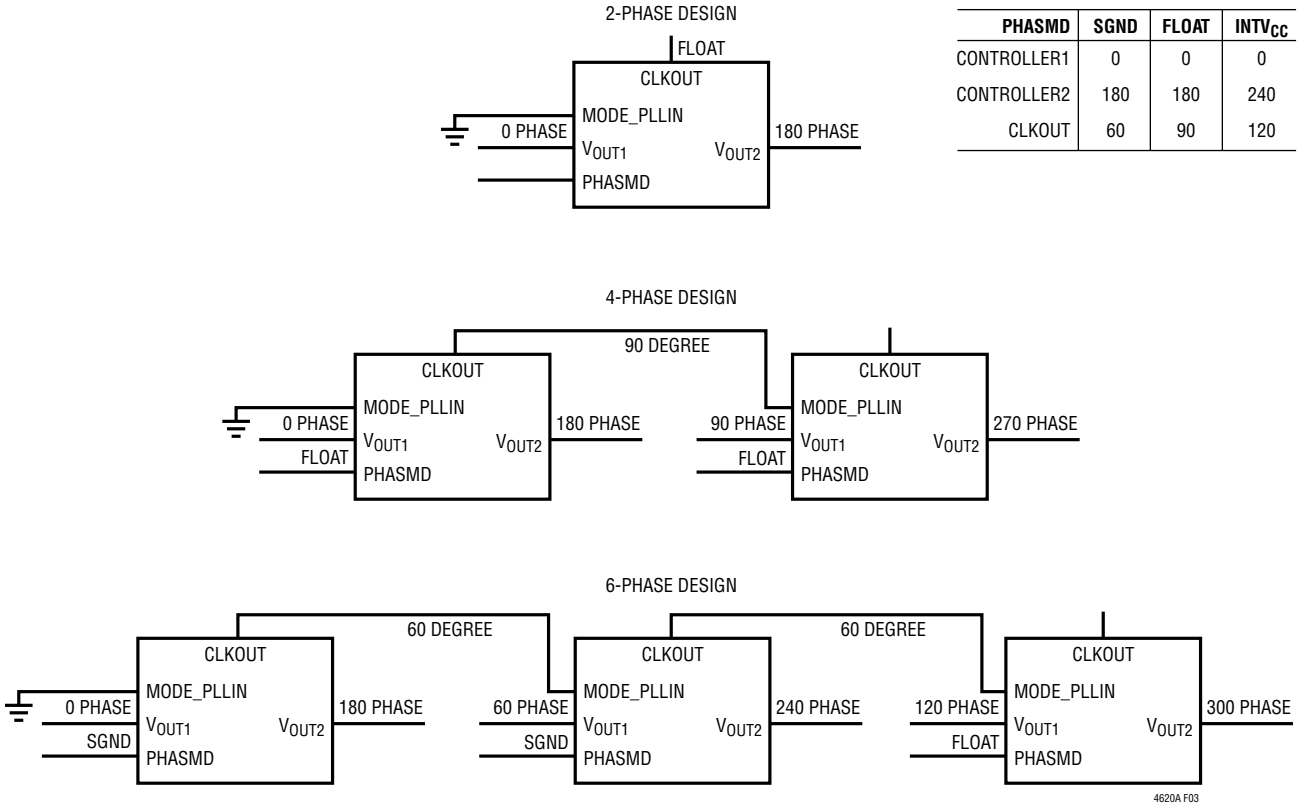

PHASMD	SGND	FLOAT	$INTV_{CC}$
CONTROLLER1	0	0	0
CONTROLLER2	180	180	240
CLKOUT	60	90	120

Figure 3. Examples of 2-Phase, 4-Phase, and 6-Phase Operation with PHASMD Table

is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when all of the outputs are tied together to achieve a single high output current design.

The LTM4620A device is an inherently current mode controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design. Figure 26 shows an example of parallel operation and pin connection.

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APPLICATIONS INFORMATION

Input RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 4 shows this graph.

Frequency Selection and Phase-Lock Loop (MODE/PLLIN and f_{SET} Pins)

The LTM4620A device is operated over a range of frequencies to improve power conversion efficiency. It is recommended to operate the lower output voltages or lower duty cycle conversions at lower frequencies to improve efficiency by lowering power MOSFET switching losses. Higher output voltages or higher duty cycle conversions can be operated at higher frequencies to limit inductor ripple current. The efficiency graphs will show an operating frequency chosen for that condition. Select frequency in reference to the highest output voltage.

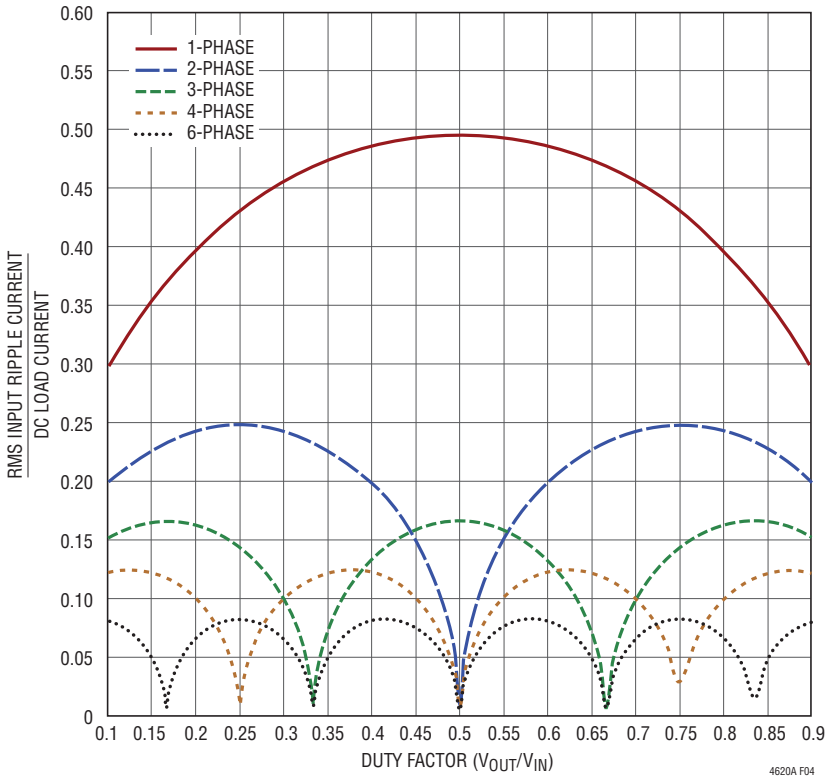

Figure 4. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle

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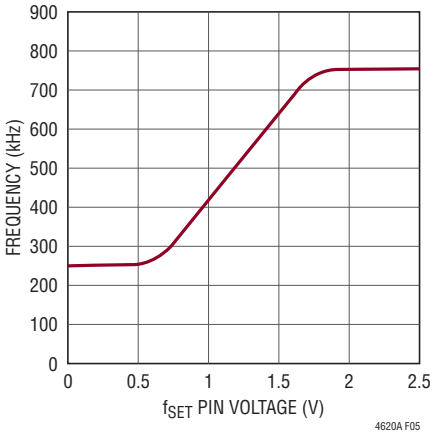

Figure 5. Operating Frequency vs f_{SET} Pin Voltage

The LTM4620A switching frequency can be set with an external resistor from the f_{SET} pin to SGND. An accurate 10µA current source into the resistor will set a voltage that programs the frequency or a DC voltage can be applied. Figure 5 shows a graph of frequency setting verses programming voltage. An external clock can be applied to the MODE/PLLIN pin from 0V to $INTV_{CC}$ over a frequency range of 400kHz to 780kHz. The clock input high threshold is 1.6V and the clock input low threshold is 1V. The LTM4620A has the PLL loop filter components on board. The frequency setting resistor should always be present to set the initial switching frequency before locking to an external clock. Both regulators will operate in continuous mode while being externally clock.

The output of the PLL phase detector has a pair of complementary current sources that charge and discharge the internal filter network. When the external clock is applied then the f_{SET} frequency resistor is disconnected with an internal switch, and the current sources control the frequency adjustment to lock to the incoming external clock. When no external clock is applied, then the internal switch is on, thus connecting the external f_{SET} frequency set resistor for free run operation.

Minimum On-Time

Minimum on-time t_{ON} is the smallest time duration that the LTM4620A is capable of turning on the top MOSFET on either channel. It is determined by internal timing delays, and the gate charge required turning on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$\frac{V_{OUT}}{V_{IN} \bullet FREQ} > t_{ON(MIN)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the output ripple will increase. The on-time can be increased by lowering the switching frequency. A good rule of thumb is to keep on-time longer than 110ns.

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK pins. The output can be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider to implement coincident tracking. The LTM4620A uses an accurate 60.4k resistor internally for the top feedback resistor for each channel. Figure 6 shows an example of coincident tracking. Equations:

$$SLAVE = \left(1 + \frac{60.4k}{R_{TA}}\right) \bullet V_{TRACK}$$

V_{TRACK} is the track ramp applied to the slave's track pin. V_{TRACK} has a control range of 0V to 0.6V, or the internal reference voltage. When the master's output is divided down with the same resistor values used to set the slave's output, then the slave will coincident track with the master until it reaches its final value. The master will continue to its final value from the slave's regulation point. Voltage tracking is disabled when V_{TRACK} is more than 0.6V. R_{TA} in Figure 6 will be equal to the R_{FB} for coincident tracking. Figure 7 shows the coincident tracking waveforms.

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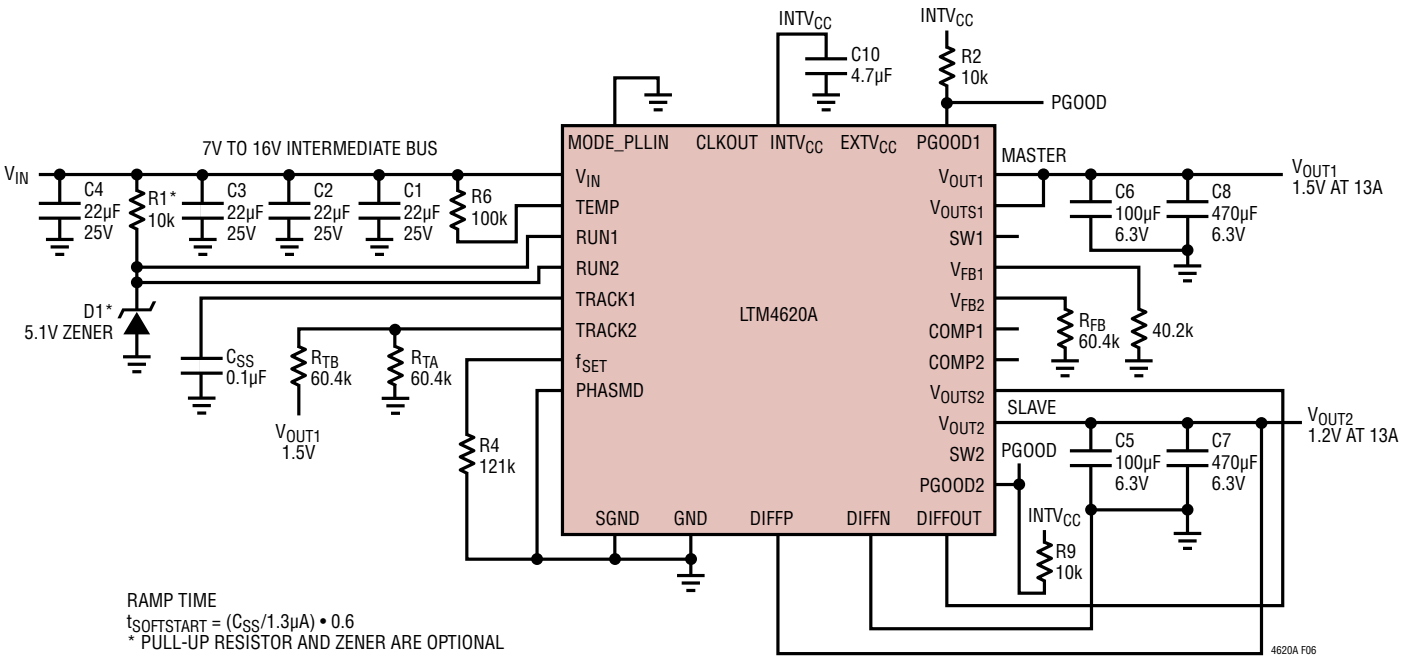

Figure 6. Example of Output Tracking Application Circuit

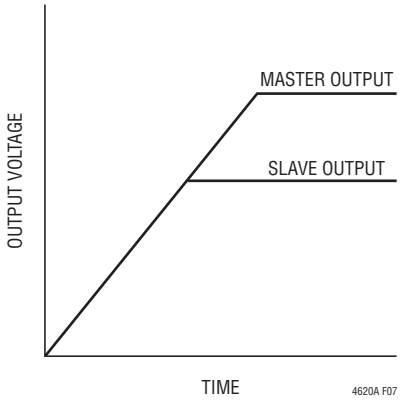

Figure 7. Output Coincident Tracking Waveform

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The TRACK pin can be controlled by a capacitor placed on the regulator TRACK pin to ground. A 1.3µA current source will charge the TRACK pin up to the reference voltage and then proceed up to $INTV_{CC}$. After the 0.6V ramp, the TRACK pin will no longer be in control, and the internal voltage reference will control output regulation from the feedback divider. Foldback current limit is disabled during this sequence of turn-on during tracking or soft-starting. The TRACK pins are pulled low when the RUN pin is below 1.2V. The total soft-start time can be calculated as:

$$t_{SOFT\text{-}START} = \left(\frac{C_{SS}}{1.3\mu A} \right) \bullet 0.6$$

Regardless of the mode selected by the MODE/PLLIN pin, the regulator channels will always start in pulse-skipping mode up to TRACK = 0.5V. Between TRACK = 0.5V and 0.54V, it will operate in forced continuous mode and revert to the selected mode once TRACK > 0.54V. In order to track with another channel once in steady state operation, the LTM4620A is forced into continuous mode operation as soon as V_{FB} is below 0.54V regardless of the setting on the MODE/PLLIN pin.

Ratiometric tracking can be achieved by a few simple calculations and the slew rate value applied to the master's TRACK pin. As mentioned above, the TRACK pin has a control range from 0 to 0.6V. The master's TRACK pin slew rate is directly equal to the master's output slew rate in Volts/Time. The equation:

$$\frac{MR}{SR} \bullet 60.4k = R_{TB}$$

where MR is the master's output slew rate and SR is the slave's output slew rate in Volts/Time. When coincident tracking is desired, then MR and SR are equal, thus R_{TB} is equal the 60.4k. R_{TA} is derived from equation:

$$R_{TA} = \frac{0.6V}{\frac{V_{FB}}{60.4k} + \frac{V_{FB}}{R_{FB}} - \frac{V_{TRACK}}{R_{TB}}}$$

where V_{FB} is the feedback voltage reference of the regulator, and V_{TRACK} is 0.6V. Since R_{TB} is equal to the 60.4k top feedback resistor of the slave regulator in equal slew rate or coincident tracking, then R_{TA} is equal to R_{FB} with $V_{FB} = V_{TRACK}$. Therefore R_{TB} = 60.4k, and R_{TA} = 60.4k in Figure 6.

In ratiometric tracking, a different slew rate maybe desired for the slave regulator. R_{TB} can be solved for when SR is slower than MR. Make sure that the slave supply slew rate is chosen to be fast enough so that the slave output voltage will reach it final value before the master output.

For example, MR = 1.5V/1ms, and SR = 1.2V/1ms. Then R_{TB} = 76.8k. Solve for R_{TA} to equal to 49.9k.

Each of the TRACK pins will have the 1.3µA current source on when a resistive divider is used to implement tracking on that specific channel. This will impose an offset on the TRACK pin input. Smaller values resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the 60.4k is used then a 6.04k can be used to reduce the TRACK pin offset to a negligible value.

Power Good

The PGOOD pins are open drain pins that can be used to monitor valid output voltage regulation. This pin monitors a ±10% window around the regulation point. A resistor can be pulled up to a particular supply voltage no greater than 6V maximum for monitoring.

Stability Compensation

The module has already been internally compensated for all output voltages. Table 5 is provided for most application requirements. The LTpowerCAD will be provided for other control loop optimization.

Run Enable

The RUN pins have an enable threshold of 1.4V maximum, typically 1.25V with 150mV of hysteresis. They control the turn on each of the channels and $INTV_{CC}$. These pins can be pulled up to V_{IN} for 5V operation, or a 5V Zener diode can be placed on the pins and a 10k to 100k resistor can be placed up to higher than 5V input for enabling the channels. The RUN pins can also be used for output voltage sequencing. In parallel operation the RUN pins can be tie together

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APPLICATIONS INFORMATION

and controlled from a single control. See the Typical Application circuits in Figure 26.

$INTV_{CC}$ and $EXTV_{CC}$

The LTM4620A module has an internal 5V low dropout regulator that is derived from the input voltage. This regulator is used to power the control circuitry and the power MOSFET drivers. This regulator can source up to 70mA, and typically uses ~30mA for powering the device at the maximum frequency. This internal 5V supply is enabled by either RUN1 or RUN2.

$EXTV_{CC}$ allows an external 5V supply to power the LTM4620A and reduce power dissipation from the internal low dropout 5V regulator. The power loss savings can be calculated by:

$$(V_{IN} – 5V) • 30mA = PLOSS$$

$EXTV_{CC}$ has a threshold of 4.7V for activation, and a maximum rating of 6V. When using a 5V input, connect this 5V input to $EXTV_{CC}$ also to maintain a 5V gate drive level. $EXTV_{CC}$ must sequence on after V_{IN}, and $EXTV_{CC}$ must sequence off before V_{IN}. When designing a 5V output, connect this 5V output to $EXTV_{CC}$. Use an external 5V bias on $EXTV_{CC}$ to improve efficiency.

Differential Remote Sense Amplifier

An accurate differential remote sense amplifier is provided to sense low output voltages accurately at the remote load points. This is especially true for high current loads. The amplifier can be used on one of the two channels, or on a single parallel output. It is very important that the DIFFP and DIFFN are connected properly at the output, and DIFFOUT is connected to either V_{OUTS1} or V_{OUTS2}. In parallel operation, the DIFFP and DIFFN are connected properly at the output, and DIFFOUT is connected to one of the V_{OUTS} pins. Review the parallel schematics in Figure 29 and review Figure 2. The diffamp can only be used for output voltage ≤3.3V.

SW Pins

The SW pins are generally for testing purposes by monitoring these pins. These pins can also be used to dampen out switch node ringing caused by LC parasitic in the switched current paths. Usually a series R-C combination is used called a snubber circuit. The resistor will dampen the resonance and the capacitor is chosen to only affect the high frequency ringing across the resistor. If the stray inductance or capacitance can be measured or approximated then a somewhat analytical technique can be used to select the snubber values. The inductance is usually easier to predict. It combines the power path board inductance in combination with the MOSFET interconnect bond wire inductance.

First the SW pin can be monitored with a wide bandwidth scope with a high frequency scope probe. The ring frequency can be measured for its value. The impedance Z can be calculated:

$$Z(L) = 2\pi fL,$$

where f is the resonant frequency of the ring, and L is the total parasitic inductance in the switch path. If a resistor is selected that is equal to Z, then the ringing should be dampened. The snubber capacitor value is chosen so that its impedance is equal to the resistor at the ring frequency. Calculated by: $Z(C) = 1/(2\pi fC)$. These values are a good place to start with. Modification to these components should be made to attenuate the ringing with the least amount of power loss.

Temperature Monitoring (TEMP)

A diode connected PNP transistor is used for the TEMP monitor function by monitoring its voltage over temperature. The temperature dependence of this diode can be understood in the equation:

$$D = nVTIn\left(\frac{ID}{IS}\right),$$

Where V_T is the thermal voltage (kT/q), and n, the ideality factor is 1 for the two diode connected PNPs being used in the LTM4620. Since I_D has an exponential temperature dependence that can be understood from the typical empirical equation for I_S:

$$I_S = I_{0\ exp\ (–VG0/VT)},$$

Where I_0 is some process and geometry dependent current (I_0 is typically around 20 orders of magnitude larger than I_S at room temperature, so I_0 is much larger than typical

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values of I_D), and VG0 is the band gap voltage of 1.2V extrapolated to absolute zero of –273°C Kelvin. Figure 8 shows a plot of the diode temperature characteristic of the diode connected PNP transistor biased with a 100µA current source. This plot would extend to the left back to 1.2V at –273°C Kelvin. This curve is stop at –55°C due to the test system limits.

If we take the I_S equation and substitute into the V_D equation, then we get:

$$VD = VG0 - \left(\frac{Kt}{q}\right) \ln\left(\frac{I0}{ID}\right), V_T = \left(\frac{kT}{q}\right)$$

The expression shows that the junction voltage of the PNP connected diode decreases linearly if I_0 were constant from a value VG0 of 1.2V at absolute zero to a decreasing value with increased temperature.

If we take this equation and differentiate it with respect to temperature T, then:

$$\frac{dVD}{dT} = -\left(VG0 - VD\right) / T \quad \text{This} \quad \frac{dVD}{dT}$$

change as a function of temperature is the typical ~–2mV/°C. This equation is simplified for the first order derivation.

Solving for T, T = –(VG0 – VD)/ dVD provide the temperature.

1st Example: Figure 4 for 27°C, or 300°C Kelvin the diode voltage is 0.598V, thus, 300°C = –(1200mV – 598mV)/ –2mV/°C)

2nd Example: Figure 4 for 75°C, or 350°C Kelvin the diode voltage is 0.50V, thus, 350°C = –(1200mV – 500mV)/ –2mV/°C)

Converting the Kelvin scale to Celsius is simply taking the Kelvin temp and subtracting –273°C Kelvin from it.

A typical forward voltage is measured and placed in the electrical characteristics section of the data sheet, and Figure 8 is the plot of this forward voltage. Measure this forward voltage at 27°C to establish a reference point. Then use the above expression while measuring the forward voltage over temperature will provide a general temperature monitor.

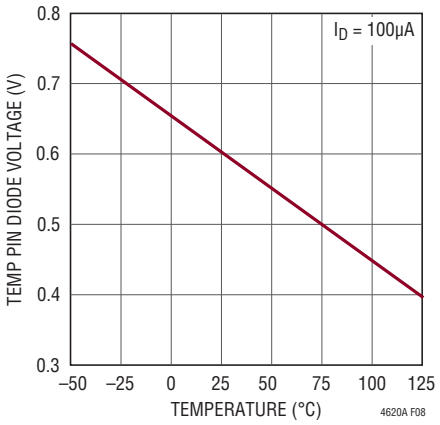

Figure 8. Diode Voltage V_D vs Temperature T(°C) for Different Bias Currents

The diode connected PNP transistor can be pulled up to V_{IN} with a resistor to set the current to 100µA for using this diode connected transistor as a general temperature monitor by monitoring the diode voltage drop with temperature. See Figure 27 for an example.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD 51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board—also defined by JESD 51-9 (“Test Boards for Area Array Surface Mount Package Thermal Measurements”). The motivation for providing these thermal coefficients in found in JESD 51-12 (“Guidelines for Reporting and Using Electronic Package Thermal Information”).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator’s thermal performance in their application at various electrical and environmental operating

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conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

4. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

A graphical representation of the aforementioned thermal resistances is given in Figure 9; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

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Within a SIP (system-in-package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD 51-9 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the µModule with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due-diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory test have been performed and correlated to the µModule model, then the θ_{JB} and θ_{BA} are summed together to correlate quite well with the µModule model with no airflow or heat sinking in a properly define chamber. This θ_{JB} + θ_{BA} value is shown in the Pin Configuration section and should accurately equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink. Each system has its own thermal characteristics, therefore thermal analysis must be performed by the user in a particular system.

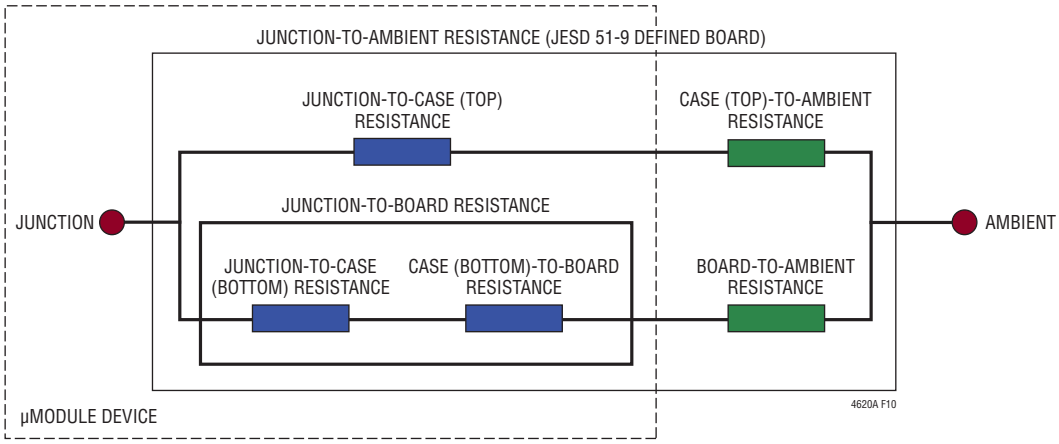

Figure 9. Graphical Representation of JESD 51-12 Thermal Coefficients

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The LTM4620A module has been designed to effectively remove heat from both the top and bottom of the package. The bottom substrate material has very low thermal resistance to the printed circuit board and the exposed top metal is thermally connected to the power devices and the power inductors. An external heat sink can be applied to the top of the device for excellent heat sinking with airflow. Basically all power dissipating devices are mounted directly to the substrate and the top exposed metal. This provides two low thermal resistance paths to remove heat.

Figure 10 shows a temperature plot of the LTM4620A with BGA heat sink and 200LFM airflow with ~5.3W of internal dissipation.

Figure 11 shows a temperature plot of the LTM4620A with no heat sink and 200LFM airflow with ~6.5W of internal dissipation.

These plots equate to a paralleled 1.2V at 26A design, and a 5V at 25A design operating from a 12V input.

Safety Considerations

The LTM4620A modules do not provide isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

The fuse or circuit breaker should be selected to limit the current to the regulator during overvoltage in case of an internal top MOSFET fault. If the internal top MOSFET fails, then turning it off will not resolve the overvoltage, thus the internal bottom MOSFET will turn on indefinitely trying to protect the load. Under this fault condition, the input voltage will source very large currents to ground through the failed internal top MOSFET and enabled internal bottom MOSFET. This can cause excessive heat and board damage depending on how much power the input voltage can deliver to this system. A fuse or circuit breaker can be used as a secondary fault protector in this situation.

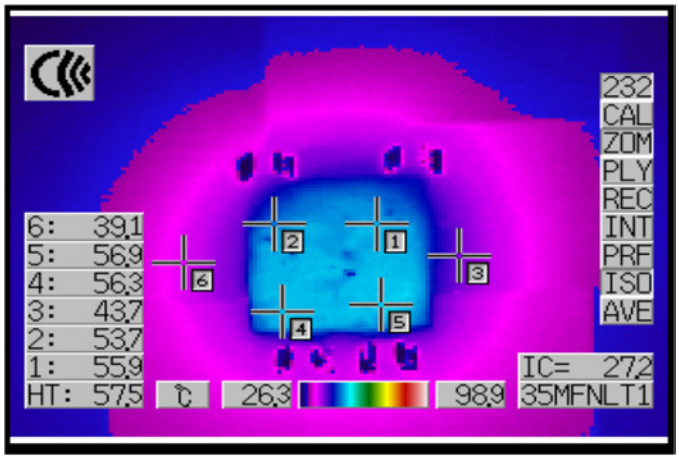

Figure 10. LTM4620A 12V to 1.2V at 26A with 200LFM Airflow

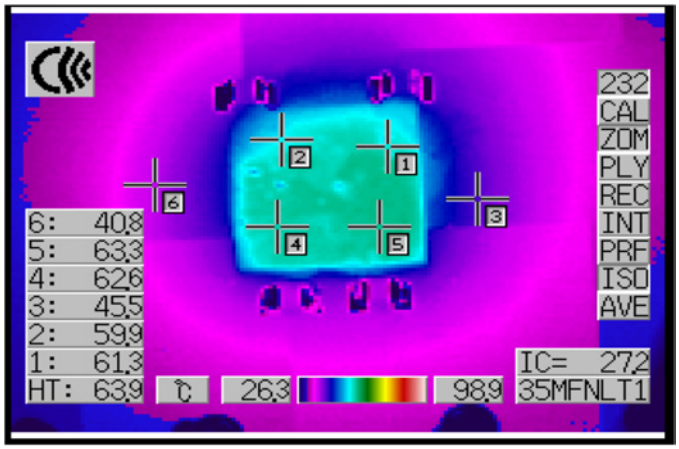

Figure 11. LTM4620A 12V to 5V at 25A with 200LFM Airflow

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The device does support over current protection. A temperature diode is provided for monitoring internal temperature, and can be used to detect the need for thermal shutdown that can be done by controlling the RUN pin.

Power Derating

The 1V, 2.5V and 5V power loss curves in Figures 12 to 14 can be used in coordination with the load current derating curves in Figures 15 to 24 for calculating an approximate θ_{JA} thermal resistance for the LTM4620A with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with a 1.35 to 1.4 multiplicative factor at 125°C. These factors come from the fact that the power loss of the regulator increases about 45% from 25°C to 150°C, thus a 45% spread over 125°C delta equates to ~0.35%/°C loss increase. A 125°C maximum junction minus 25°C room temperature equates to a 100°C increase. This 100°C increase multiplied by 0.35%/°C equals a 35% power loss increase at the 125°C junction, thus the 1.35 multiplier.

The derating curves are plotted with CH1 and CH2 in parallel single output operation starting at 26A of load with low ambient temperature. The output voltages are 1V, 2.5V and 5V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis.

The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at ~120°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased.

The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 15, the load current is derated to ~19A at ~80°C with no air or heat sink and the power loss for the 12V to 1.0V at 19A output is a ~5.1W loss. The 5.1W loss is calculated with the ~3.75W room temperature loss from the 12V to 1.0V power loss curve at 19A, and the 1.35 multiplying factor at 125°C ambient. If the 80°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 40°C divided 5.1W equals a 7.8°C/W θ_{JA} thermal resistance. Table 2 specifies a 6.5 to 7°C/W value which is pretty close. The airflow graphs are more accurate due to the fact that the ambient temperature environment is controlled better with airflow. As an example in Figure 16, the load current is derated to ~22A at ~90°C with 200LFM of airflow and the power loss for the 12V to 1.0V at 22A output is a ~5.94W loss.

The 5.94W loss is calculated with the ~4.4W room temperature loss from the 12V to 1.0V power loss curve at 22A, and the 1.35 multiplying factor at 125°C ambient. If the 90°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 30°C divided 5.94W equals a 5.1°C/W θ_{JA} thermal resistance. Table 2 specifies a 5.5°C/W value which is pretty close. Tables 2-4 provide equivalent thermal resistances for 1.0V, 2.5V and 5V outputs with and without airflow and heat sinking.

The derived thermal resistances in Tables 2-4 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick four layer board with two ounce copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are 101mm × 114mm. The BGA heat sinks are listed below Table 4.

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Table 2. 1.0V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	LGA θ_{JA} (°C/W)	BGA θ_{JA} (°C/W)
Figures 15, 16	5, 12	Figure 12	0	None	6.5 to 7	6.5 to 7
Figures 15, 16	5, 12	Figure 12	200	None	5.5	5.5
Figures 15, 16	5, 12	Figure 12	400	None	5	5
Figures 17, 18	5, 12	Figure 12	0	BGA Heat Sink	6.5	6.5
Figures 17, 18	5, 12	Figure 12	200	BGA Heat Sink	5	5
Figures 17, 18	5, 12	Figure 12	400	BGA Heat Sink	4	4

Table 3. 2.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	LGA θ_{JA} (°C/W)	BGA θ_{JA} (°C/W)
Figures 19, 20	5, 12	Figure 13	0	None	6.5 to 7	6.5 to 7
Figures 19, 20	5, 12	Figure 13	200	None	5.5 to 6	5.5 to 6
Figures 19, 20	5, 12	Figure 13	400	None	4.5	4.5
Figures 21, 22	5, 12	Figure 13	0	BGA Heat Sink	6.5 to 7	6.5 to 7
Figures 21, 22	5, 12	Figure 13	200	BGA Heat Sink	4	4
Figures 21, 22	5, 12	Figure 13	400	BGA Heat Sink	3.5	3.5

Table 4. 5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	LGA θ_{JA} (°C/W)	BGA θ_{JA} (°C/W)
Figure 23	12	Figure 14	0	None	6.5 to 7	6.5 to 7
Figure 23	12	Figure 14	200	None	5.5 to 6	5.5 to 6
Figure 23	12	Figure 14	400	None	4.5	4.5
Figure 24	12	Figure 14	0	BGA Heat Sink	6.5 to 7	6.5 to 7
Figure 24	12	Figure 14	200	BGA Heat Sink	4	4
Figure 24	12	Figure 14	400	BGA Heat Sink	3.5	3.5

Connect 5V output to $EXTV_{CC}$ to increase efficiency.

HEAT SINK MANUFACTURER	PART NUMBER	WEBSITE
Aavid Thermalloy	375424B00034G	www.aavid.com
Cool Innovations	4-050503P 4-050508P	www.coolinnovations.com

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Table 5. Output Voltage Response vs Component Matrix (Refer to Figure 23) 0A to 7A Load Step Typical Measured Values

VENDORS	VALUE	PART NUMBER	ESR
TDK, C_{OUT1} Ceramic	100µF 6.3V	C4532X5R0J107MZ	~1mΩ
Murata, C_{OUT1} Ceramic	100µF 6.3V	GRM32ER60J107M	~1mΩ
AVX, C_{OUT1} Ceramic	100µF 6.3V	18126D107MAT	~1mΩ
Sanyo POSCAP, C_{OUT2} Bulk	470µF 2R5	2R5TPD470M5	9mΩ
Sanyo POSCAP, C_{OUT2} Bulk	470µF 6.3V	6TPD470M	9mΩ
Sanyo, C_{IN} Bulk	56µF 25V	25SVP56M	
Sanyo, POSCAP C_{OUT2} Bulk	100µF 6.3V	67PE100MI	15mΩ to 18mΩ
Sanyo, POSCAP C_{OUT2} Bulk	220µF 2.5V	2R5TPE220M9	
Sanyo, POSCAP C_{OUT2} Bulk	220µF 6V	6TPF220ML	

V_{OUT} (V)	C_{IN} (CERAMIC)	C_{IN} (BULK)**	C_{OUT1} (CERAMIC)	C_{OUT2} (BULK)	C_{FF} (pF)	C_{BOT} (pF)	C_{COMP} (pF)	V_{IN} (V)	DROOP (mV)	P-P DEVIATION AT 6A LOAD STEP (mV)	RECOVERY TIME (µs)	LOAD STEP (A/µs)	R_{FB} (kΩ)	FREQ
1	22µF × 3	56µF	100µF	470µF × 2	None	None	None	5	24	46	30	6	90.9	400
1	22µF × 3	56µF	100µF	470µF × 2	150	None	None	12	24	46	30	6	90.9	400
1	22µF × 3	56µF	100µF × 3	470µF	100	None	None	12	33	63	23	6	90.9	400
1.2	22µF × 3	56µF	100µF × 3	470µF	100	None	None	12	35	70	23	6	60.4	500
1.2	22µF × 3	56µF	100µF	470µF × 2	150			5	24	46	25	6	60.4	500
1.2	22µF × 3	56µF	100µF	470µF × 2	150			12	24	46	25	6	60.4	500
1.5	22µF × 3	56µF	100µF	470µF × 2	220	None		5	26	52	40	6	40.2	550
1.5	22µF × 3	56µF	100µF	470µF × 2	220			12	26	52	40	6	40.2	550
1.5	22µF × 3	56µF	100µF	220µF	47			12	64	120	20	6	40.2	500
1.8	22µF × 3	56µF	100µF	220µF	33			12	61	120	20	6	30.2	600
1.8	22µF × 3	56µF	100µF	220µF	33			5	61	120	20	6	30.2	600
1.8	22µF × 3	56µF	100µF × 3	None	100			12	80	160	18	6	30.2	600
2.5	22µF × 3	56µF	100µF × 3	None	150	None	47	12	60	120	20	6	19.1	650
2.5	22µF × 3	56µF	100µF × 3	None	150	None	47	12	60	120	20	6	19.1	650
3.3	22µF × 3	56µF	100µF	100µF	33			12	118	240	30	6	13.3	700
3.3	22µF × 3	56µF	100µF × 2		100			12	120	240	20	6	13.3	700
5	22µF × 3	56µF	100µF		47			12	188	382	25	6	8.25	750
5	22µF × 3	56µF		100µF				12	180	360	20	6	8.25	750

**Bulk capacitance is optional if V_{IN} has very low input impedance.

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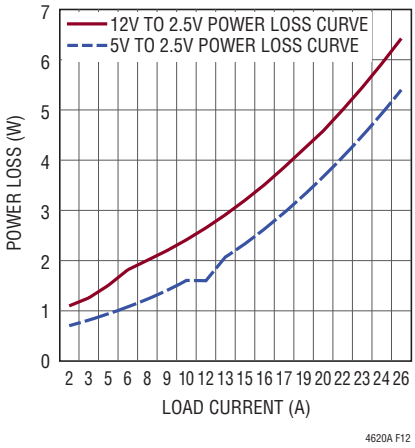

Figure 12. 2.5V Power Loss Curve

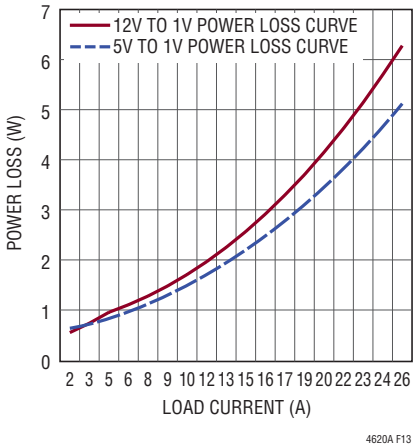

Figure 13. 1V Power Loss Curve

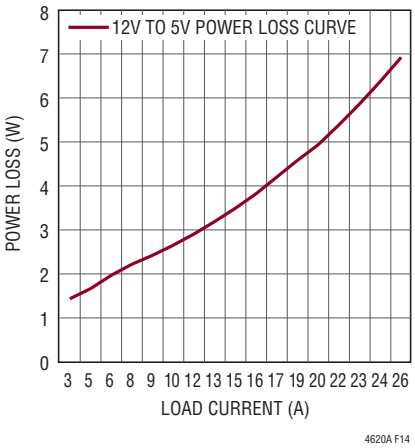

Figure 14. 5V Power Loss Curve

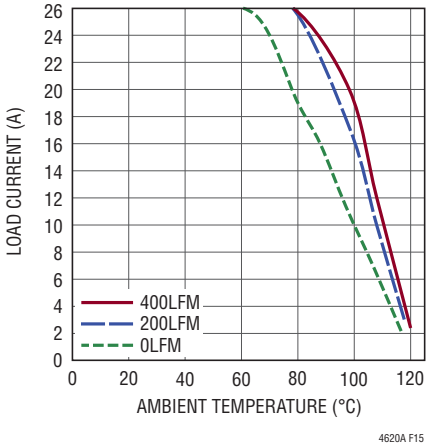

Figure 15. 12V to 1V Derating Curve, No Heat Sink

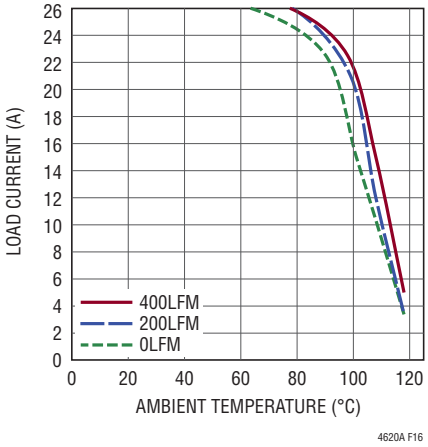

Figure 16. 5V to 1V Derating Curve, No Heat Sink

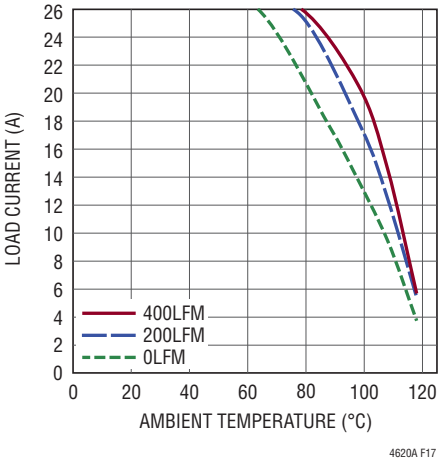

Figure 17. 12V to 1V Derating Curve, BGA Heat Sink

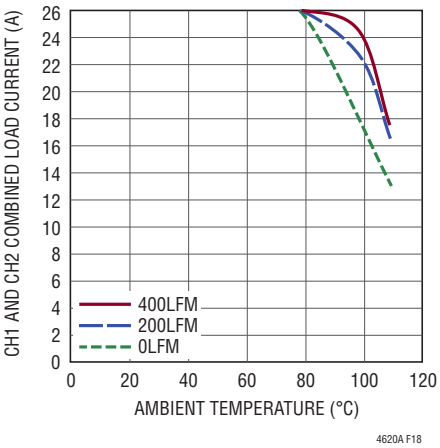

Figure 18. 5V to 1V Derating Curve, BGA Heat Sink

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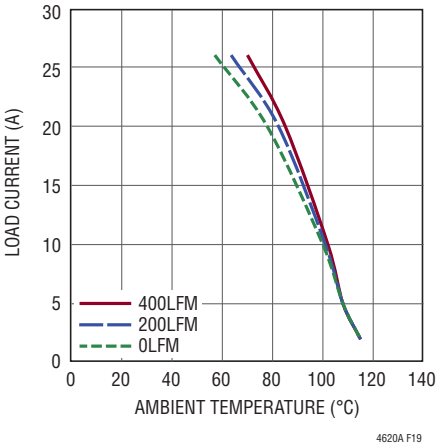

Figure 19. 12V to 2.5V Derating Curve, No Heat Sink

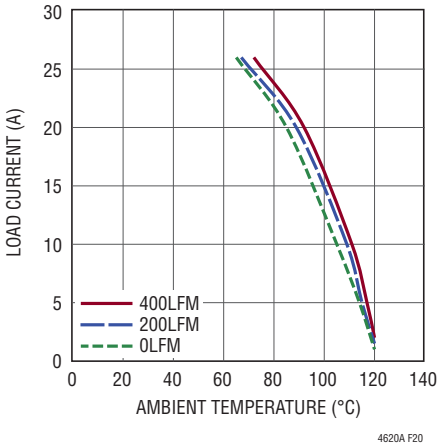

Figure 20. 5V to 2.5V Derating Curve, No Heat Sink

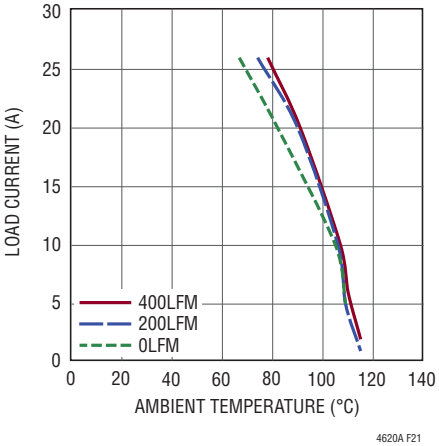

Figure 21. 12V to 2.5V Derating Curve, with Heat Sink

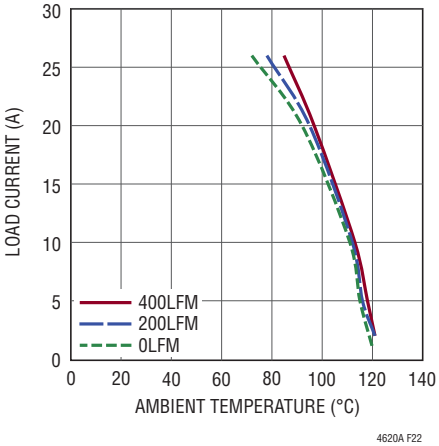

Figure 22. 5V to 2.5V Derating Curve, with Heat Sink

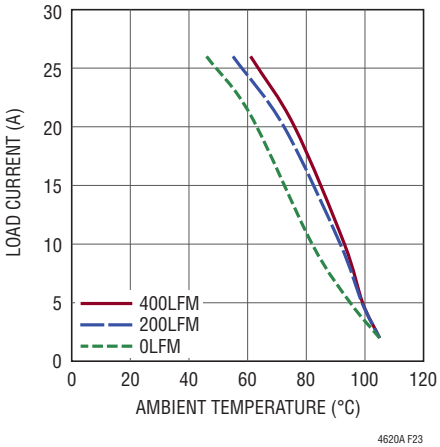

Figure 23. 12V to 5V Derating Curve, No Heat Sink

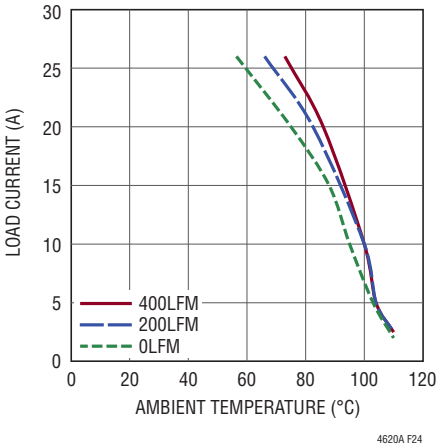

Figure 24. 12V to 5V Derating Curve, with Heat Sink

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APPLICATIONS INFORMATION

Layout Checklist/Example

The high integration of LTM4620A makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND, V_{OUT1} and V_{OUT2}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie the V_{OUT}, V_{FB}, and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK pin can be tied a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.

Figure 25 gives a good example of the recommended layout.

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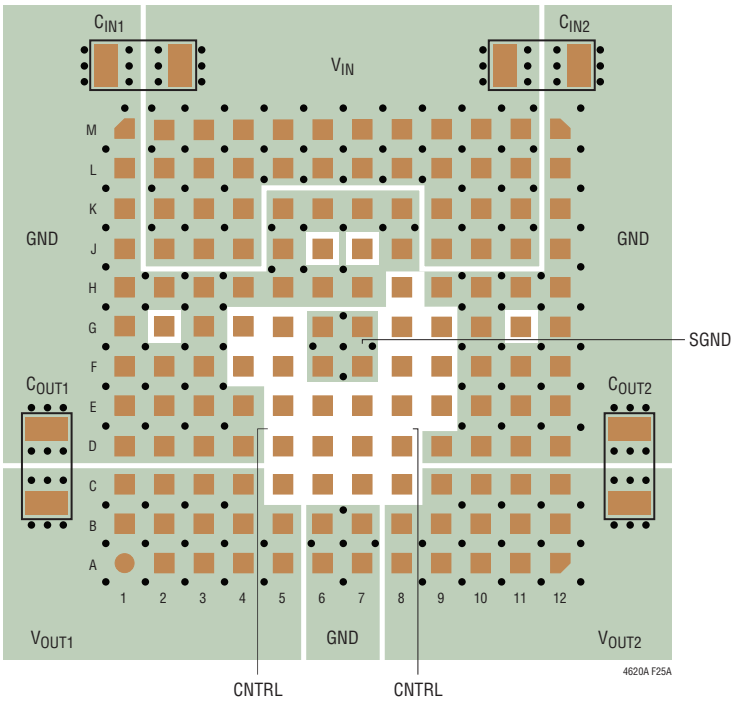
APPLICATIONS INFORMATION

LGA



BGA

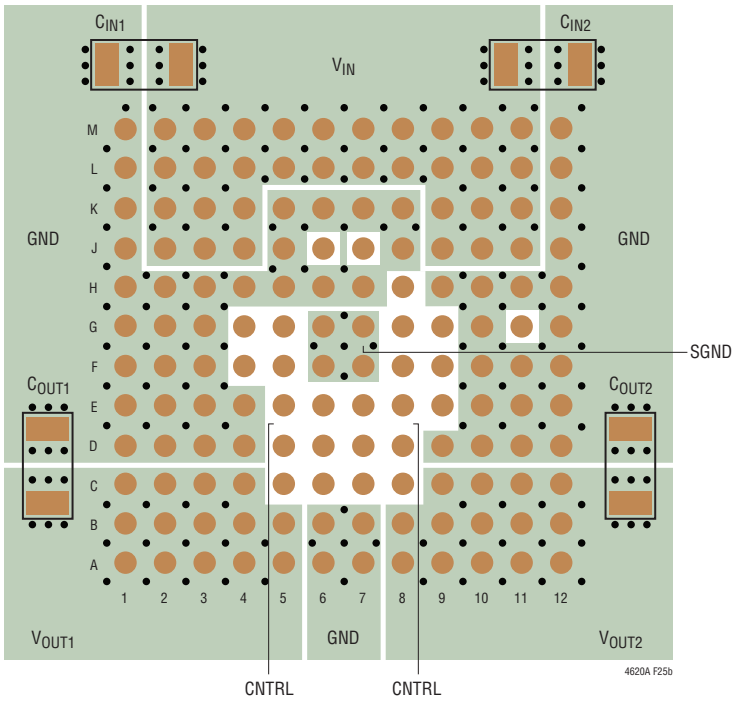


Figure 25. Recommended PCB Layout

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APPLICATIONS INFORMATION

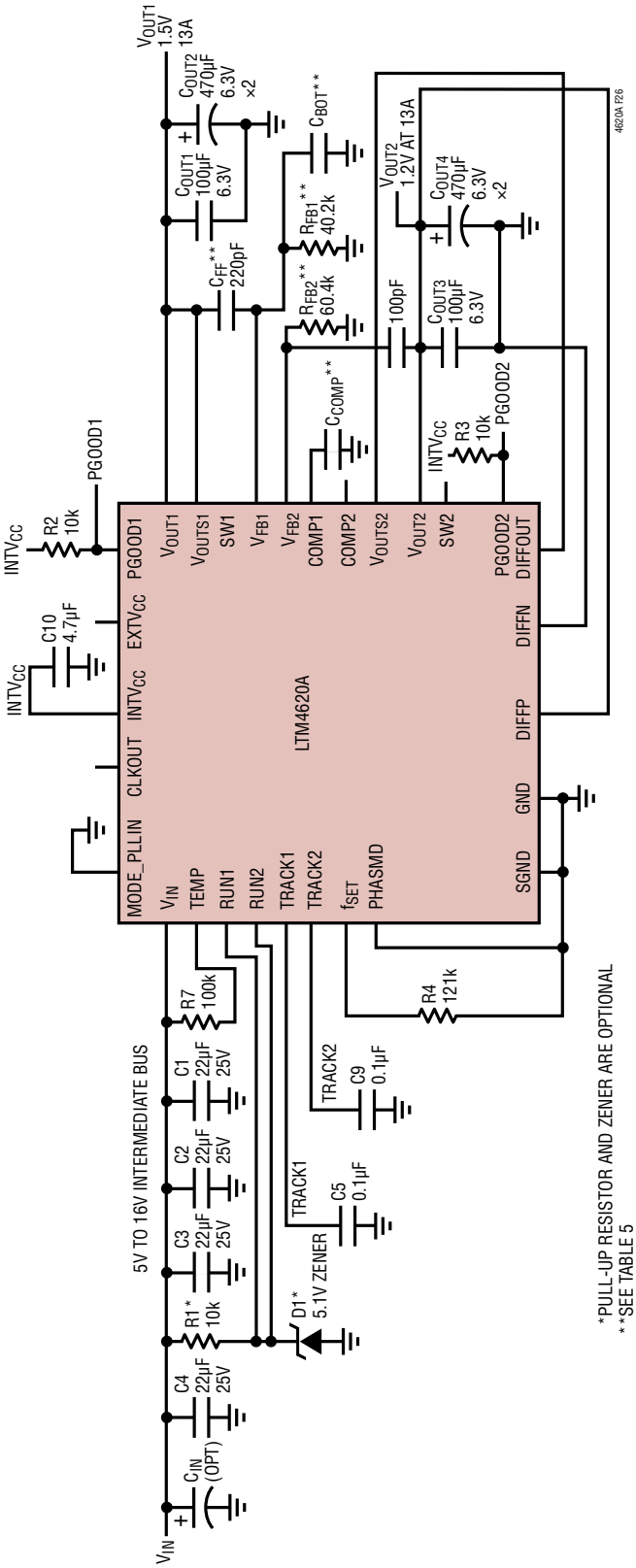

Figure 26. Typical $5V_{IN}$ to $16V_{IN}$, 1.5V and 1.2V Outputs

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TYPICAL APPLICATIONS

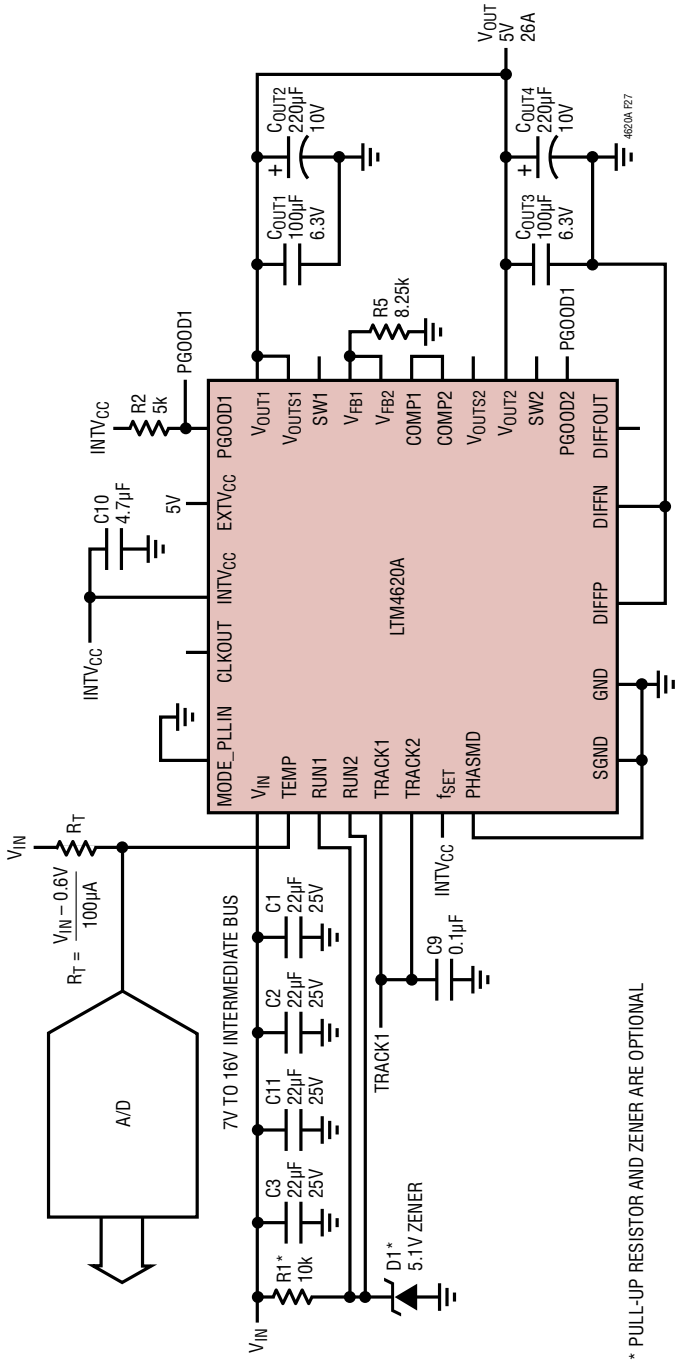

Figure 27. LTM4620A 2-Phase, 5V at 20A Design with Temperature Monitoring

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TYPICAL APPLICATIONS

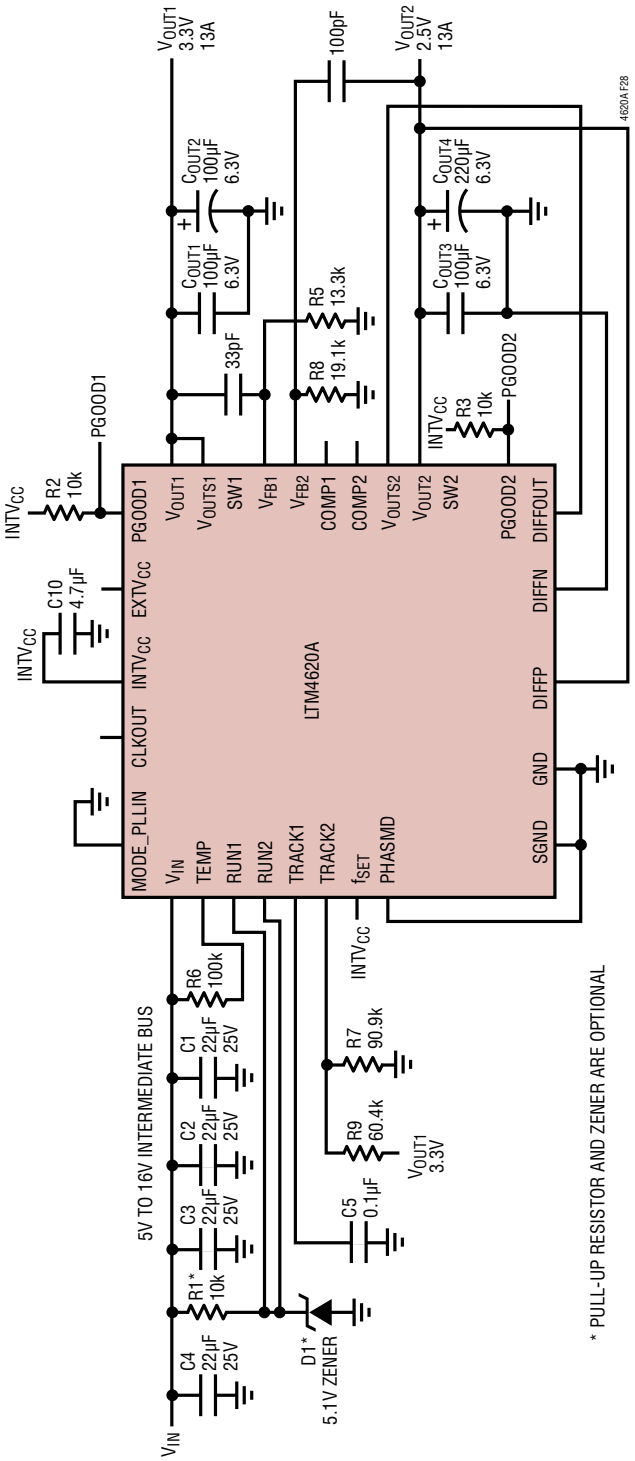

Figure 28. LTM4620A 3.3V and 2.5V Output Tracking

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TYPICAL APPLICATIONS

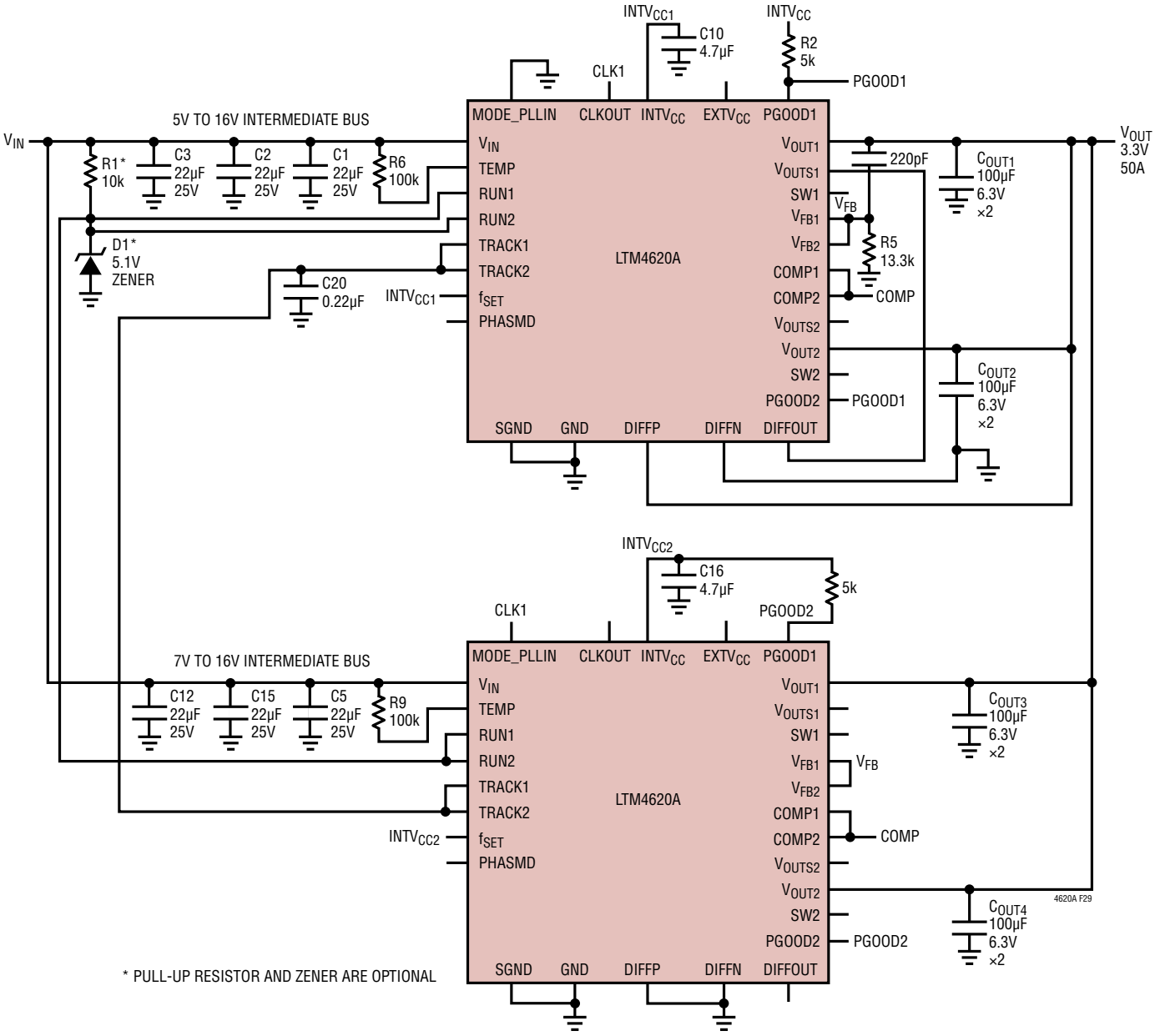

Figure 29. 4-Phase, 3.3V at 50A, 750kHz

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PACKAGE DESCRIPTION

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

LTM4620A Component LGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT1}	B1	V_{OUT1}	C1	V_{OUT1}	D1	GND	E1	GND	F1	GND
A2	V_{OUT1}	B2	V_{OUT1}	C2	V_{OUT1}	D2	GND	E2	GND	F2	GND
A3	V_{OUT1}	B3	V_{OUT1}	C3	V_{OUT1}	D3	GND	E3	GND	F3	GND
A4	V_{OUT1}	B4	V_{OUT1}	C4	V_{OUT1}	D4	GND	E4	GND	F4	MODE_PLLIN
A5	V_{OUT1}	B5	V_{OUT1}	C5	V_{OUT1S}	D5	V_{FB1}	E5	TRACK1	F5	RUN1
A6	GND	B6	GND	C6	f_{SET}	D6	SGND	E6	COMP1	F6	SGND
A7	GND	B7	GND	C7	SGND	D7	V_{FB2}	E7	COMP2	F7	SGND
A8	V_{OUT2}	B8	V_{OUT2}	C8	V_{OUT2S}	D8	TRACK2	E8	DIFFP	F8	DIFFOUT
A9	V_{OUT2}	B9	V_{OUT2}	C9	V_{OUT2}	D9	GND	E9	DIFFN	F9	RUN2
A10	V_{OUT2}	B10	V_{OUT2}	C10	V_{OUT2}	D10	GND	E10	GND	F10	GND
A11	V_{OUT2}	B11	V_{OUT2}	C11	V_{OUT2}	D11	GND	E11	GND	F11	GND
A12	V_{OUT2}	B12	V_{OUT2}	C12	V_{OUT2}	D12	GND	E12	GND	F12	GND

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	GND	H1	GND	J1	GND	K1	GND	L1	GND	M1	GND
G2	SW1	H2	GND	J2	V_{IN}	K2	V_{IN}	L2	V_{IN}	M2	V_{IN}
G3	GND	H3	GND	J3	V_{IN}	K3	V_{IN}	L3	V_{IN}	M3	V_{IN}
G4	PHASEMD	H4	GND	J4	V_{IN}	K4	V_{IN}	L4	V_{IN}	M4	V_{IN}
G5	CLKOUT	H5	GND	J5	GND	K5	GND	L5	V_{IN}	M5	V_{IN}
G6	SGND	H6	GND	J6	TEMP	K6	GND	L6	V_{IN}	M6	V_{IN}
G7	SGND	H7	GND	J7	$EXTV_{CC}$	K7	GND	L7	V_{IN}	M7	V_{IN}
G8	PGOOD2	H8	$INTV_{CC}$	J8	GND	K8	GND	L8	V_{IN}	M8	V_{IN}
G9	PGOOD1	H9	GND	J9	V_{IN}	K9	V_{IN}	L9	V_{IN}	M9	V_{IN}
G10	GND	H10	GND	J10	V_{IN}	K10	V_{IN}	L10	V_{IN}	M10	V_{IN}
G11	SW2	H11	GND	J11	V_{IN}	K11	V_{IN}	L11	V_{IN}	M11	V_{IN}
G12	GND	H12	GND	J12	GND	K12	GND	L12	GND	M12	GND

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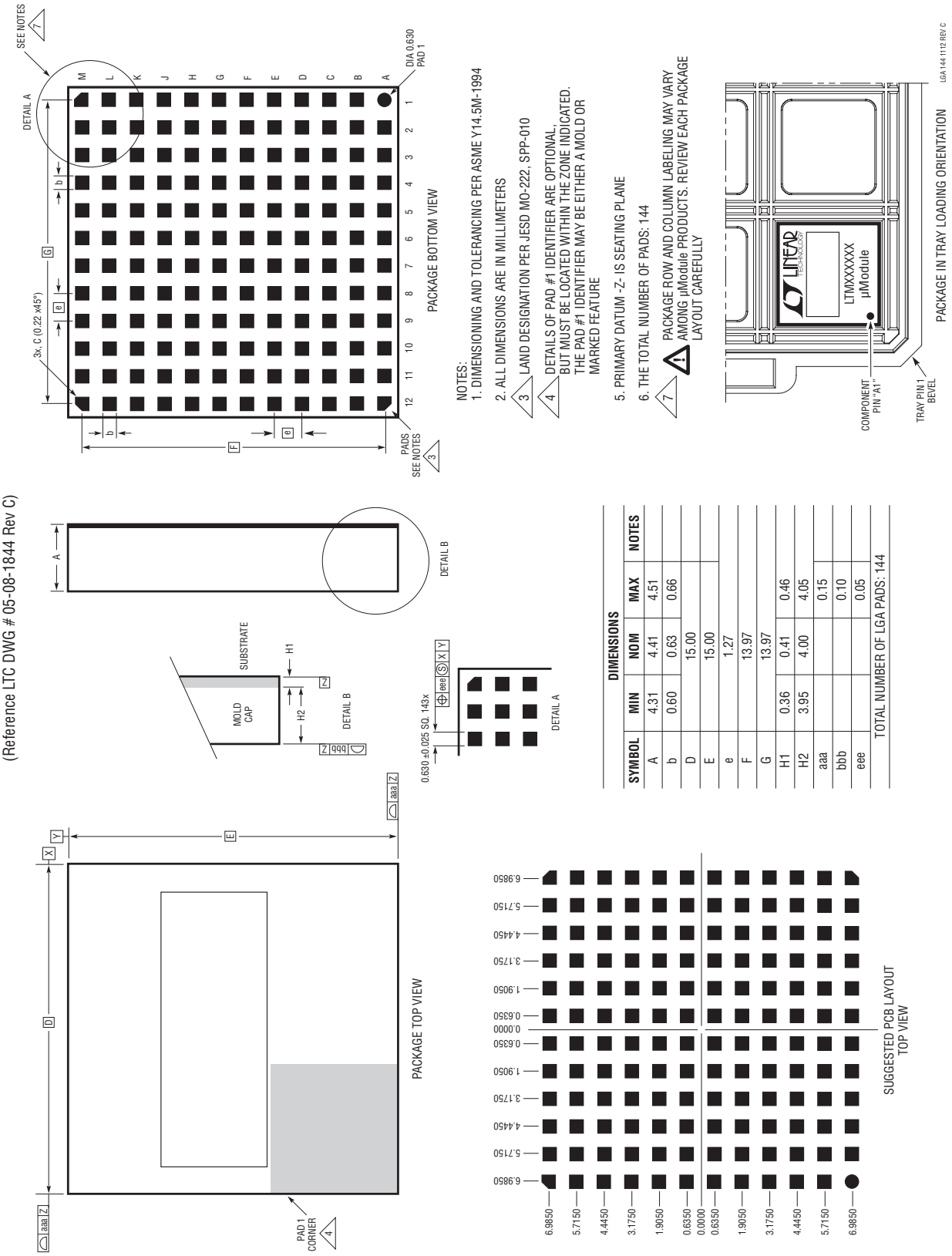
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTM4620A#packaging for the most recent package drawings.



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.31	4.41	4.51	
b	0.60	0.63	0.66	
D		15.00		
E		15.00		
e		1.27		
F		13.97		
G		13.97		
H1	0.36	0.41	0.46	
H2	3.95	4.00	4.05	
aaa			0.15	
bbb			0.10	
eee			0.05	
TOTAL NUMBER OF LGA PADS: 144				

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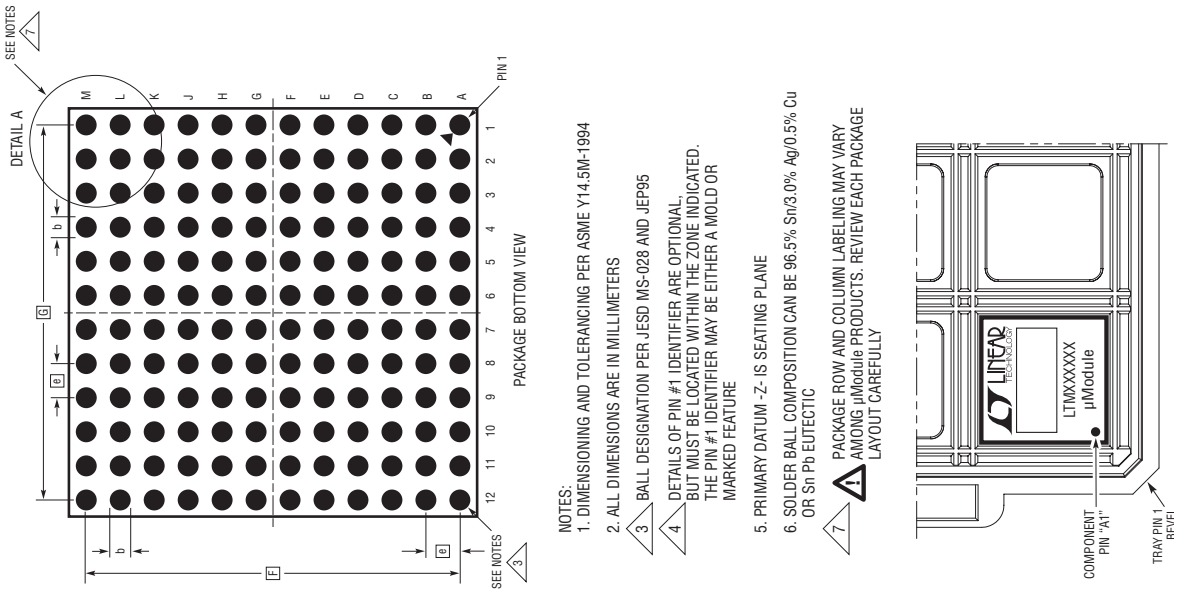
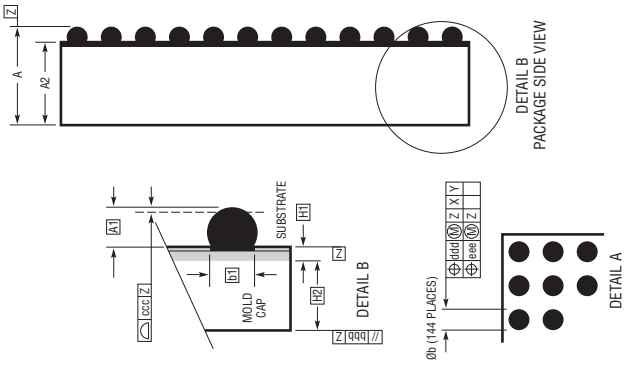
PACKAGE DESCRIPTION

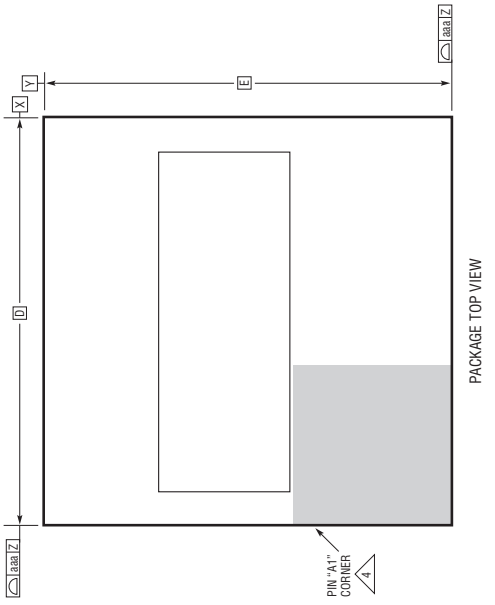
Please refer to http://www.linear.com/product/LTM4620A#packaging for the most recent package drawings.

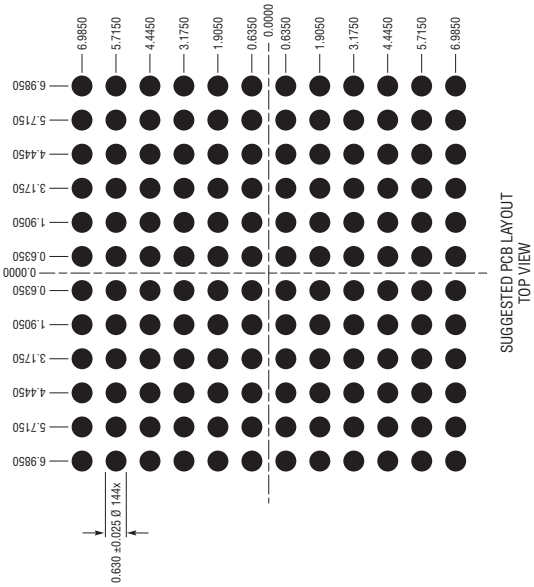


BGA Package
144-Lead (15mm × 15mm × 5.01mm)
(Reference LTC DWG # 05-08-1880 Rev C)



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.81	5.01	5.21	
A1	0.50	0.60	0.70	BALL HT
A2	4.31	4.41	4.51	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		15.00		
E		15.00		
e		1.27		
F		13.97		
G		13.97		
H1	0.36	0.41	0.46	SUBSTRATE THK
H2	3.95	4.00	4.05	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
	TOTAL NUMBER OF BALLS: 144			





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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/13	Added explanation for TEMP pin Changed TEMP explanation and formulas	11 20, 21
B	03/14	Add SnPb BGA package option	1, 2
C	06/17	Added LTM4620AY MP-Grade to the Order Information	2

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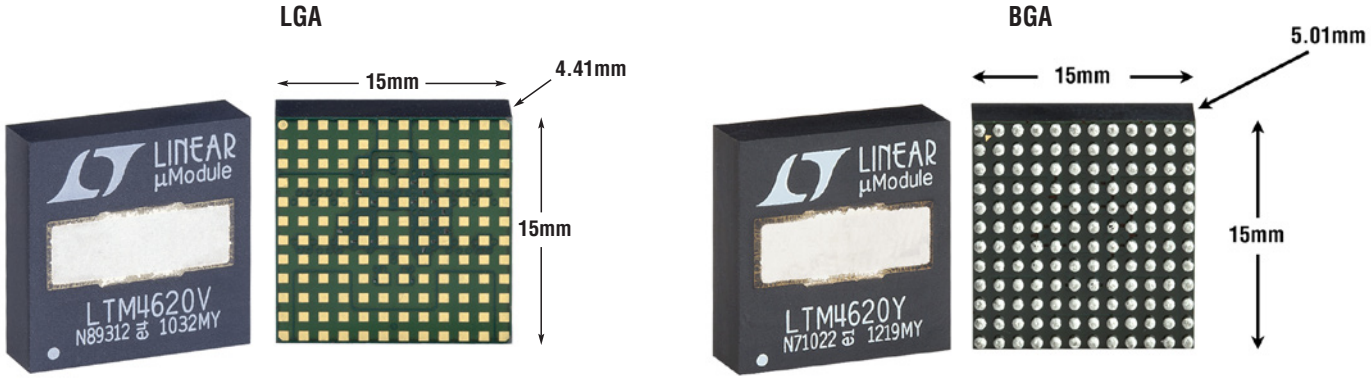
PACKAGE PHOTO



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4628	Dual 8A, Single 16A µModule Regulator	Pin Compatible with LTM4620A; 4.5V ≤ V_{IN} ≤ 26.5V, 0.6V ≤ V_{OUT} ≤ 5.5V, 15mm × 15mm × 4.32mm
LTM4627	15A µModule Regulator	4.5V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 15mm × 15mm × 4.32mm
LTM4611	Ultralow V_{IN}, 15A µModule Regulator	1.5V ≤ V_{IN} ≤ 5.5V, 0.8V ≤ V_{OUT} ≤ 5V, 15mm × 15mm × 4.32mm
LTM4620	Dual 13A or Single 26A	Lower Output Voltage Range, 0.6V to 2.5V, Pin Compatible
LTM4637	20A µModule Regulator	4.5V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 15mm × 15mm × 4.32mm

DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. Quick Power Search Input V_{in} (Min) V V_{in} (Max) V Output V_{out} V I_{out} A Search	
TechClip Videos	Quick videos detailing how to bench test electrical and thermal performance of µModule products.	
Digital Power System Management	Linear Technology's family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

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