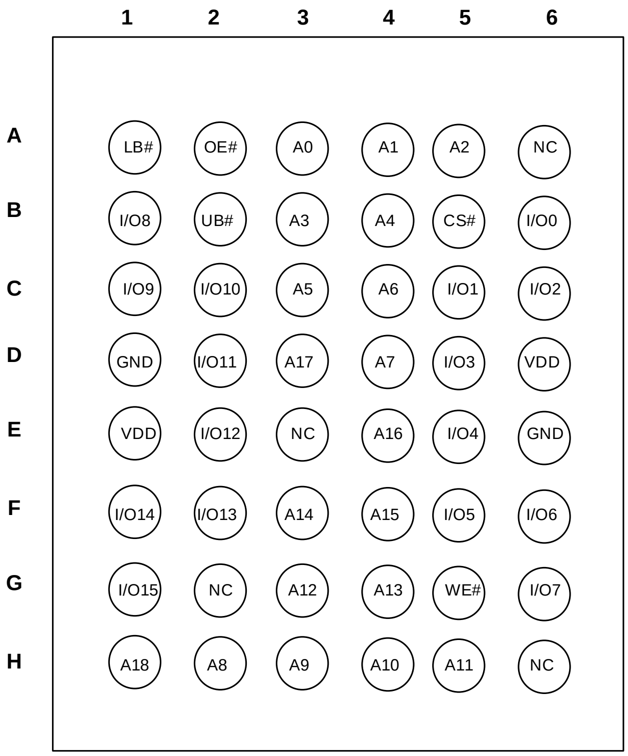
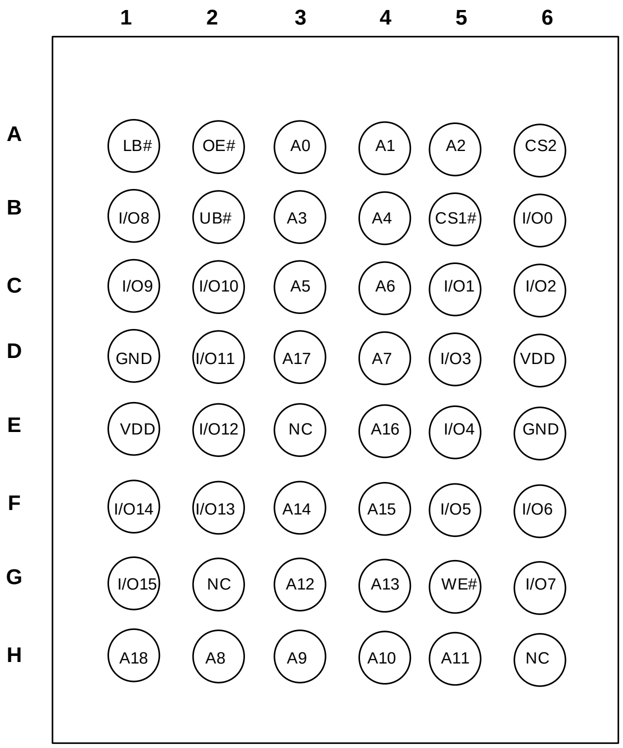
PIN CONFIGURATIONS

48-Pin mini BGA (6mm x 8mm), 1 CS



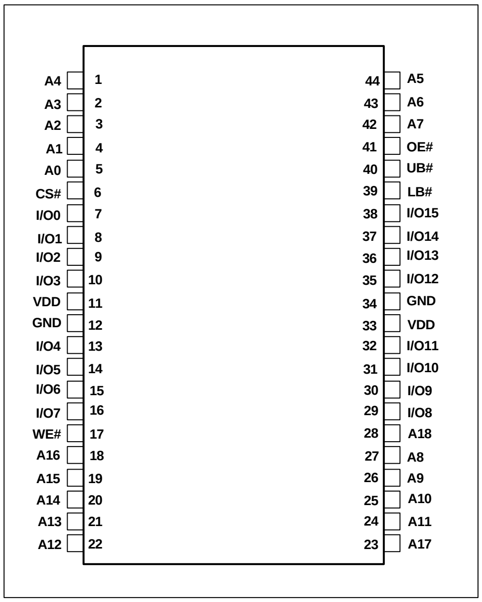
	1	2	3	4	5	6
A	LB#	OE#	A0	A1	A2	NC
B	I/O8	UB#	A3	A4	CS#	I/O0
C	I/O9	I/O10	A5	A6	I/O1	I/O2
D	GND	I/O11	A17	A7	I/O3	VDD
E	VDD	I/O12	NC	A16	I/O4	GND
F	I/O14	I/O13	A14	A15	I/O5	I/O6
G	I/O15	NC	A12	A13	WE#	I/O7
H	A18	A8	A9	A10	A11	NC

48-Pin mini BGA (6mm x 8mm), 2 CS



	1	2	3	4	5	6
A	LB#	OE#	A0	A1	A2	CS2
B	I/O8	UB#	A3	A4	CS1#	I/O0
C	I/O9	I/O10	A5	A6	I/O1	I/O2
D	GND	I/O11	A17	A7	I/O3	VDD
E	VDD	I/O12	NC	A16	I/O4	GND
F	I/O14	I/O13	A14	A15	I/O5	I/O6
G	I/O15	NC	A12	A13	WE#	I/O7
H	A18	A8	A9	A10	A11	NC

44-Pin TSOP (TYPE II)



A4	1	44	A5
A3	2	43	A6
A2	3	42	A7
A1	4	41	OE#
A0	5	40	UB#
CS#	6	39	LB#
I/O0	7	38	I/O15
I/O1	8	37	I/O14
I/O2	9	36	I/O13
I/O3	10	35	I/O12
VDD	11	34	GND
GND	12	33	VDD
I/O4	13	32	I/O11
I/O5	14	31	I/O10
I/O6	15	30	I/O9
I/O7	16	29	I/O8
WE#	17	28	A18
A16	18	27	A8
A15	19	26	A9
A14	20	25	A10
A13	21	24	A11
A12	22	23	A17

PIN DESCRIPTIONS

A0-A18	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CS# or CS1# & CS2	Chip Enable Inputs
OE#	Output Enable Input
WE#	Write Enable Input
LB#	Lower-byte Control (I/O0-I/O7)
UB#	Upper-byte Control (I/O8-I/O15)
NC	No Connection
VDD	Power
GND	Ground

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FUNCTION DESCRIPTION

SRAM is one of random access memories. Each byte or word has an address and can be accessed randomly. SRAM has three different modes supported. Each function is described below with Truth Table.
All function description including Table is based on 2 Chip Select option.

STANDBY MODE

Device enters standby mode when deselected (CS1# HIGH or CS2 LOW or both UB# and LB# are HIGH). The input and output pins (I/O0-15) are placed in a high impedance state. The current consumption in this mode will be ISB1 or ISB2. CMOS input in this mode will maximize saving power.

WRITE MODE

Write operation issues with Chip selected (CS1# LOW and CS2 HIGH) and Write Enable (WE#) input LOW. The input and output pins (I/O0-15) are in data input mode. Output buffers are closed during this time even if OE# is LOW. UB# and LB# enables a byte write feature. By enabling LB# LOW, data from I/O pins (I/O0 through I/O7) are written into the location specified on the address pins. And with UB# being LOW, data from I/O pins (I/O8 through I/O15) are written into the location.

READ MODE

Read operation issues with Chip selected (CS1# LOW and CS2 HIGH) and Write Enable (WE#) input HIGH. When OE# is LOW, output buffer turns on to make data output. Any input to I/O pins during READ mode is not permitted. UB# and LB# enables a byte read feature. By enabling LB# LOW, data from memory appears on I/O0-7. And with UB# being LOW, data from memory appears on I/O8-15.

In the READ mode, output buffers can be turned off by pulling OE# HIGH. In this mode, internal device operates as READ but I/Os are in a high impedance state. Since device is in READ mode, active current is used.

TRUTH TABLE

Mode	CS1#	CS2	WE#	OE#	LB#	UB#	I/O0-I/O7	I/O8-I/O15	VDD Current
Not Selected	H	X	X	X	X	X	High-Z	High-Z	ISB2
	X	L	X	X	X	X	High-Z	High-Z	
	X	X	X	X	H	H	High-Z	High-Z	
Output Disabled	L	H	H	H	L	X	High-Z	High-Z	ICC,ICC1
	L	H	H	H	X	L	High-Z	High-Z	
Read	L	H	H	L	L	H	DOUT	High-Z	ICC,ICC1
	L	H	H	L	H	L	High-Z	DOUT	
	L	H	H	L	L	L	DOUT	DOUT	
Write	L	H	L	X	L	H	DIN	High-Z	ICC,ICC1
	L	H	L	X	H	L	High-Z	DIN	
	L	H	L	X	L	L	DIN	DIN	

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ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
Vterm	Terminal Voltage with Respect to GND	–0.5 to V_{DD} + 0.5V	V
V_{DD}	V_{DD} Related to GND	–0.3 to 4.0	V
tStg	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE(1)

Range	Ambient Temperature	PART NUMBER	SPEED (MAX)	VDD(MIN)	VDD(TYP)	VDD(MAX)
Commercial	0°C to +70°C	~ALL	55ns	1.65V	1.8V	2.2V
Industrial	-40°C to +85°C		55ns	1.65V	1.8V	2.2V
Automotive	-40°C to +125°C		55ns	1.65V	1.8V	2.2V
Commercial	0°C to +70°C	~BLL	45ns	2.2V	3.0V	3.6V
Industrial	-40°C to +85°C		45ns	2.2V	3.0V	3.6V
Automotive	-40°C to +125°C		55ns	2.2V	3.0V	3.6V

Note:

1. Full device AC operation assumes a 100 µs ramp time from 0 to Vcc(min) and 200 µs wait time after Vcc stabilization.

PIN CAPACITANCE (1)

Parameter	Symbol	Test Condition	Max	Units
Input capacitance	C_{IN}	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DD}(typ)	6	pF
DQ capacitance (IO0–IO15)	$C_{I/O}$		8	pF

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

THERMAL CHARACTERISTICS (1)

Parameter	Symbol	Rating	Units
Thermal resistance from junction to ambient (airflow = 1m/s)	$R_{\theta JA}$	TBD	°C/W
Thermal resistance from junction to pins	$R_{\theta JB}$	TBD	°C/W
Thermal resistance from junction to case	$R_{\theta JC}$	TBD	°C/W

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

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AC TEST CONDITIONS (OVER THE OPERATING RANGE)

Parameter	**Unit (1.65V~2.2V)**	**Unit (2.2V~3.6V)**
Input Pulse Level	0V to V_{DD} -0.2V	0V to V_{DD} -0.3V
Input Rise and Fall Time	1V/ns	1V/ns
Output Timing Reference Level	0.9V	½ V_{DD}
R1	13500	1005
R2	10800	820
V_{TM}	1.8V	3.0V
Output Load Conditions	Refer to Figure 1 and 2	

OUTPUT LOAD CONDITIONS FIGURES

FIGURE 1

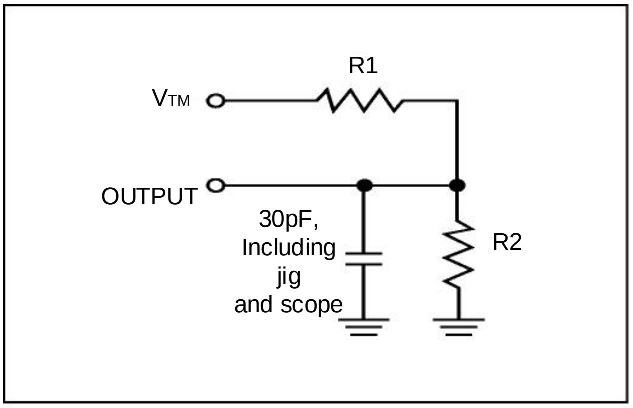
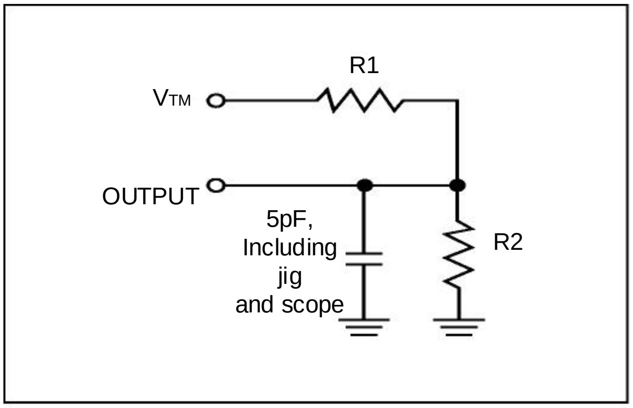


FIGURE 2



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DC ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

VDD = 1.65V ~ 2.2V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	—	0.2	V
$V_{IH}^{(1)}$	Input HIGH Voltage		1.4	V_{DD} + 0.2	V
$V_{IL}^{(1)}$	Input LOW Voltage		–0.2	0.4	V
I_{LI}	Input Leakage	GND < V_{IN} < V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND < V_{IN} < V_{DD}, Output Disabled	–1	1	µA

Notes:
1. VILL(min) = -1.0V AC (pulse width < 10ns). Not 100% tested.
VIHH (max) = VDD + 1.0V AC (pulse width < 10ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

VDD = 2.2V ~ 3.6V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	2.2 ≤ V_{DD} < 2.7, I_{OH} = -0.1 mA	2.0	—	V
		2.7 ≤ V_{DD} ≤ 3.6, I_{OH} = -1.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	2.2 ≤ V_{DD} < 2.7, I_{OL} = 0.1 mA	—	0.4	V
		2.7 ≤ V_{DD} ≤ 3.6, I_{OL} = 2.1 mA	—	0.4	V
$V_{IH}^{(1)}$	Input HIGH Voltage	2.2 ≤ V_{DD} < 2.7	1.8	V_{DD} + 0.3	V
		2.7 ≤ V_{DD} ≤ 3.6	2.0	V_{DD} + 0.3	V
$V_{IL}^{(1)}$	Input LOW Voltage	2.2 ≤ V_{DD} < 2.7	–0.3	0.6	V
		2.7 ≤ V_{DD} ≤ 3.6	–0.3	0.8	V
I_{LI}	Input Leakage	GND < V_{IN} < V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND < V_{IN} < V_{DD}, Output Disabled	–1	1	µA

Notes:
1. VILL(min) = -2.0V AC (pulse width < 10ns). Not 100% tested.
VIHH (max) = VDD + 2.0V AC (pulse width < 10ns). Not 100% tested.

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DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

IS62/65WV51216HALL (VDD = 1.65V ~ 2.2V)

Symbol	Parameter	Test Conditions	Grade		Typ(1)	Max	Unit
ICC	V_{DD} Dynamic Operating Supply Current	$V_{DD} = V_{DD}$ (max), $I_{OUT} = 0$mA, f = f_{max}	Com.		-	25	mA
			Ind.		-	25	
			Auto. A3		-	25	
ICC1	V_{DD} Static Operating Supply Current	$V_{DD} = V_{DD}$ (max), $I_{OUT} = 0$mA, f = 0	Com.		-	6	mA
			Ind.		-	6	
			Auto. A3		-	6	
ISB2	CMOS Standby Current (CMOS Inputs)	$V_{DD} = V_{DD}$ (max), (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ V_{DD} - 0.2V, CS2 ≥ V_{DD} - 0.2V or (3) LB# and UB# ≥ V_{DD} - 0.2V CS1# ≤ 0.2V, CS2 ≥ V_{DD} - 0.2V, f = 0	Com.	25°C	3.2	6	µA
				40°C	3.4	8	
				70°C	5.0	11	
			Ind.	85°C	6.6	14	
			Auto. A3	125°C	18.0	35	

Notes:
1. Typical value indicates the value for the center of distribution at V_{DD}=V_{DD} (Typ.), and not 100% tested.
2. Maximum value at 25°C, 40°C are guaranteed by design, and not 100% tested.

DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

IS62/65WV51216HBLL (VDD = 2.2V ~ 3.6V)

Symbol	Parameter	Test Conditions	Grade		Typ(1)	Max	Unit
ICC	V_{DD} Dynamic Operating Supply Current	$V_{DD} = V_{DD}$ (max), $I_{OUT} = 0$mA, f = f_{max}	Com.		-	25	mA
			Ind.		-	25	
			Auto. A3		-	25	
ICC1	V_{DD} Static Operating Supply Current	$V_{DD} = V_{DD}$ (max), $I_{OUT} = 0$mA, f = 0	Com.		-	6	mA
			Ind.		-	6	
			Auto. A3		-	6	
ISB2	CMOS Standby Current (CMOS Inputs)	$V_{DD} = V_{DD}$ (max), (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ V_{DD} - 0.2V, CS2 ≥ V_{DD} - 0.2V or (3) LB# and UB# ≥ V_{DD} - 0.2V CS1# ≤ 0.2V, CS2 ≥ V_{DD} - 0.2V, f = 0	Com.	25°C	3.2	6	µA
				40°C	3.4	8	
				70°C	5.0	11	
			Ind.	85°C	6.6	14	
			Auto. A3	125°C	18.0	35	

Notes:
1. Typical value indicates the value for the center of distribution at V_{DD}=V_{DD} (Typ.), and not 100% tested.
2. Maximum value at 25°C, 40°C are guaranteed by design, and not 100% tested.

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AC CHARACTERISTICS(6) (OVER OPERATING RANGE)

READ CYCLE AC CHARACTERISTICS

Parameter	Symbol	45ns		55ns		unit	notes
		Min	Max	Min	Max		
Read Cycle Time	tRC	45	-	55	-	ns	1,5
Address Access Time	tAA	-	45	-	55	ns	1
Output Hold Time	tOHA	10	-	10	-	ns	1
CS1#, CS2 Access Time	tACS1/ACS2	-	45	-	55	ns	1
UB#, LB# Access Time	tBA	-	45	-	55	ns	1
OE# Access Time	tDOE	-	20	-	25	ns	1
OE# to High-Z Output	tHZOE	-	15	-	20	ns	2
OE# to Low-Z Output	tLZOE	5	-	5	-	ns	2
CS1#, CS2 to High-Z Output	tHZCS	-	15	-	20	ns	2
CS1#, CS2 to Low-Z Output	tLZCS	10	-	10	-	ns	2
UB#, LB# to High-Z Output	tHZB	-	15	-	20	ns	2
UB#, LB# to Low-Z Output	tLZB	10	-	10	-	ns	2

WRITE CYCLE AC CHARACTERISTICS

Parameter	Symbol	45ns		55ns		unit	notes
		Min	Max	Min	Min		
Write Cycle Time	tWC	45	-	55	-	ns	1,3,5
CS1#, CS2 to Write End	tSCS1/SCS2	35	-	40	-	ns	1,3
Address Setup Time to Write End	tAW	35	-	40	-	ns	1,3
UB#,LB# to Write End	tPWB	35	-	40	-	ns	1,3
Address Hold from Write End	tHA	0	-	0	-	ns	1,3
Address Setup Time	tSA	0	-	0	-	ns	1,3
WE# Pulse Width	tPWE	35	-	40	-	ns	1,3,4
Data Setup to Write End	tSD	20	-	25	-	ns	1,3
Data Hold from Write End	tHD	0	-	0	-	ns	1,3
WE# LOW to High-Z Output	tHZWE	-	15	-	20	ns	2,3
WE# HIGH to Low-Z Output	tLZWE	5	-	5	-	ns	2,3

Notes:

1. Tested with the load in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. tHZOE, tHZCS, tHZB, and tHZWE transitions are measured when the output enters a high impedance state. Not 100% tested.
3. The internal write time is defined by the overlap of CS1# = LOW, CS2=HIGH, UB# or LB# = LOW, and WE# = LOW. All four conditions must be in valid states to initiate a Write, but any condition can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. tPWE > tHZWE + tSD when OE# is LOW.
5. Address inputs must meet V_{IH} and V_{IL} SPEC during this period. Any glitch or unknown inputs are not permitted. Unknown input with standby mode is acceptable.
6. Data retention characteristics are defined later in DATA RETENTION CHARACTERISTICS.

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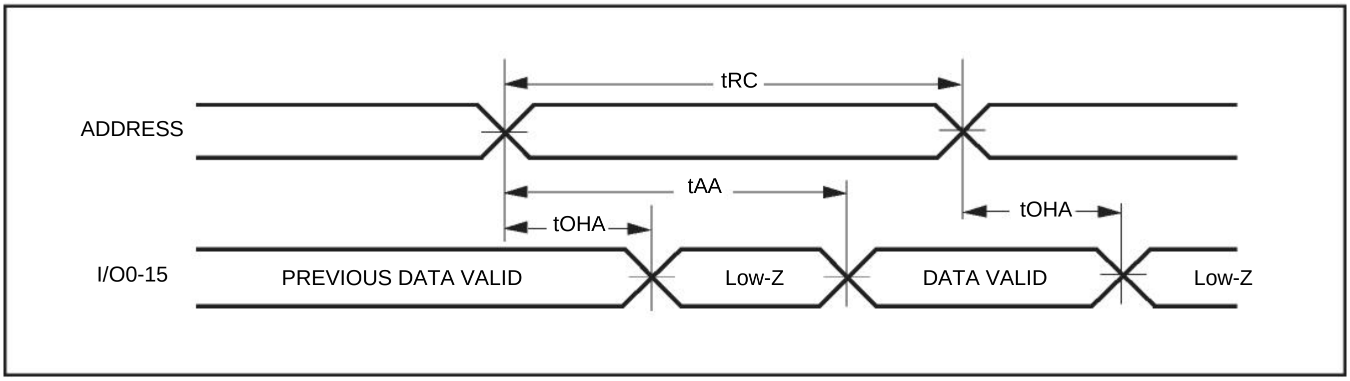
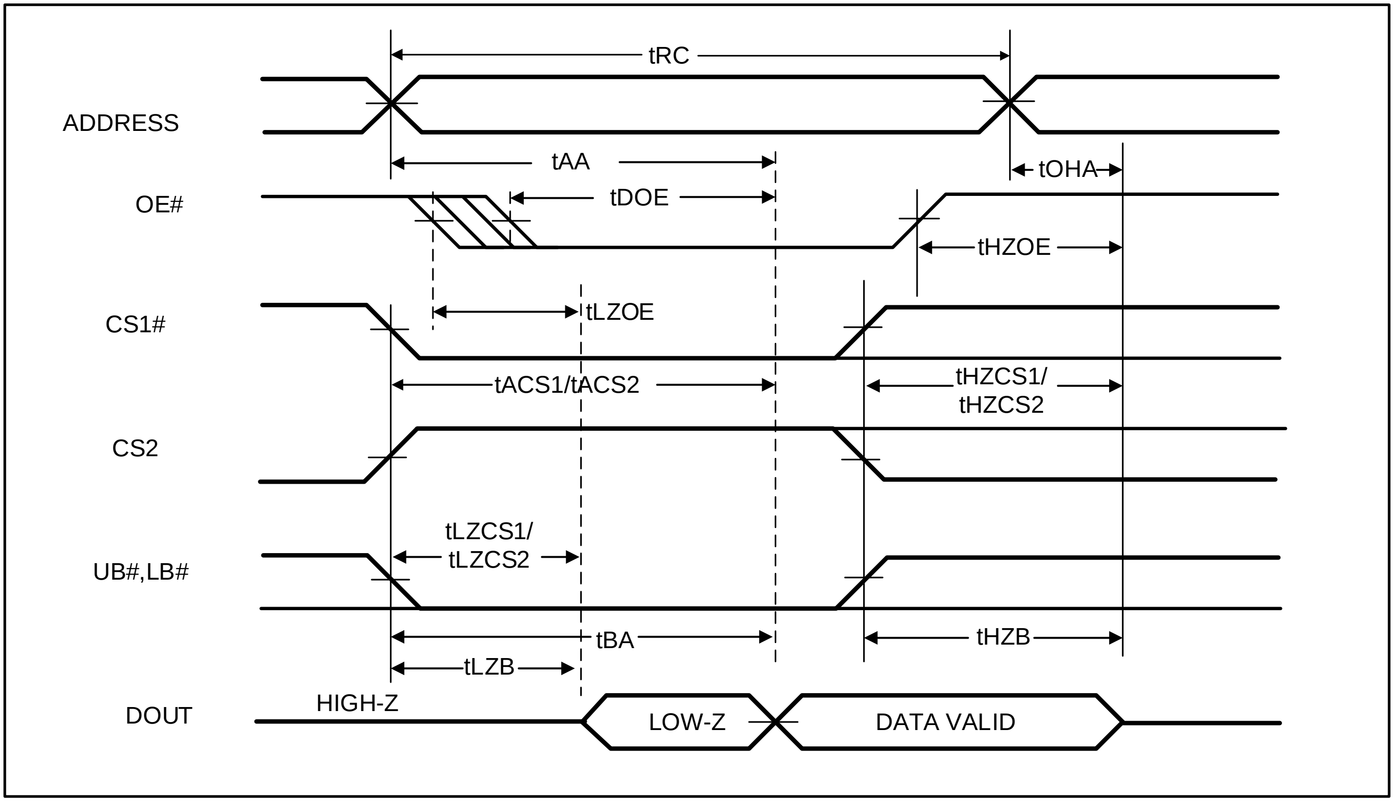
Timing Diagram

READ CYCLE NO. 1[1] (ADDRESS CONTROLLED, CS1# = OE# = UB# = LB# = LOW, CS2 = WE# = HIGH)



Note:
1. The device is continuously selected.

READ CYCLE NO.2[1] (OE# CONTROLLED, WE# = HIGH)



Notes:
1. Address is valid prior to or coincident with CS1# LOW or CS2 HIGH transition.

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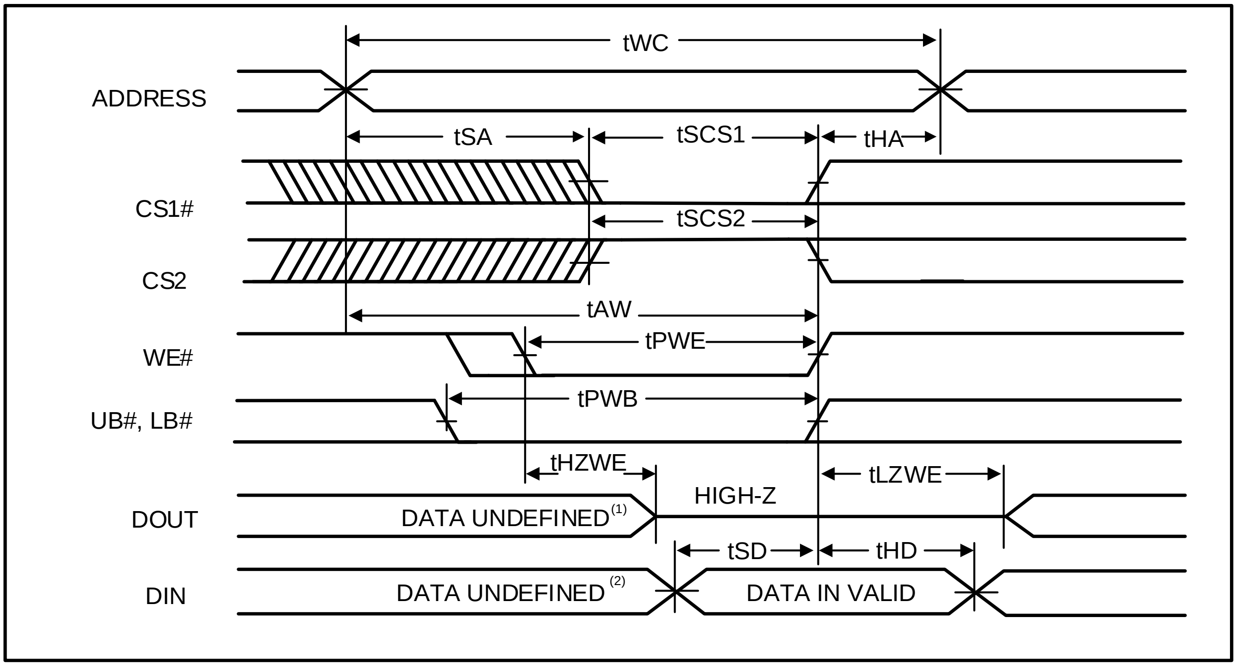
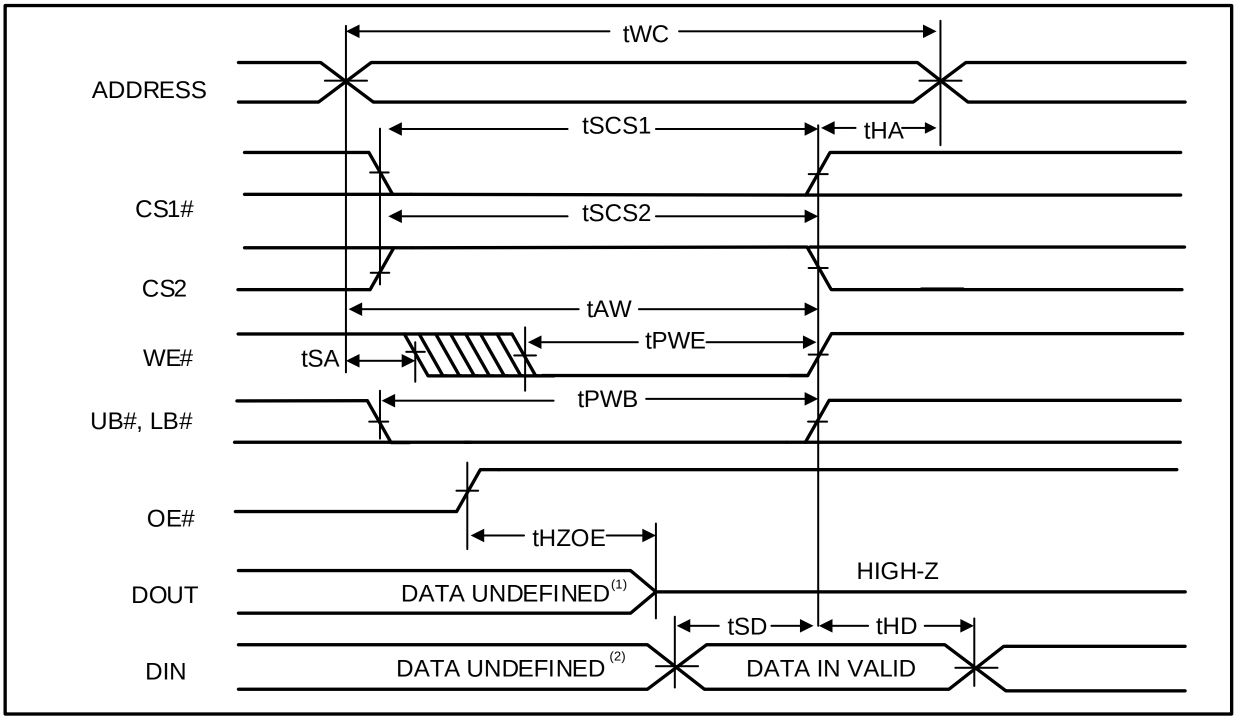
WRITE CYCLE NO.1 (1, 2) (CS1#, CS2 Controlled, OE# = HIGH or LOW)



Notes:

1. tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if OE# goes high before Write Cycle. tHZOE is the time DOUT goes to High-Z after OE# goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

WRITE CYCLE NO. 2(1,2) (WE# CONTROLLED: OE# IS HIGH DURING WRITE CYCLE)



Notes:
1. tHZOE is the time DOUT goes to High-Z after OE# goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

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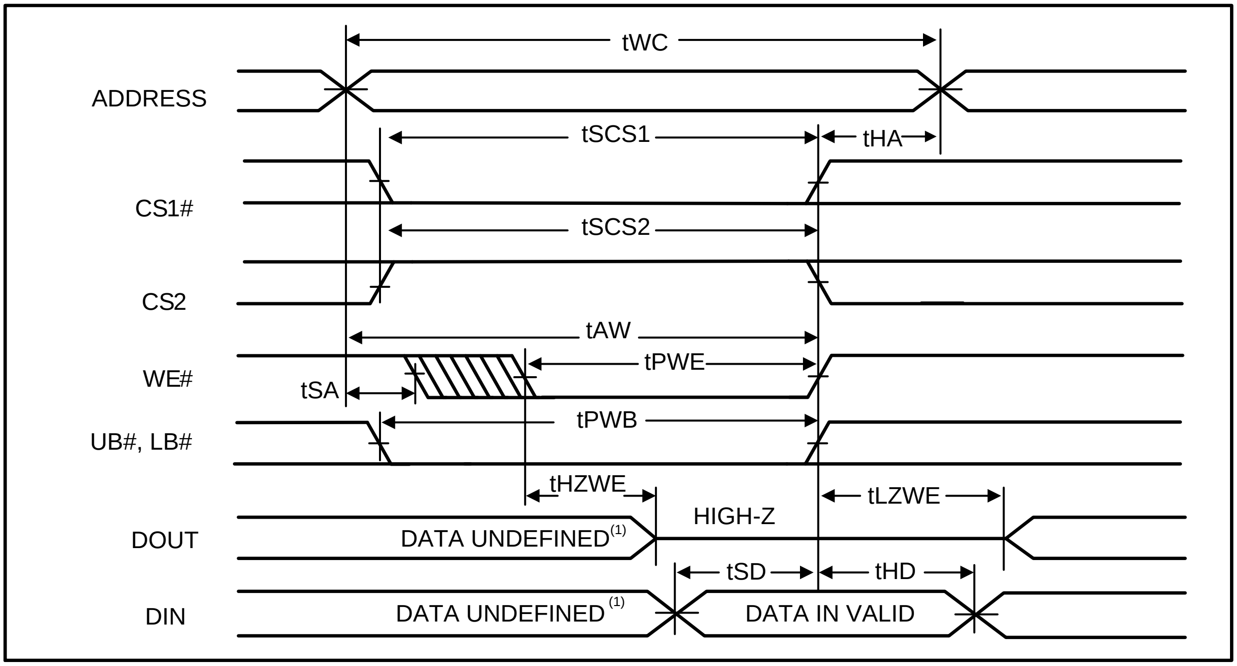
WRITE CYCLE NO. 3(1) (WE# CONTROLLED: OE# IS LOW DURING WRITE CYCLE)



Note:

1. If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.

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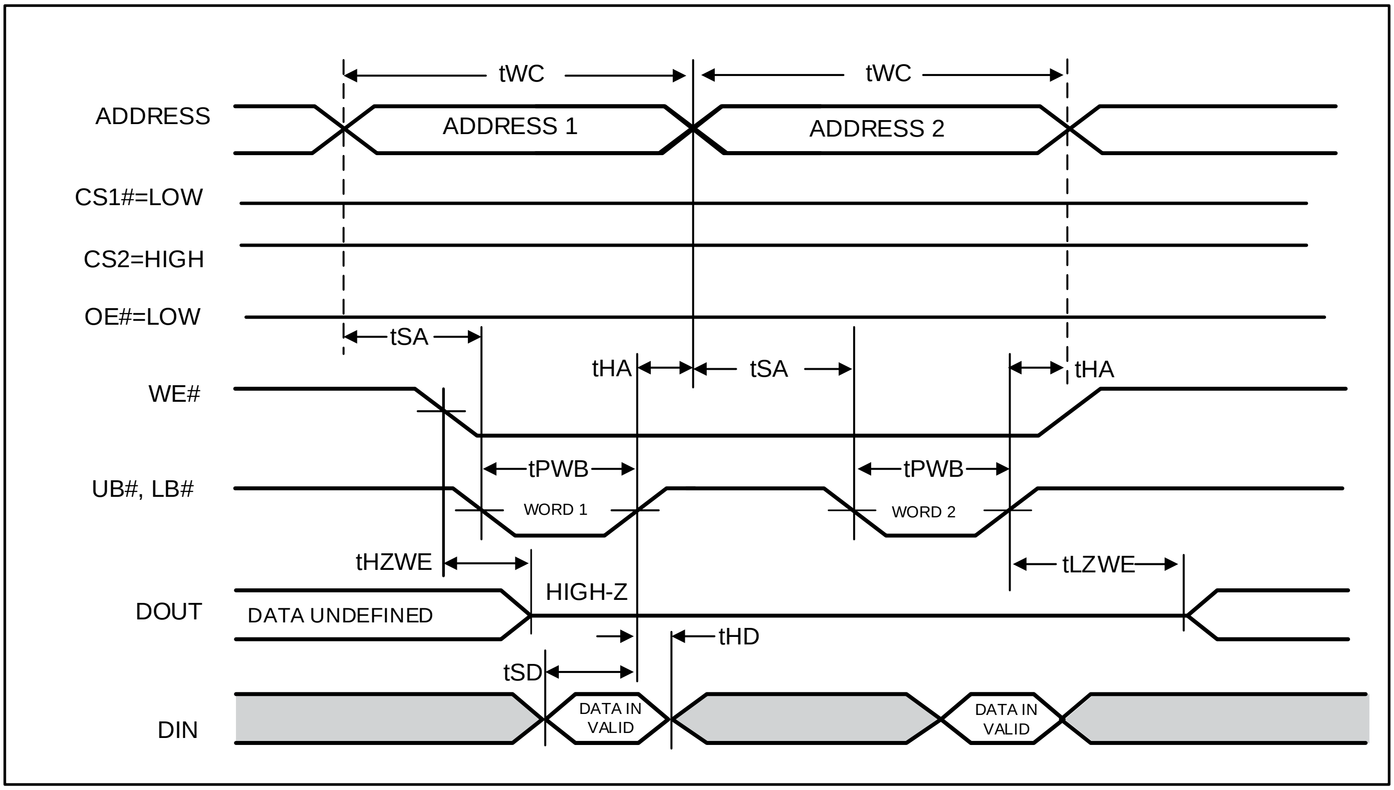
WRITE CYCLE NO. 4$^{(1, 2, 3)}$ (UB# & LB# Controlled, OE# = LOW)



Notes:
1. If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.
2. Due to the restriction of note1, OE# is recommended to be HIGH during write period.
3. WE# stays LOW in this example. If WE# toggles, tPWE and tHZWE must be considered.

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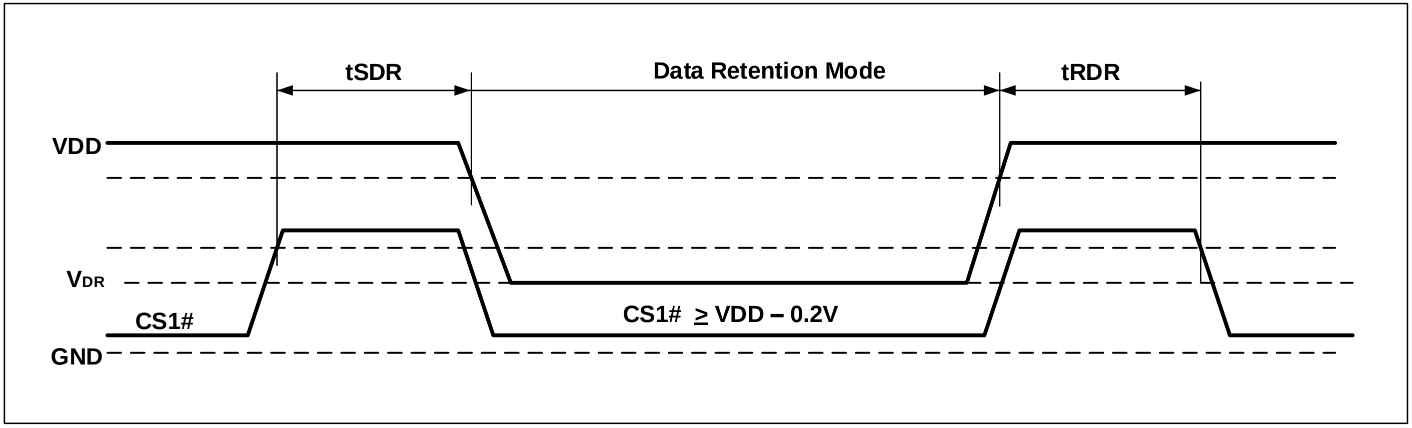
DATA RETENTION CHARACTERISTICS

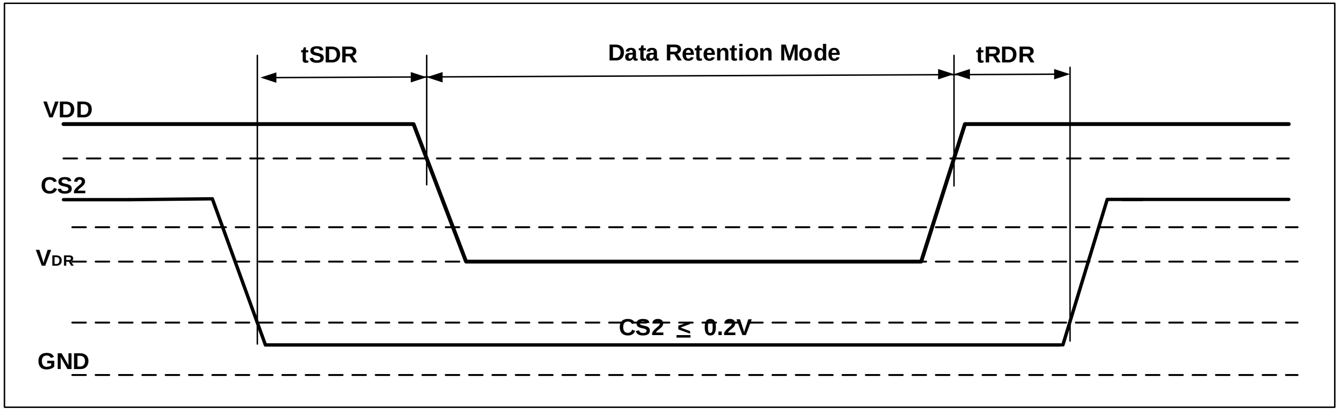
Symbol	Parameter	Test Condition		Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		1.5	-	-	V
I_{DR}	Data Retention Current	V_{DD} = MAX, CS1# ≥ V_{DD} – 0.2V or CS2 ≤ 0.2V or (LB# and UB#) ≥ V_{DD} - 0.2V, VIN ≤ 0.2V or VIN ≥ V_{DD} - 0.2V	25°C	-	3.2	5.5	uA
			85°C	-	-	13	
			125°C	-	-	33	
t_{SDR} (2)	Data Retention Setup Time	See Data Retention Waveform		0	-	-	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		tRC	-	-	ns

Notes:
1. Typical value indicates the value for the center of distribution at $V_{DD} = V_{DR}$ (min.), and not 100% tested.
2. VDD power down slope must be longer than 100 us/volt when enter into Data Retention Mode.

DATA RETENTION WAVEFORM (CS1# CONTROLLED)



DATA RETENTION WAVEFORM (CS2 CONTROLLED)



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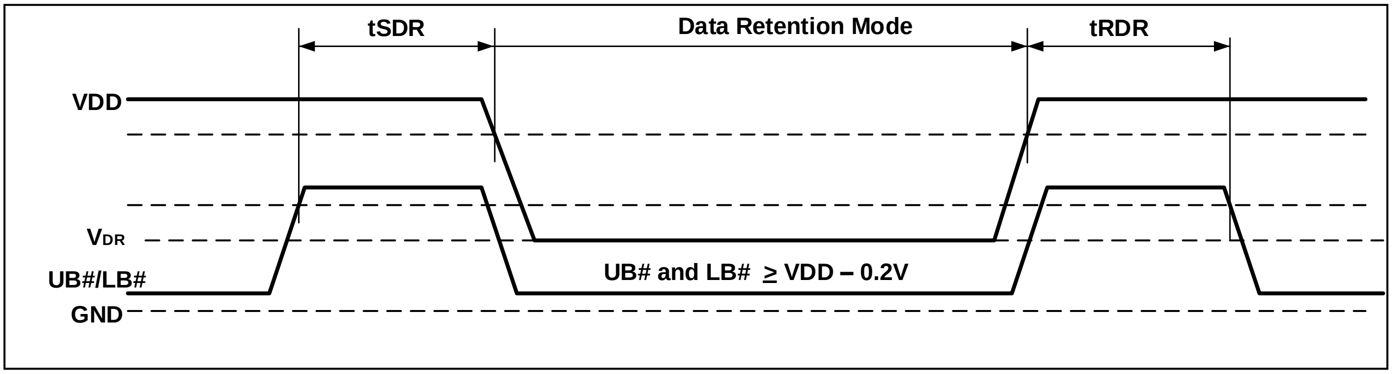
DATA RETENTION WAVEFORM (UB# AND LB# CONTROLLED)



Notes:

1. CS2 must satisfy either CS2 ≥ VDD -0.2V or CS2 ≤ 0.2V
2. CS1# must satisfy either CS1# ≥ VDD - 0.2V or CS1# ≤ 0.2V

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ORDERING INFORMATION

IS62/65WV51216HALL (1.65V - 2.2V)

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
55	IS62WV51216HALL-55TL	TSOP (Type II), Lead-free
55	IS62WV51216HALL-55B	mini BGA (6mm x 8mm), 1 CS Option
55	IS62WV51216HALL-55BL	mini BGA (6mm x 8mm), 1 CS Option, Lead-free
55	IS62WV51216HALL-55B2	mini BGA (6mm x 8mm), 2 CS Option
55	IS62WV51216HALL-55B2L	mini BGA (6mm x 8mm), 2 CS Option, Lead-free

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS62WV51216HALL-55TLI	TSOP (Type II), Lead-free
55	IS62WV51216HALL-55BI	mini BGA (6mm x 8mm), 1 CS Option
55	IS62WV51216HALL-55BLI	mini BGA (6mm x 8mm), 1 CS Option, Lead-free
55	IS62WV51216HALL-55B2I	mini BGA (6mm x 8mm), 2 CS Option
55	IS62WV51216HALL-55B2LI	mini BGA (6mm x 8mm), 2 CS Option, Lead-free

AUTOMOTIVE RANGE (A3): –40°C TO +125°C

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IS62/65WV51216HBLL (2.2V - 3.6V)

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
45	IS62WV51216HBLL-45TL	TSOP (Type II), Lead-free
45	IS62WV51216HBLL-45B	mini BGA (6mm x 8mm), 1 CS Option
45	IS62WV51216HBLL-45BL	mini BGA (6mm x 8mm), 1 CS Option, Lead-free
45	IS62WV51216HBLL-45B2	mini BGA (6mm x 8mm), 2 CS Option
45	IS62WV51216HBLL-45B2L	mini BGA (6mm x 8mm), 2 CS Option, Lead-free

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
45	IS62WV51216HBLL-45TLI	TSOP (Type II), Lead-free
45	IS62WV51216HBLL-45BI	mini BGA (6mm x 8mm), 1 CS Option
45	IS62WV51216HBLL-45BLI	mini BGA (6mm x 8mm), 1 CS Option, Lead-free
45	IS62WV51216HBLL-45B2I	mini BGA (6mm x 8mm), 2 CS Option
45	IS62WV51216HBLL-45B2LI	mini BGA (6mm x 8mm), 2 CS Option, Lead-free

Automotive Range (A3): –40°C to +125°C

Speed (ns)	Order Part No.	Package
55	IS65WV51216HBLL-55CTLA3	TSOP (Type II), Lead-free, Copper Lead-frame
55	IS65WV51216HBLL-55BA3	mini BGA (6mm x 8mm), 1 CS Option
55	IS65WV51216HBLL-55BLA3	mini BGA (6mm x 8mm), 1 CS Option, Lead-free
55	IS65WV51216HBLL-55B2A3	mini BGA (6mm x 8mm), 2 CS Option
55	IS65WV51216HBLL-55B2LA3	mini BGA (6mm x 8mm), 2 CS Option, Lead-free

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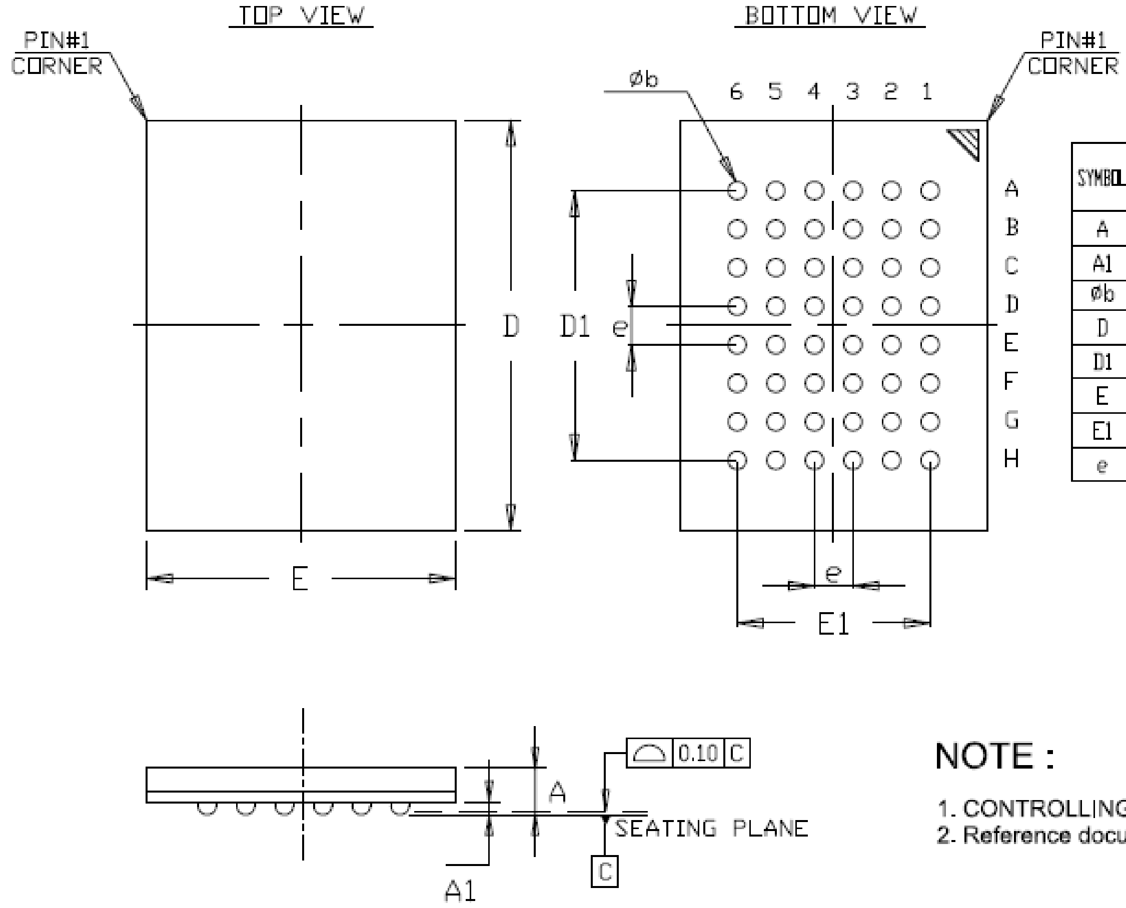
PACKAGE INFORMATION



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.00			0.039
A1	0.20	—	0.30	0.008	—	0.012
øb	0.30	0.35	0.40	0.012	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	5.25 BSC			0.207 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	3.75 BSC			0.148 BSC		
e	0.75 BSC.			0.030 BSC.		

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

TITLE	48L 6x8mm VF-BGA Package Outline	REV.	A	DATE	12/10/2013

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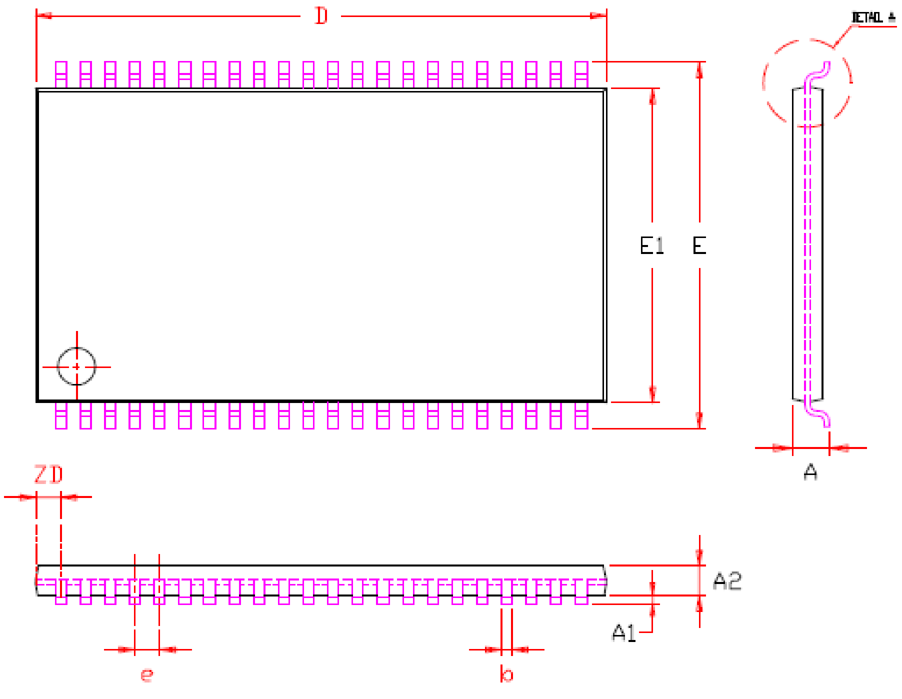
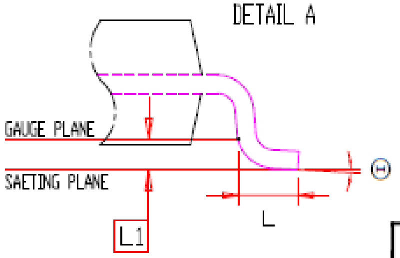


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00		1.20	0.039		0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.45	0.012		0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80 BSC.			0.031 BSC.		
L	0.40		0.69	0.016		0.027
L1	0.25 BSC.			0.010 BSC.		
ZD	0.805 REF.			0.032 REF.		
Θ	0		8°	0		8°



NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

ISSI	TITLE	44L 400mil TSOP-2 Package Outline	REV.	F	DATE	06/04/2008

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