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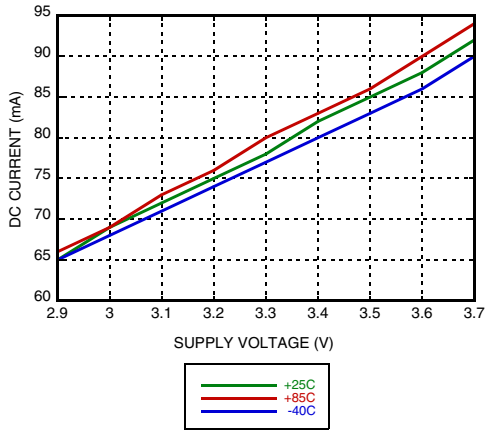
14 Gbps, FAST RISE TIME D-TYPE FLIP-FLOP w/ PROGRAMMABLE OUTPUT VOLTAGE & POSITIVE SUPPLY

Electrical Specifications (continued)

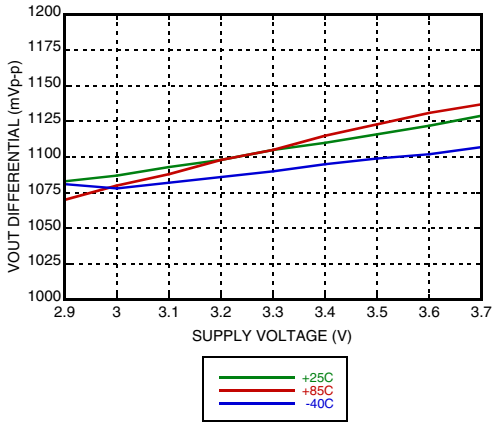
Parameter	Conditions	Min.	Typ.	Max	Units
Output Low Voltage			2.74		V
Output Rise / Fall Time	Differential, 20% - 80%		22 / 20		ps
Output Return Loss	Frequency <13 GHz		10		dB
Random Jitter Jr	rms			0.2	ps rms
Deterministic Jitter, Jd	peak-to-peak, 2^{15}-1 PRBS input [1]		2		ps, p-p
Propagation Delay Clock to Data, td			105		ps
Clock Phase Margin	13 GHz		320		deg
Set Up & Hold Time, t_{SH}			6		ps
VR Pin Current	VR = 3.3 V		2		mA
VR Pin Current	VR = 3.7 V			3.5	mA

[1] Deterministic jitter calculated by simultaneously measuring the jitter of a 300 mV, 13 GHz, 2^{15}-1 PRBS input, and a single-ended output

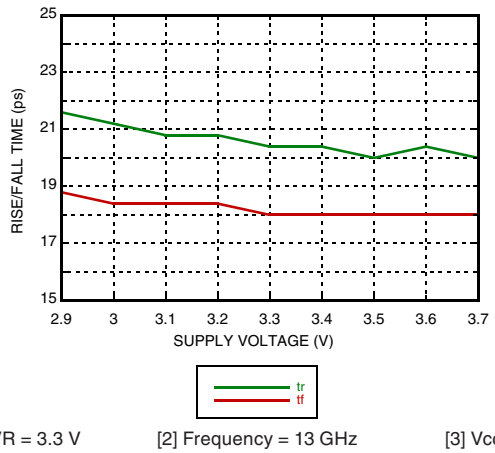
DC Current vs. Supply Voltage [1][2]



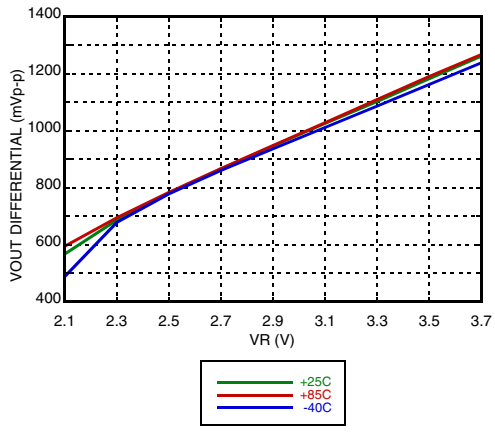
Output Differential Voltage vs. Supply Voltage [1][2]



Rise / Fall Time vs. Supply Voltage [1][2]



Output Differential Voltage vs. VR [1][2]



[1] VR = 3.3 V [2] Frequency = 13 GHz [3] Vcc = 3.3 V

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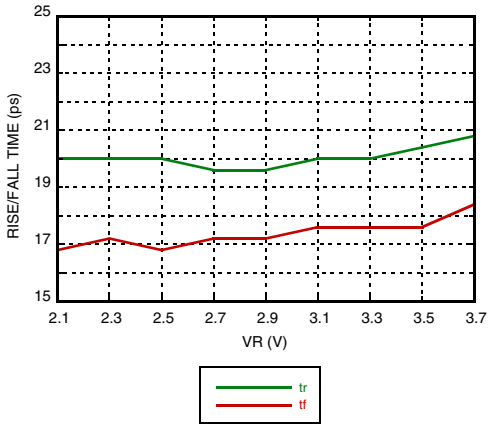
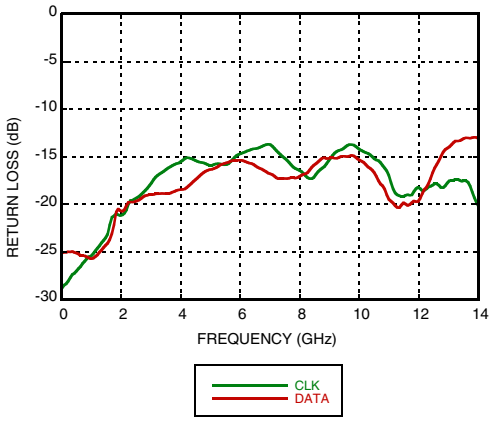
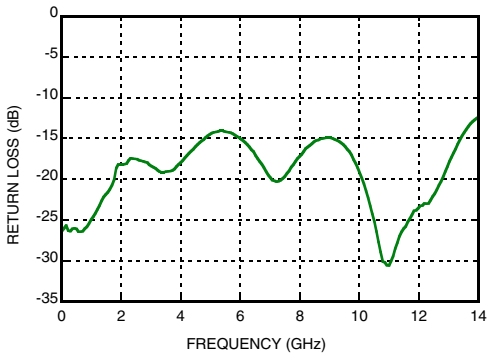
Rise / Fall Time vs. VR [1][2]



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



[1] Vcc = 3.3 V [2] Frequency = 13 GHz

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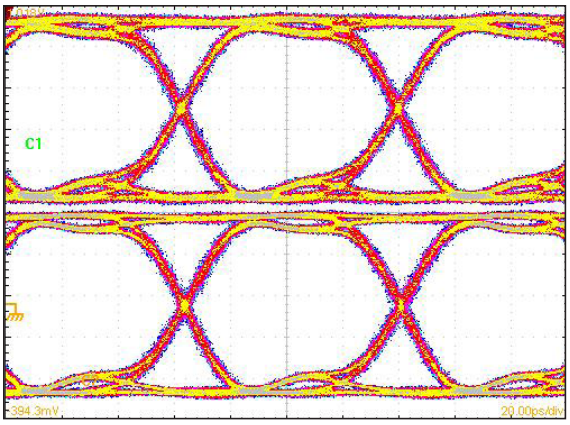
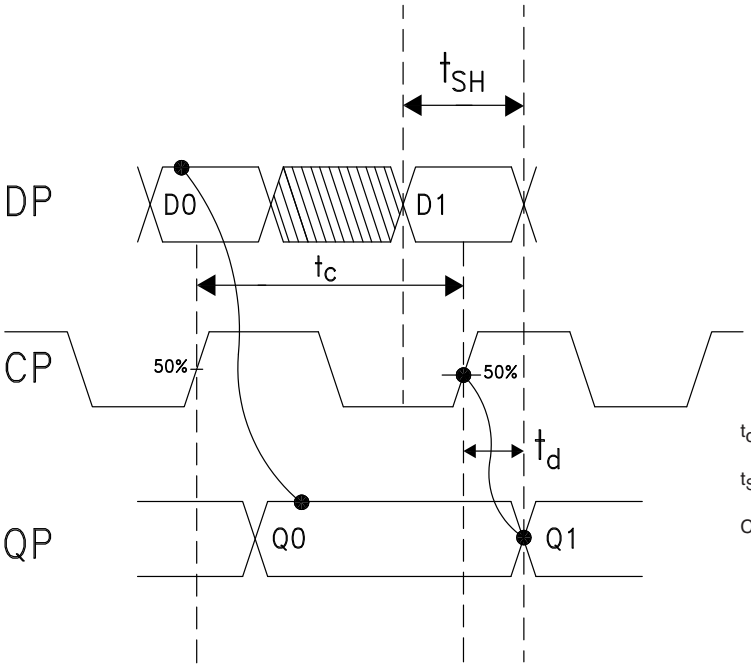
Eye Diagram



[1] Test Conditions:
Pattern generated with an Agilent N4903A Serial BERT.
Eye Diagram presented on a Tektronix CSA 8000.
Device input = 13 Gbps PN code.
Both output channels shown.
Device is AC coupled to scope.

Timing Diagram



$t_c = \frac{1}{f_{clock}}$

t_{SH} = Setup and Hold Time

CPM = Clock Phase Margin = $360° \frac{t_c - t_{SH}}{t_c}$

Truth Table

Input		Outputs
D	C	Q
L	L -> H	L
H	L -> H	H
Notes: D = DP - DN C = CP - CN Q = QP - QN	H - Positive voltage level L - Negative voltage level	

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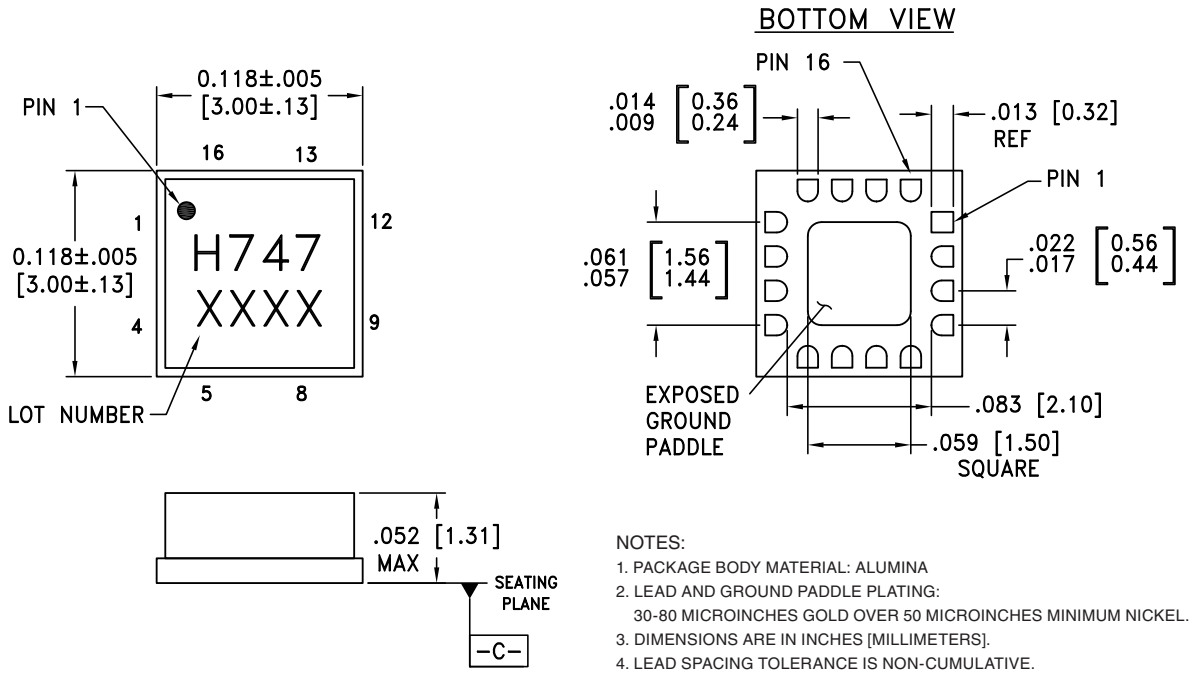
Absolute Maximum Ratings

Power Supply Voltage (Vcc)	Vcc -0.5 V to 3.75 V
Input Signals	Vcc - 2.0 V to Vcc + 0.5 V
Output Signals	Vcc - 1.5 V to Vcc + 0.5 V
Continuous Pdiss (T = 85 °C) (derate 17 mW/°C above 85 °C)	0.68 W
Thermal Resistance ($R_{th\ j\text{-}p}$) worst case junction to package paddle	59 °C/W
Maximum Junction Temperature	125 °C
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C
ESD Sensitivity (HBM)	Class 1C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO GND.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC747LC3C	Alumina, White	Gold over Nickel	MSL3 [1]	H747 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

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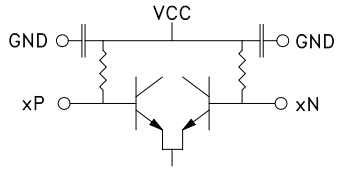
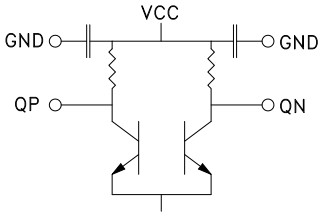
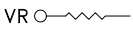
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9, 12	GND	Signal Grounds	
2, 3 6, 7	DN, DP CP, CN	Differential Data Inputs: Current Mode Logic (CML) referenced to positive supply.	
10, 11	QN, QP	Differential Data Outputs: Current Mode Logic (CML) referenced to positive supply.s	
13, 16	Vcc	Positive Supply	
14, Package Base	GND	Supply Ground	
15	VR	Output level control. Output level may be adjusted by applying a voltage to VR per “Output Differential vs. VR” plot.	

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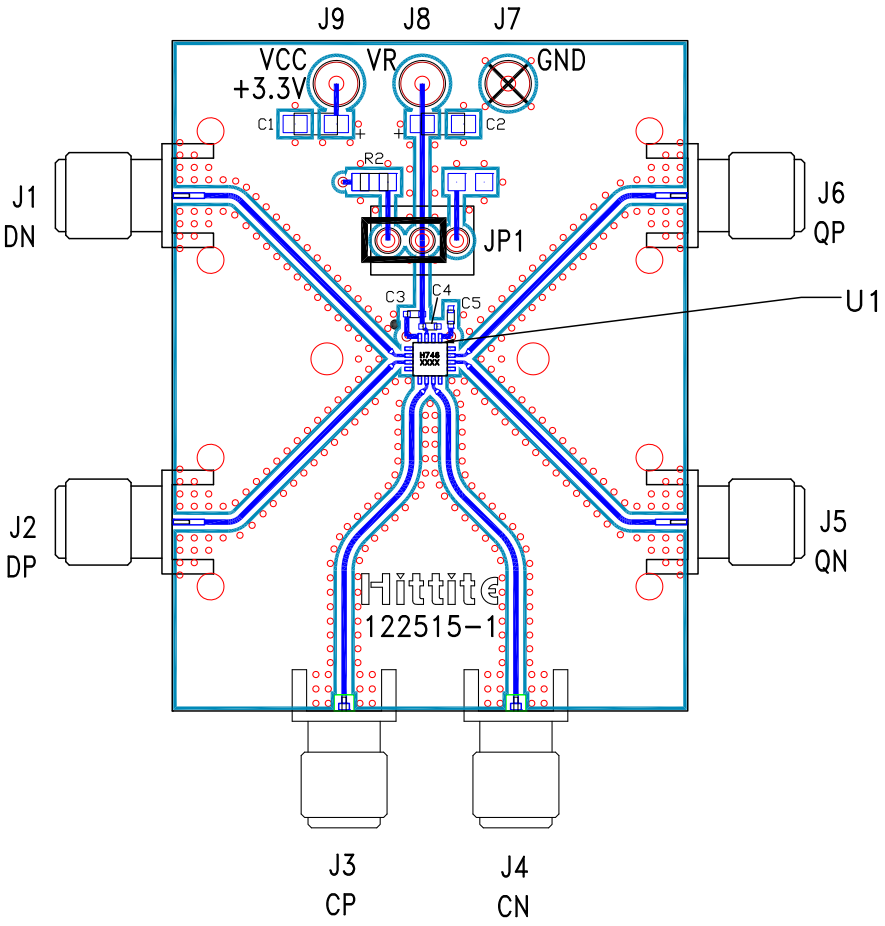
Evaluation PCB



List of Materials for Evaluation PCB EVAL01-HMC747LC3C [1]

Item	Description
J1 - J6	PCB Mount SMA RF Connectors
J7 - J9	DC Pin
JP1	Shorting Jumper
C1, C2	4.7 µF Capacitor, Tantalum
C3 - C5	100 pF Capacitor, 0402 Pkg.
R2	10 Ohm Resistor, 0603 Pkg.
U1	HMC747LC3C High Speed Logic, D-Type Flip-Flop
PCB [2]	122515 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package gro-und leads should be connected directly to the ground plane similar to that shown. The exposed package base should be connected to GND. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to Vcc for normal operation.

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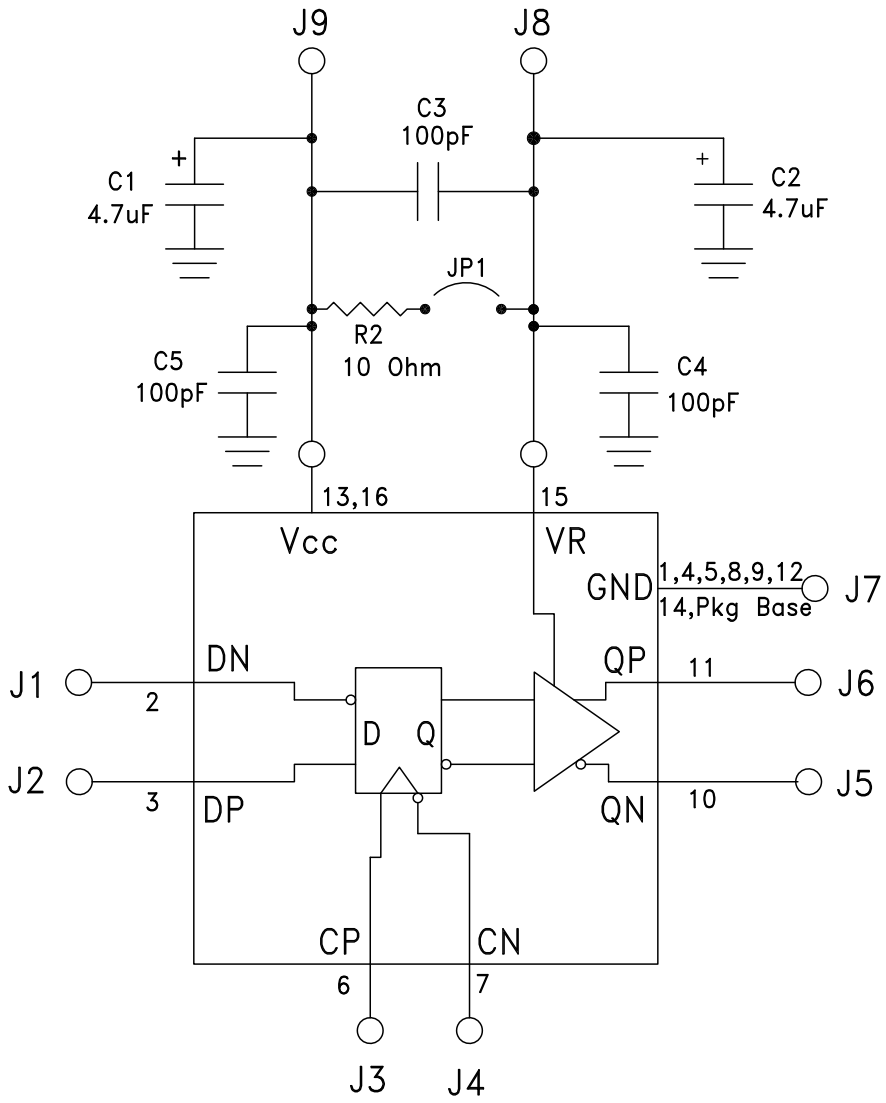
Application Circuit



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