# 1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32GG980 devices.

*Table 1.1. Ordering Information*

| Ordering Code | Flash (kB) | RAM (kB) | Max Speed (MHz) | Supply Voltage (V) | Temperature (ºC) | Package |
|---|---|---|---|---|---|---|
| EFM32GG980F512G-E-QFP100 | 512 | 128 | 48 | 1.98 - 3.8 | -40 - 85 | LQFP100 |
| EFM32GG980F1024G-E-QFP100 | 1024 | 128 | 48 | 1.98 - 3.8 | -40 - 85 | LQFP100 |

Adding the suffix 'R' to the part number (e.g. EFM32GG980F512G-E-QFP100R) denotes tape and reel.

Visit **www.silabs.com** for information on global distributors and representatives.

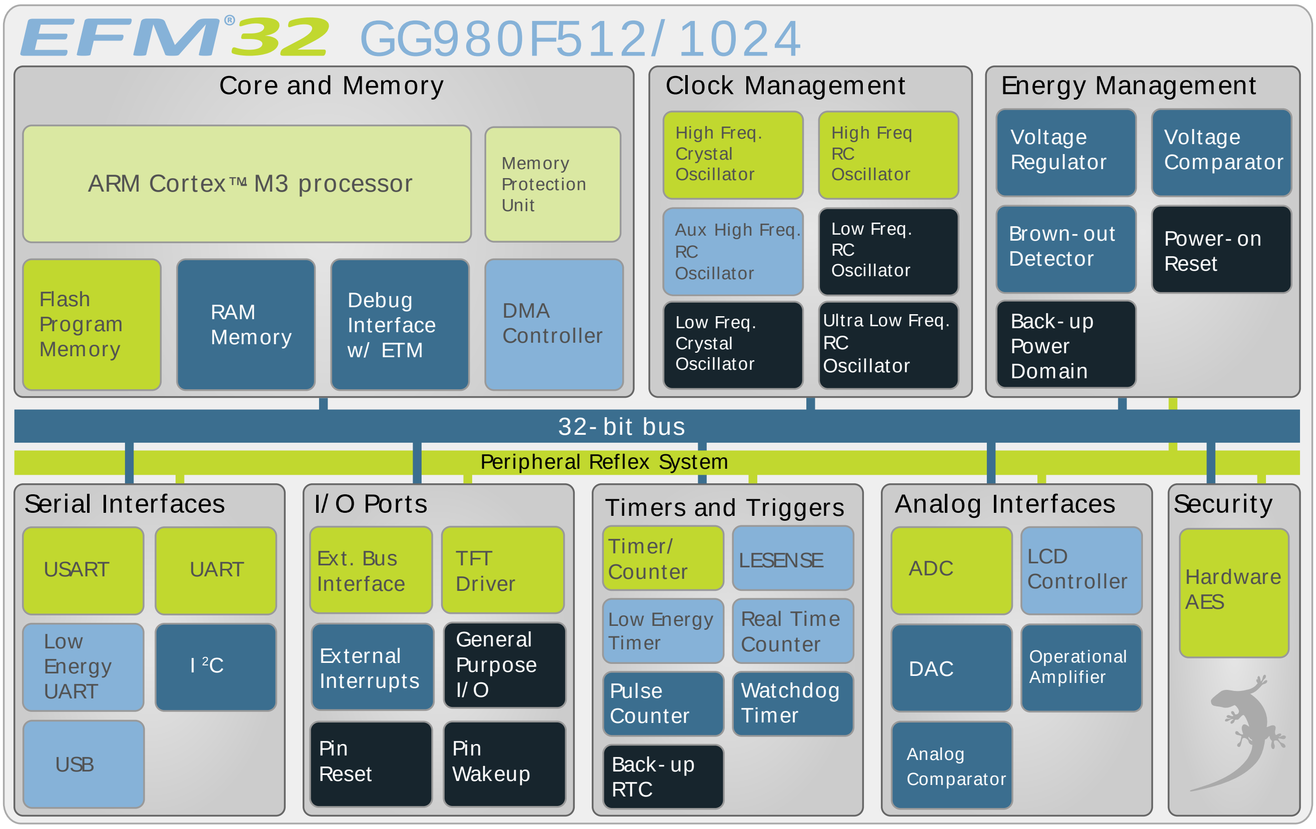
# 2 System Summary

## 2.1 System Introduction

The EFM32 MCUs are the world’s most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32GG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32GG980 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32GG Reference Manual*.

A block diagram of the EFM32GG980 is shown in Figure 2.1 (p. 3) .

***Figure 2.1. Block Diagram***


EFM32 GG980F512/1024
Core and Memory
ARM Cortex™ M3 processor
Memory Protection Unit
Flash Program Memory
RAM Memory
Debug Interface w/ ETM
DMA Controller
Clock Management
High Freq. Crystal Oscillator
High Freq RC Oscillator
Aux High Freq. RC Oscillator
Low Freq. RC Oscillator
Low Freq. Crystal Oscillator
Ultra Low Freq. RC Oscillator
Energy Management
Voltage Regulator
Voltage Comparator
Brown-out Detector
Power-on Reset
Back-up Power Domain
32-bit bus
Peripheral Reflex System
Serial Interfaces
USART
UART
Low Energy UART
I²C
USB
I/O Ports
Ext. Bus Interface
TFT Driver
External Interrupts
General Purpose I/O
Pin Reset
Pin Wakeup
Timers and Triggers
Timer/Counter
LESENSE
Low Energy Timer
Real Time Counter
Pulse Counter
Watchdog Timer
Back-up RTC
Analog Interfaces
ADC
LCD Controller
DAC
Operational Amplifier
Analog Comparator
Security
Hardware AES

### 2.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a  Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in *EFM32 Cortex-M3 Reference Manual*.

### 2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface  and an Embedded Trace Module (ETM) for data/instruction tracing .  In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

### 2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32GG microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

### 2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

### 2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32GG.

### 2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32GG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

### 2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32GG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

### 2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

### 2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

### 2.1.10 External Bus Interface (EBI)

The External Bus Interface provides access to external parallel interface devices such as SRAM, FLASH, ADCs and LCDs. The interface is memory mapped into the address bus of the Cortex-M3. This enables seamless access from software without manually manipulating the IO settings each time a read or write is performed. The data and address lines are multiplexed in order to reduce the number of pins required to interface the external devices. The timing is adjustable to meet specifications of the external devices. The interface is limited to asynchronous devices.

### 2.1.11 TFT Direct Drive

The EBI contains a TFT controller which can drive a TFT via a 565 RGB interface. The TFT controller supports programmable display and port sizes and offers accurate control of frequency and setup and hold timing. Direct Drive is supported for TFT displays which do not have their own frame buffer. In that case TFT Direct Drive can transfer data from either on-chip memory or from an external memory device to the TFT at low CPU load. Automatic alpha-blending and masking is also supported for transfers through the EBI interface.

### 2.1.12 Universal Serial Bus Controller (USB)

The USB is a full-speed USB 2.0 compliant OTG host/device controller. The USB can be used in Device, On-the-go (OTG) Dual Role Device or Host-only configuration. In OTG mode the USB supports both Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The device supports both full-speed (12MBit/s) and low speed (1.5MBit/s) operation. The USB device includes an internal dedicated Descriptor-Based Scatter/Gather DMA and supports up to 6 OUT endpoints and 6 IN endpoints, in addition to endpoint 0. The on-chip PHY includes all OTG features, except for the voltage booster for supplying 5V to VBUS when operating as host.

### 2.1.13 Inter-Integrated Circuit Interface (I2C)

The $I^2C$ module provides an interface between the MCU and a serial $I^2C$-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the $I^2C$ module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

### 2.1.14 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

### 2.1.15 Pre-Programmed USB/UART Bootloader

The bootloader presented in application note AN0042 is pre-programmed in the device at factory. The bootloader enables users to program the EFM32 through a UART or a USB CDC class virtual UART without the need for a debugger. The autobaud feature, interface and commands are described further in the application note.

### 2.1.16 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous serial Receiver and Transmitter (UART) is a very flexible serial I/O module. It supports full- and half-duplex asynchronous UART communication.

### 2.1.17 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART$^{TM}$, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

### 2.1.18 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

### 2.1.19 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

### 2.1.20 Backup Real Time Counter (BURTC)

The Backup Real Time Counter (BURTC) contains a 32-bit counter and is clocked either by a 32.768 kHz crystal oscillator, a 32.768 kHz RC oscillator or a 1 kHz ULFRCO. The BURTC is available in all Energy Modes and it can also run in backup mode, making it operational even if the main power should drain out.

### 2.1.21 Low Energy Timer (LETIMER)

The unique LETIMER$^{TM}$, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

### 2.1.22 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

### 2.1.23 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 2.1.24 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 2.1.25 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

### 2.1.26 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

### 2.1.27 Operational Amplifier (OPAMP)

The EFM32GG980 features 3 Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors etc.

### 2.1.28 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface (LESENSE$^{TM}$), is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable FSM which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

### 2.1.29 Backup Power Domain

The backup power domain is a separate power domain containing a Backup Real Time Counter, BURTC, and a set of retention registers, available in all energy modes. This power domain can be configured to automatically change power source to a backup battery when the main power drains out. The backup power domain enables the EFM32GG980 to keep track of time and retain data, even if the main power source should drain out.

### 2.1.30 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

### 2.1.31 General Purpose Input/Output (GPIO)

In the EFM32GG980, there are 81 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

### 2.1.32 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x34 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

## 2.2 Configuration Summary

The features of the EFM32GG980 is a subset of the feature set described in the EFM32GG Reference Manual. Table 2.1 (p. 8) describes device specific implementation of the features.

### Table 2.1. Configuration Summary

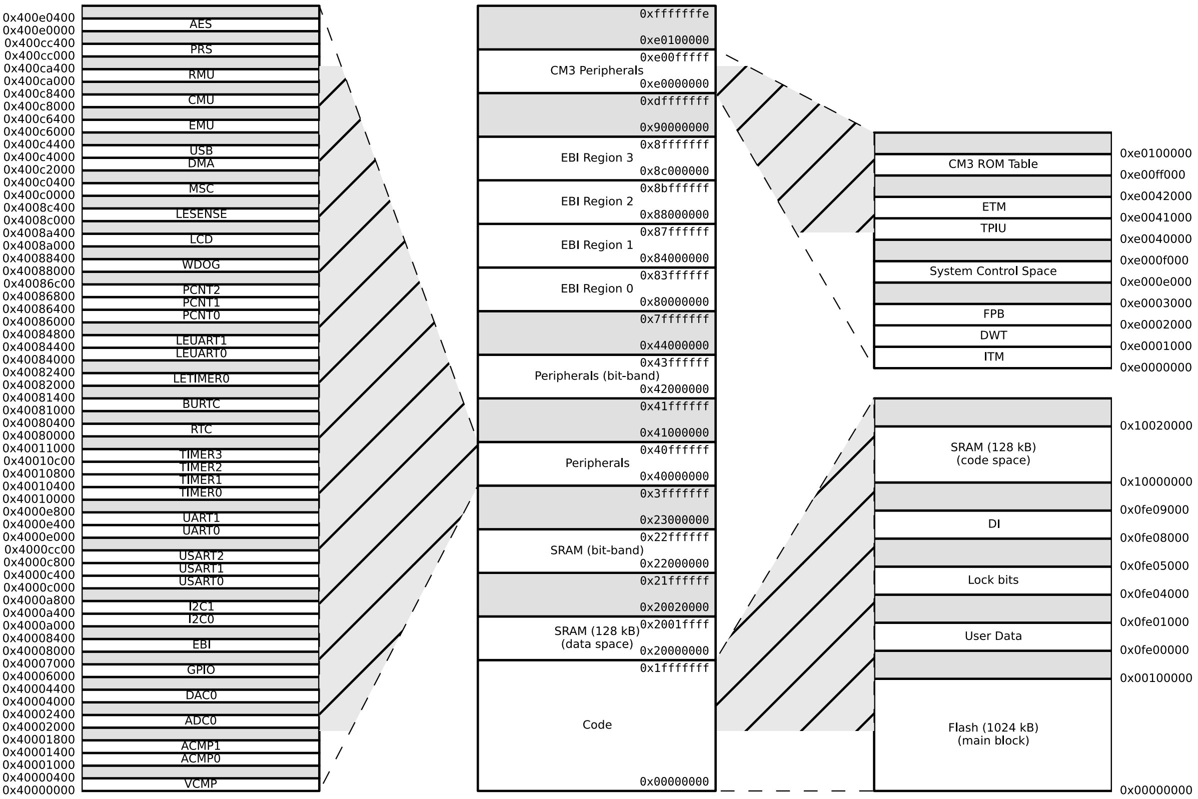
| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID |
| EBI | Full configuration | EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |

| Module | Configuration | Pin Connections |
|---|---|---|
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 81 pins | Available pins are shown in Table 4.3 (p. 66) |
| LCD | Full configuration | LCD_SEG[33:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

## 2.3 Memory Map

The *EFM32GG980* memory map is shown in Figure 2.2 (p. 9), with RAM and Flash sizes for the largest memory configuration.

### Figure 2.2. EFM32GG980 Memory Map with largest RAM and Flash sizes


0x400e0400
0x400e0000
AES
0x400cc400
0x400cc000
PRS
0x400ca400
0x400ca000
RMU
0x400c8400
0x400c8000
CMU
0x400c6400
0x400c6000
EMU
0x400c4400
0x400c4000
USB
0x400c2000
DMA
0x400c0400
0x400c0000
MSC
0x4008c400
0x4008c000
LESENSE
0x4008a400
0x4008a000
LCD
0x40088400
0x40088000
WDOG
0x40086c00
0x40086800
PCNT2
0x40086400
PCNT1
0x40086000
PCNT0
0x40084800
0x40084400
LEUART1
0x40084000
LEUART0
0x40082400
0x40082000
LETIMER0
0x40081400
0x40081000
BURTC
0x40080400
0x40080000
RTC
0x40011000
0x40010c00
TIMER3
0x40010800
TIMER2
0x40010400
TIMER1
0x40010000
TIMER0
0x4000e800
0x4000e400
UART1
0x4000e000
UART0
0x4000cc00
0x4000c800
USART2
0x4000c400
USART1
0x4000c000
USART0
0x4000a800
0x4000a400
I2C1
0x4000a000
I2C0
0x40008400
0x40008000
EBI
0x40007000
0x40006000
GPIO
0x40004400
0x40004000
DAC0
0x40002400
0x40002000
ADC0
0x40001800
0x40001400
ACMP1
0x40001000
ACMP0
0x40000400
0x40000000
VCMP
0xfffffffe
0xe0100000
0xe00fffff
CM3 Peripherals
0xe0000000
0xdfffffff
0x90000000
0x8fffffff
EBI Region 3
0x8c000000
0x8bffffff
EBI Region 2
0x88000000
0x87ffffff
EBI Region 1
0x84000000
0x83ffffff
EBI Region 0
0x80000000
0x7fffffff
0x44000000
0x43ffffff
Peripherals (bit-band)
0x42000000
0x41ffffff
0x41000000
0x40ffffff
Peripherals
0x40000000
0x3fffffff
0x23000000
0x22ffffff
SRAM (bit-band)
0x22000000
0x21ffffff
0x20020000
0x2001ffff
SRAM (128 kB)
(data space)
0x20000000
0x1fffffff
Code
0x00000000
CM3 ROM Table
0xe0100000
0xe00ff000
ETM
0xe0042000
TPIU
0xe0041000
0xe0040000
System Control Space
0xe000f000
0xe000e000
FPB
0xe0003000
DWT
0xe0002000
ITM
0xe0001000
0xe0000000
SRAM (128 kB)
(code space)
0x10020000
0x10000000
DI
0x0fe09000
0x0fe08000
Lock bits
0x0fe05000
0x0fe04000
User Data
0x0fe01000
0x0fe00000
Flash (1024 kB)
(main block)
0x00100000
0x00000000

# 3 Electrical Characteristics

## 3.1 Test Conditions

### 3.1.1 Typical Values

The typical data are based on $T_{AMB}$=25°C and $V_{DD}$=3.0 V, as defined in Table 3.2 (p. 10) , unless otherwise specified.

### 3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 10) , unless otherwise specified.

## 3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 10) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 10) .

***Table 3.1. Absolute Maximum Ratings***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature range | | -40 | | 150 | °C |
| $T_S$ | Maximum soldering temperature | Latest IPC/JEDEC J-STD-020 Standard | | | 260 | °C |
| $V_{DDMAX}$ | External main supply voltage | | 0 | | 3.8 | V |
| $V_{IOPIN}$ | Voltage on any I/O pin | | -0.3 | | $V_{DD}$+0.3 | V |
| $I_{IOMAX}$ | Current per I/O pin (sink) | | | | 100 | mA |
| | Current per I/O pin (source) | | | | -100 | mA |

## 3.3 General Operating Conditions

### 3.3.1 General Operating Conditions

***Table 3.2. General Operating Conditions***

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{AMB}$ | Ambient temperature range | -40 | | 85 | °C |
| $V_{DDOP}$ | Operating supply voltage | 1.98 | | 3.8 | V |
| $f_{APB}$ | Internal APB clock frequency | | | 48 | MHz |
| $f_{AHB}$ | Internal AHB clock frequency | | | 48 | MHz |

## 3.4 Current Consumption

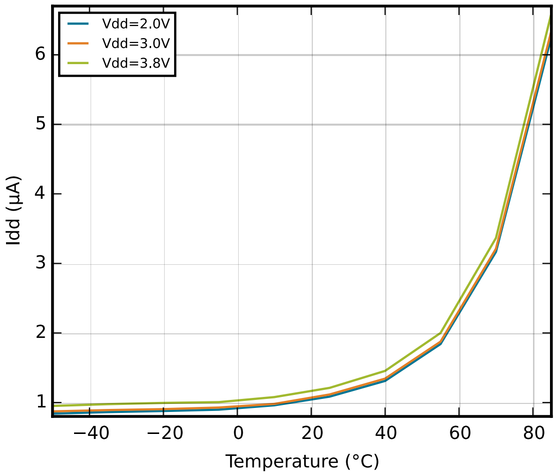
*Table 3.3. Current Consumption*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{EM0}$ | EM0 current. No prescaling. Running prime number calculation code from flash. (Production test condition = 14MHz) | 48 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 219 | 240 | µA/ MHz |
| | | 28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 205 | 225 | µA/ MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 206 | 229 | µA/ MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 209 | 232 | µA/ MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 211 | 234 | µA/ MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 215 | 242 | µA/ MHz |
| | | 1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 243 | 327 | µA/ MHz |
| $I_{EM1}$ | EM1 current (Production test condition = 14MHz) | 48 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 80 | 90 | µA/ MHz |
| | | 28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 80 | 90 | µA/ MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 81 | 91 | µA/ MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 83 | 99 | µA/ MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 85 | 100 | µA/ MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 90 | 102 | µA/ MHz |
| | | 1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 122 | 152 | µA/ MHz |
| $I_{EM2}$ | EM2 current | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 1.1[1] | 1.9[1] | µA |
| | | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 8.8[1] | 21.5[1] | µA |
| $I_{EM3}$ | EM3 current | $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 0.8[1] | 1.5[1] | µA |
| | | $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 8.2[1] | 20.3[1] | µA |
| $I_{EM4}$ | EM4 current | $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 0.02 | 0.08 | µA |
| | | $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 0.5 | 2.5 | µA |

[1] Only one RAM block enabled. The RAM block size is 32 kB.

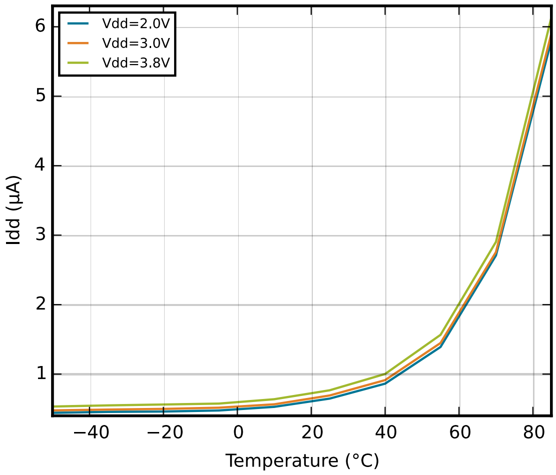
## 3.4.1 EM2 Current Consumption

*Figure 3.1. EM2 current consumption. RTC[1] prescaled to 1 Hz, 32.768 kHz LFRCO.*



## 3.4.2 EM3 Current Consumption

*Figure 3.2. EM3 current consumption.*



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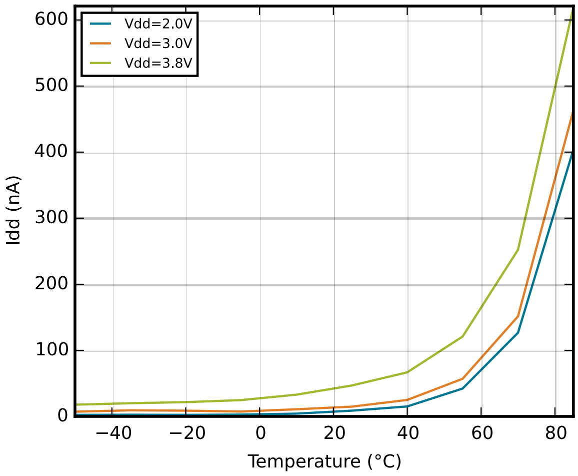
[1] Using backup RTC.

### 3.4.3 EM4 Current Consumption

*Figure 3.3. EM4 current consumption.*



## 3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

*Table 3.4. Energy Modes Transitions*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{EM10}$ | Transition time from EM1 to EM0 | | 0 | | HF-CORE-CLK cycles |
| $t_{EM20}$ | Transition time from EM2 to EM0 | | 2 | | µs |
| $t_{EM30}$ | Transition time from EM3 to EM0 | | 2 | | µs |
| $t_{EM40}$ | Transition time from EM4 to EM0 | | 163 | | µs |

## 3.6 Power Management

The EFM32GG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

### Table 3.5. Power Management

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{BODextthr-}$ | BOD threshold on falling external supply voltage | EM0 | 1.74 | | 1.96 | V |
| | | EM2 | 1.74 | | 1.98 | V |
| $V_{BODintthr-}$ | BOD threshold on falling internally regulated supply voltage | | 1.57 | | 1.70 | V |
| $V_{BODextthr+}$ | BOD threshold on rising external supply voltage | | | 1.85 | 1.98 | V |
| $V_{PORthr+}$ | Power-on Reset (POR) threshold on rising external supply voltage | | | | 1.98 | V |
| $t_{RESET}$ | Delay from reset is released until program execution starts | Applies to Power-on Reset, Brown-out Reset and pin reset. | | 163 | | µs |
| $C_{DECOUPLE}$ | Voltage regulator decoupling capacitor. | X5R capacitor recommended. Apply between DECOUPLE pin and GROUND | | 1 | | µF |
| $C_{USB\_VREGO}$ | USB voltage regulator out decoupling capacitor. | X5R capacitor recommended. Apply between USB_VREGO pin and GROUND | | 1 | | µF |
| $C_{USB\_VREGI}$ | USB voltage regulator in decoupling capacitor. | X5R capacitor recommended. Apply between USB_VREGI pin and GROUND | | 4.7 | | µF |

## 3.7 Flash

### *Table 3.6. Flash*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $EC_{FLASH}$ | Flash erase cycles before failure | | 20000 | | | cycles |
| $RET_{FLASH}$ | Flash data retention | $T_{AMB}$<150°C | 10000 | | | h |
| | | $T_{AMB}$<85°C | 10 | | | years |
| | | $T_{AMB}$<70°C | 20 | | | years |
| $t_{W\_PROG}$ | Word (32-bit) programming time | | 20 | | | µs |
| $t_{PERASE}$ | Page erase time | LPERASE == 0 | 20 | 20.4 | 20.8 | ms |
| | | LPERASE == 1 | 40 | 40.4 | 40.8 | ms |
| $t_{DERASE}$ | Device erase time | | | | 161.6 | ms |
| $I_{ERASE}$ | Erase current | LPERASE == 0 | | | 14[1] | mA |
| | | LPERASE == 1 | | | 7[1] | mA |
| $I_{WRITE}$ | Write current | LPWRITE == 0 | | | 14[1] | mA |
| | | LPWRITE == 1 | | | 7[1] | mA |
| $V_{FLASH}$ | Supply voltage during flash erase and write | | 1.98 | | 3.8 | V |

[1] Measured at 25°C

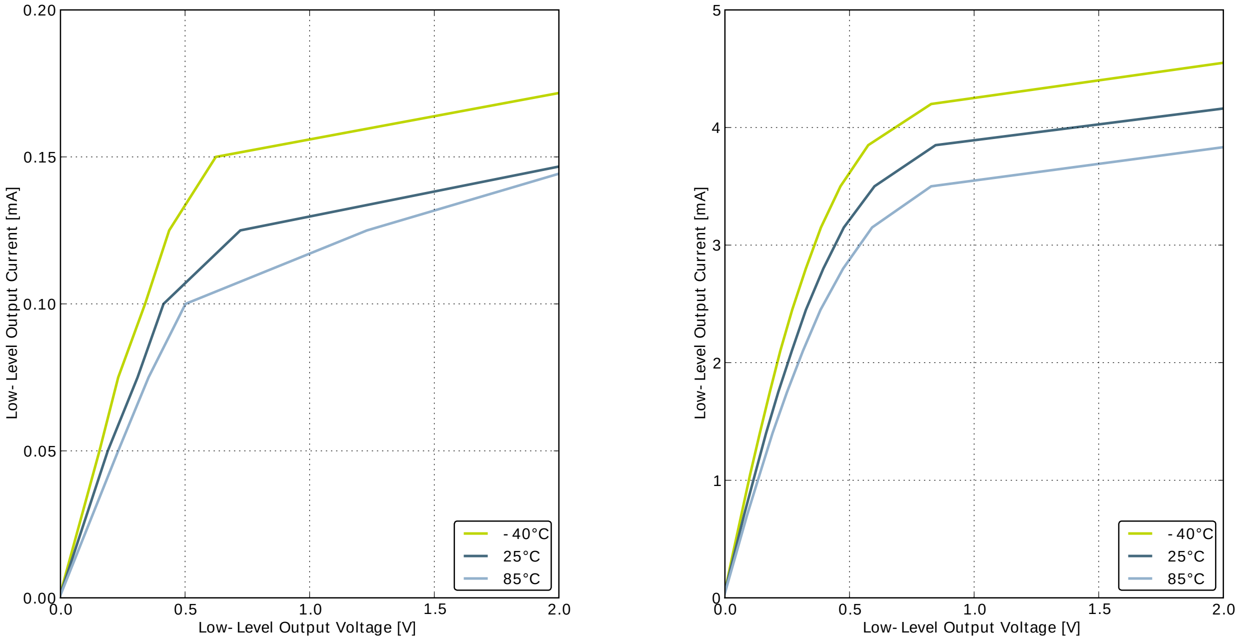
## 3.8 General Purpose Input Output

### *Table 3.7. GPIO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IOIL}$ | Input low voltage | | | | $0.30V_{DD}$ | V |
| $V_{IOIH}$ | Input high voltage | | $0.70V_{DD}$ | | | V |
| $V_{IOOH}$ | Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD) | Sourcing 0.1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | $0.80V_{DD}$ | | V |
| | | Sourcing 0.1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | $0.90V_{DD}$ | | V |
| | | Sourcing 1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW | | $0.85V_{DD}$ | | V |
| | | Sourcing 1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW | | $0.90V_{DD}$ | | V |
| | | Sourcing 6 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | $0.75V_{DD}$ | | | V |
| | | Sourcing 6 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | $0.85V_{DD}$ | | | V |

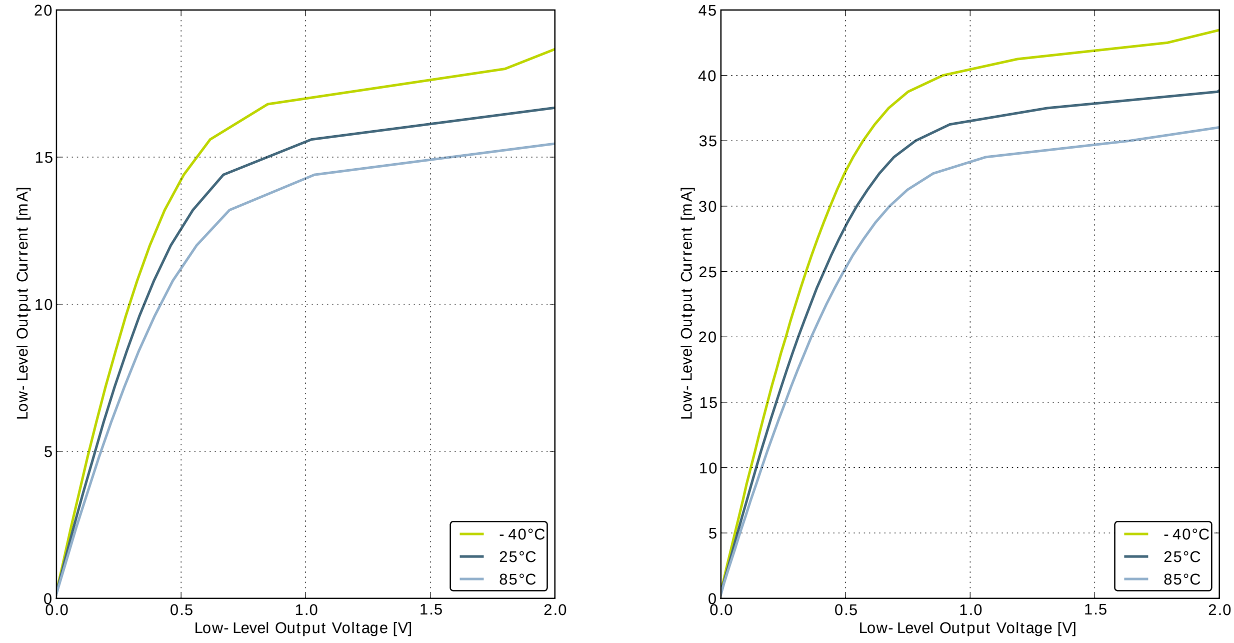
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | Sourcing 20 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH | 0.60$V_{DD}$ | | | V |
| | | Sourcing 20 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH | 0.80$V_{DD}$ | | | V |
| $V_{IOOL}$ | Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD) | Sinking 0.1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | 0.20$V_{DD}$ | | V |
| | | Sinking 0.1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | 0.10$V_{DD}$ | | V |
| | | Sinking 1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW | | 0.10$V_{DD}$ | | V |
| | | Sinking 1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW | | 0.05$V_{DD}$ | | V |
| | | Sinking 6 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | | | 0.30$V_{DD}$ | V |
| | | Sinking 6 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | | | 0.20$V_{DD}$ | V |
| | | Sinking 20 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH | | | 0.35$V_{DD}$ | V |
| | | Sinking 20 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH | | | 0.20$V_{DD}$ | V |
| $I_{IOLEAK}$ | Input leakage current | High Impedance IO connected to GROUND or $V_{DD}$ | | ±0.1 | ±40 | nA |
| $R_{PU}$ | I/O pin pull-up resistor | | | 40 | | kOhm |
| $R_{PD}$ | I/O pin pull-down resistor | | | 40 | | kOhm |
| $R_{IOESD}$ | Internal ESD series resistor | | | 200 | | Ohm |
| $t_{IOGLITCH}$ | Pulse width of pulses to be removed by the glitch suppression filter | | 10 | | 50 | ns |
| $t_{IOOF}$ | Output fall time | GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance $C_L$=12.5-25pF. | 20+0.1$C_L$ | | 250 | ns |
| | | GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance $C_L$=350-600pF | 20+0.1$C_L$ | | 250 | ns |
| $V_{IOHYST}$ | I/O pin hysteresis ($V_{IOTHR+}$ - $V_{IOTHR-}$) | $V_{DD}$ = 1.98 - 3.8 V | 0.10$V_{DD}$ | | | V |

*Figure 3.4. Typical Low-Level Output Current, 2V Supply Voltage*



GPIO_Px_CTRL DRIVEMODE = LOWEST

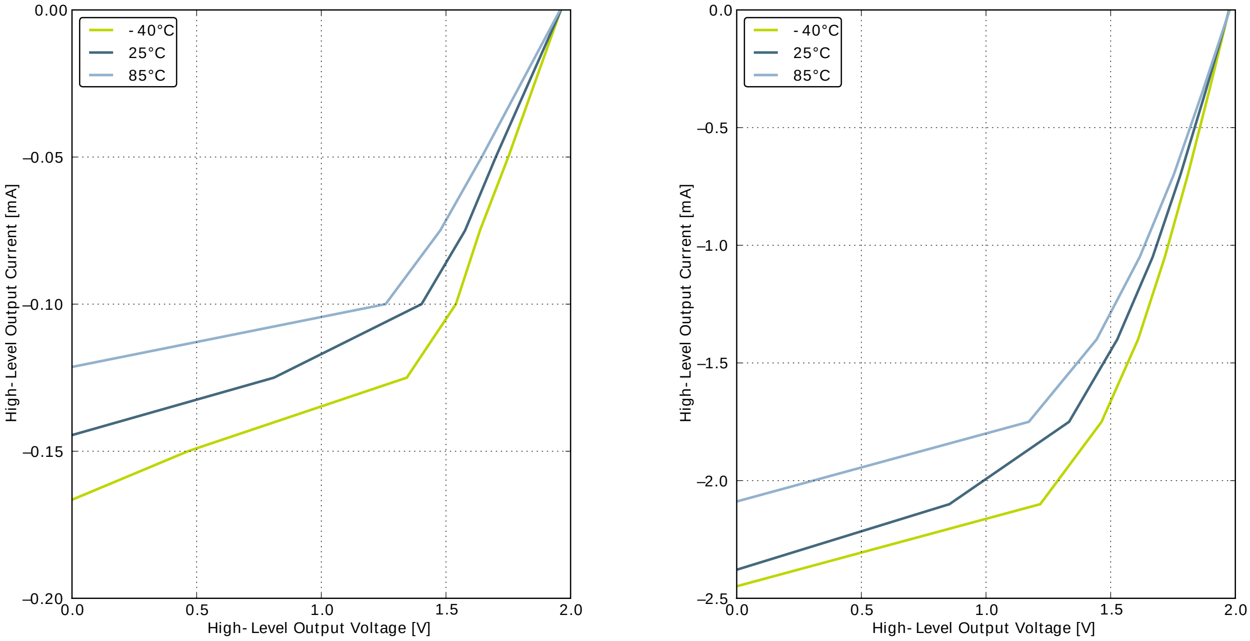
GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

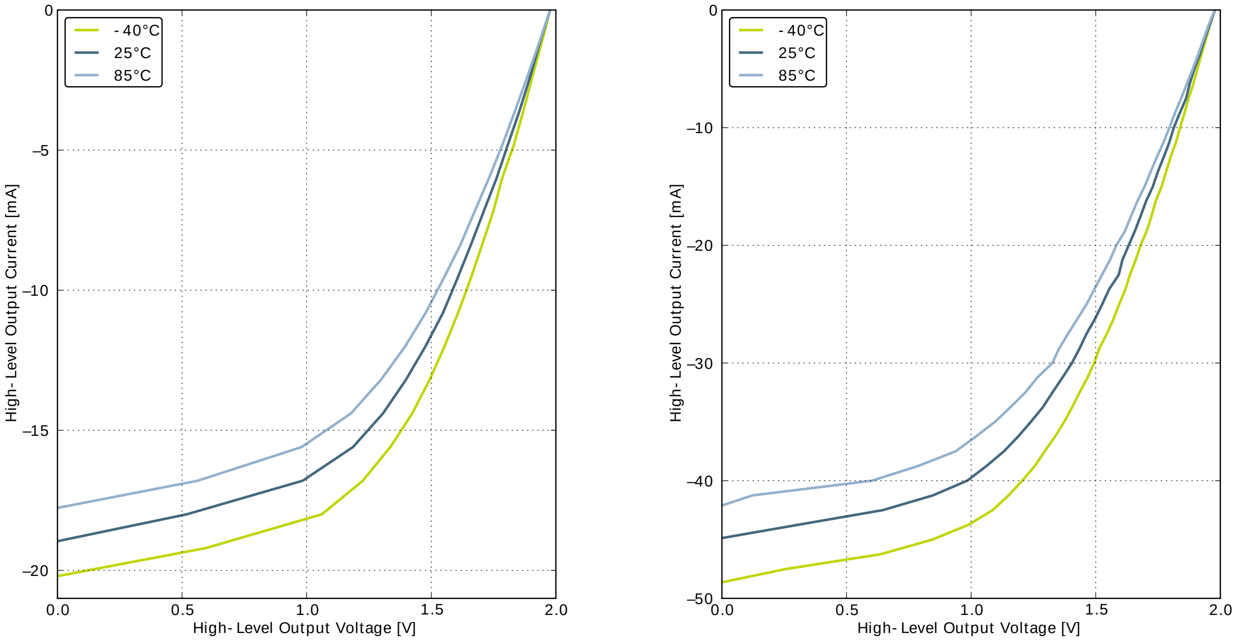
GPIO_Px_CTRL DRIVEMODE = HIGH

*Figure 3.5. Typical High-Level Output Current, 2V Supply Voltage*



GPIO_Px_CTRL DRIVEMODE = LOWEST

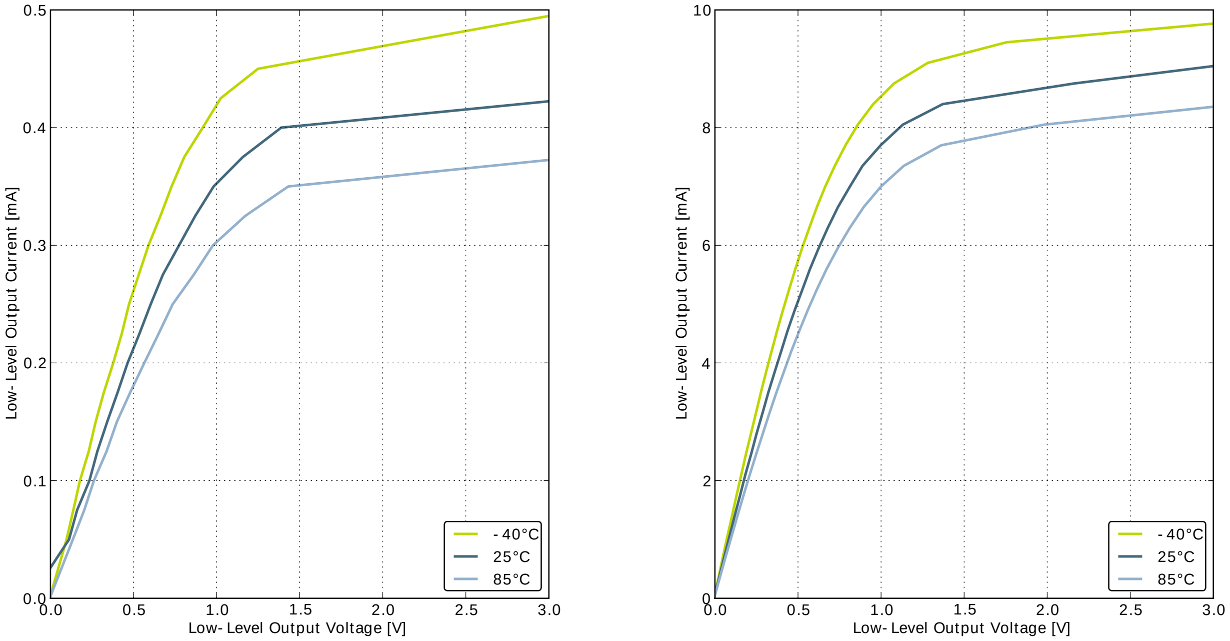
GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

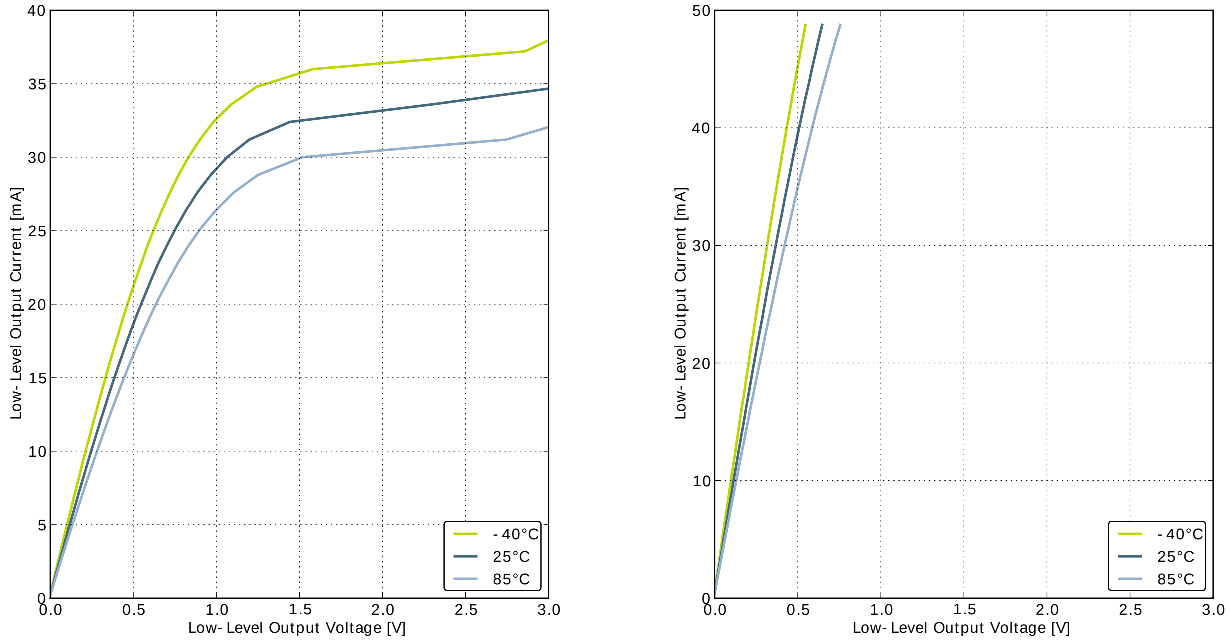
GPIO_Px_CTRL DRIVEMODE = HIGH

### *Figure 3.6. Typical Low-Level Output Current, 3V Supply Voltage*



GPIO_Px_CTRL DRIVEMODE = LOWEST

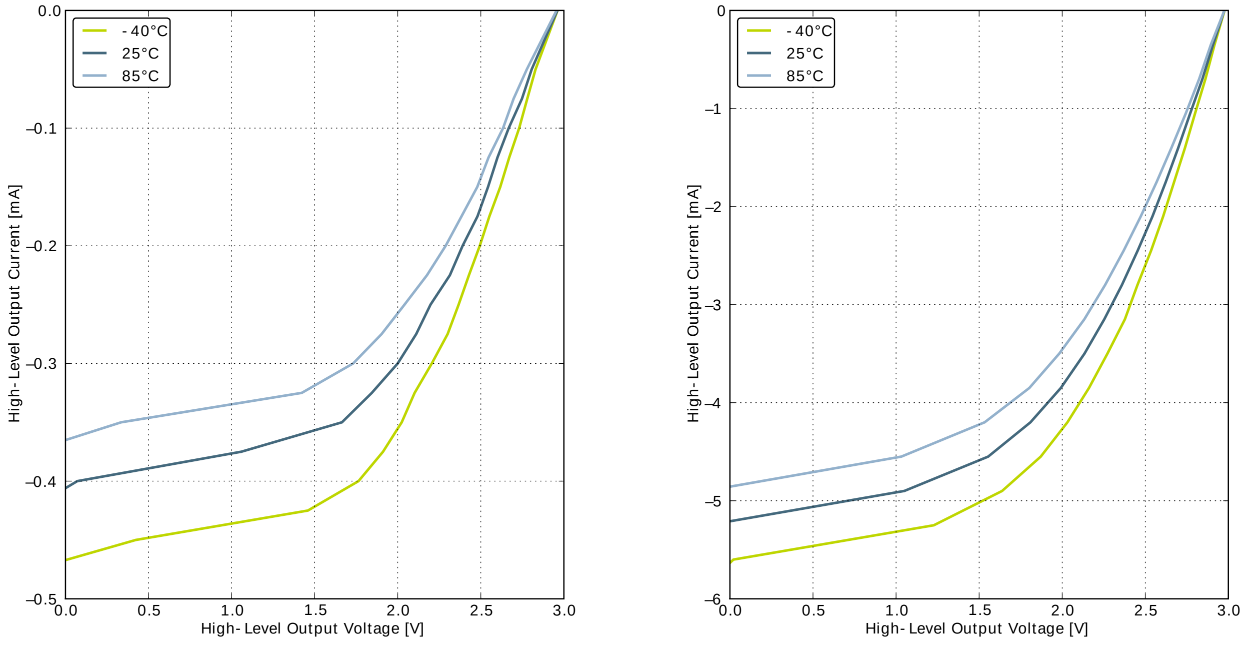
GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

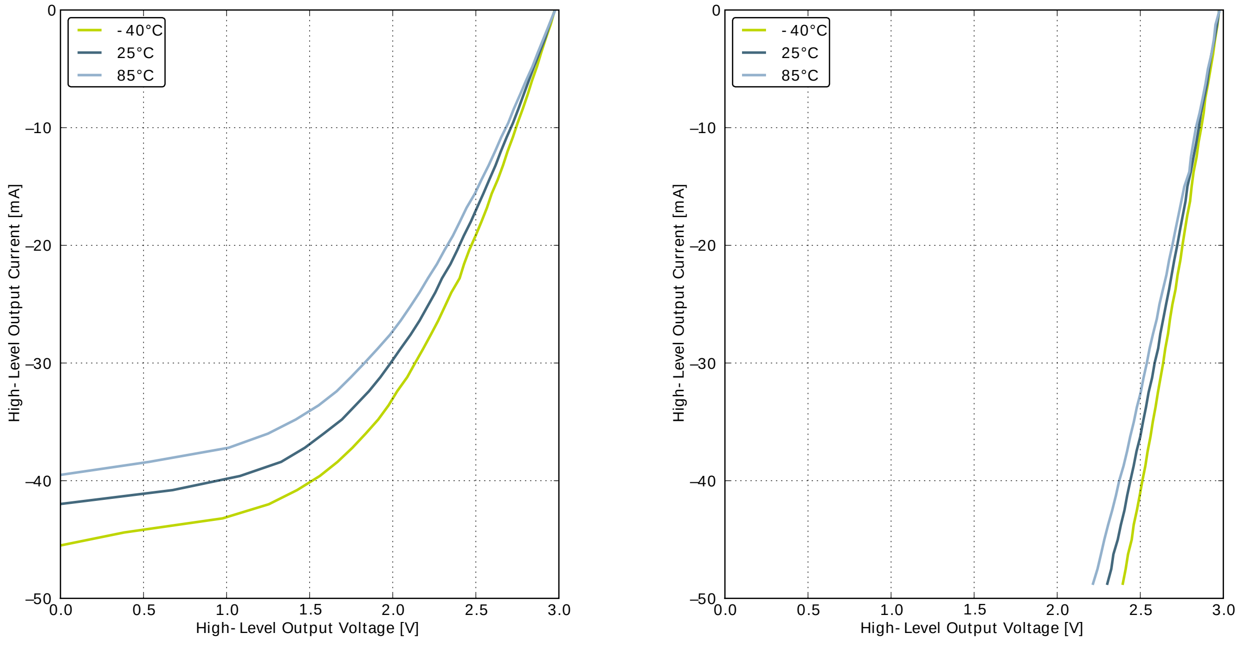
GPIO_Px_CTRL DRIVEMODE = HIGH

*Figure 3.7. Typical High-Level Output Current, 3V Supply Voltage*



GPIO_Px_CTRL DRIVEMODE = LOWEST

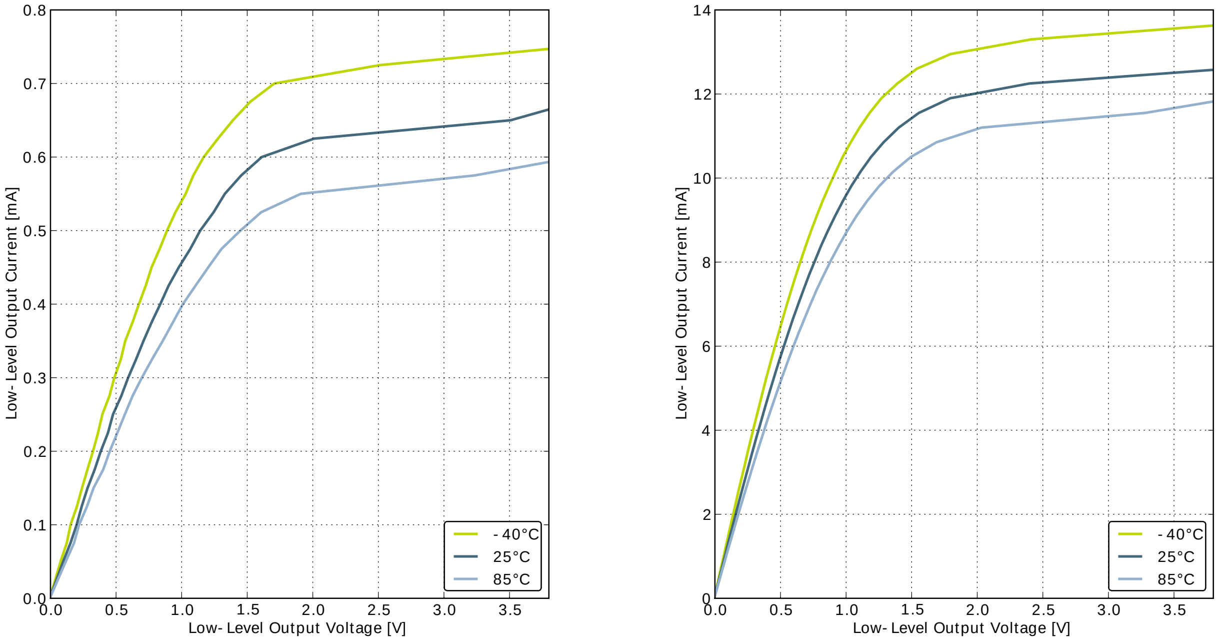
GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

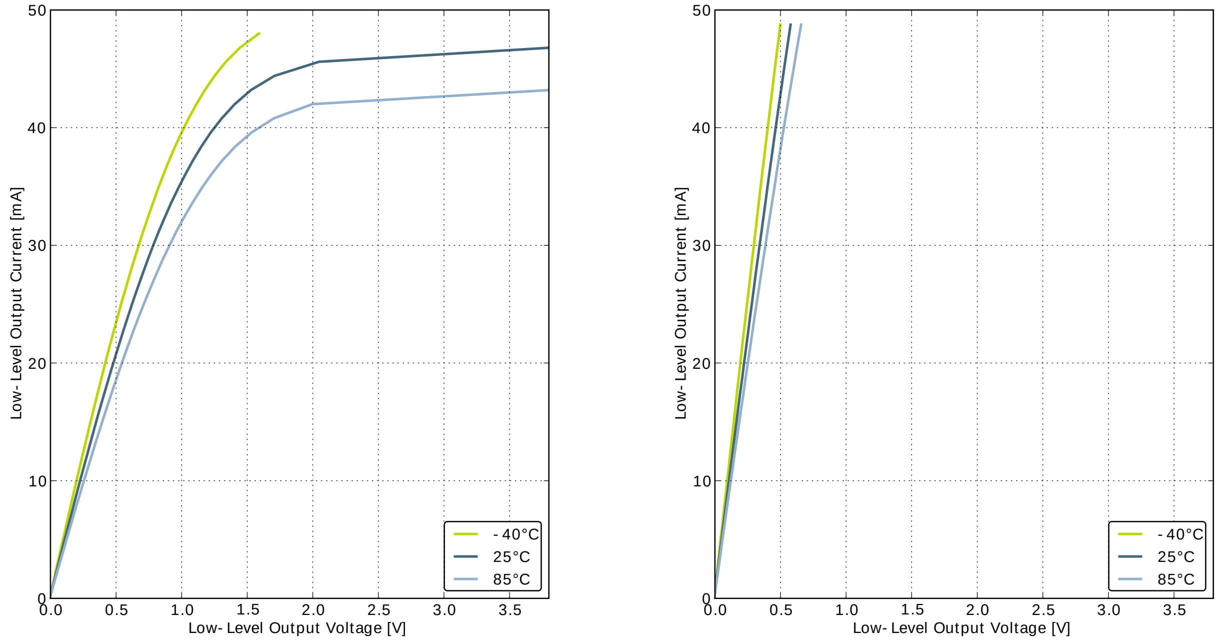
GPIO_Px_CTRL DRIVEMODE = HIGH

*Figure 3.8. Typical Low-Level Output Current, 3.8V Supply Voltage*



GPIO_Px_CTRL DRIVEMODE = LOWEST

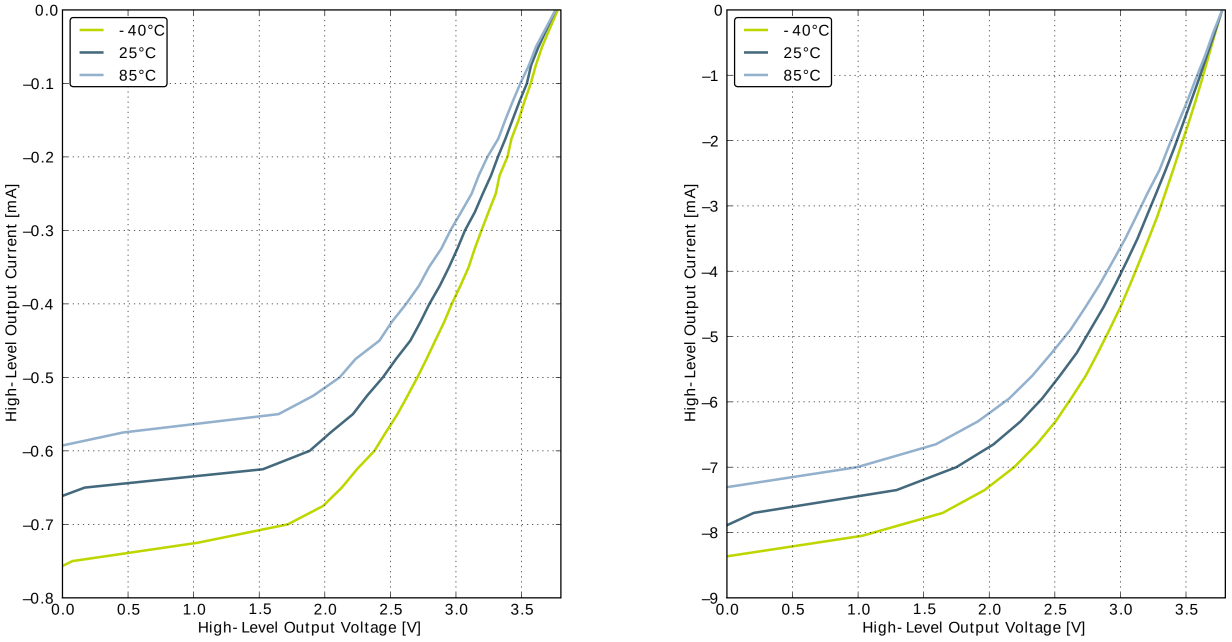
GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

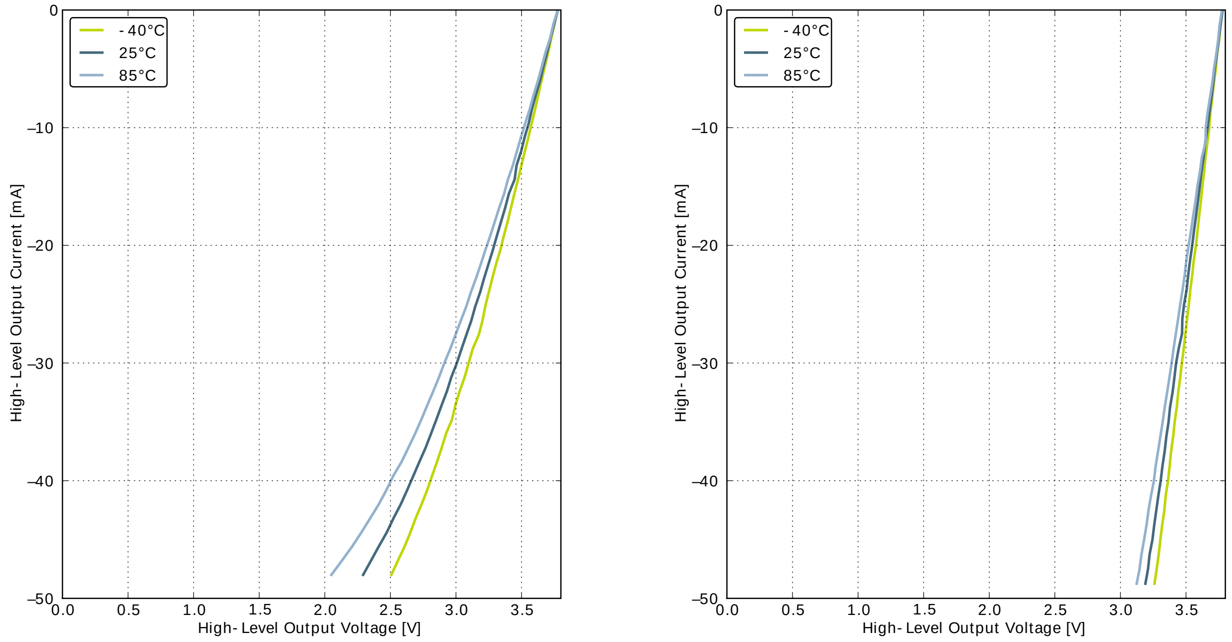
GPIO_Px_CTRL DRIVEMODE = HIGH

## Figure 3.9. Typical High-Level Output Current, 3.8V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = LOWEST

GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

GPIO_Px_CTRL DRIVEMODE = HIGH

## 3.9 Oscillators

### 3.9.1 LFXO

*Table 3.8. LFXO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LFXO}$ | Supported nominal crystal frequency | | | 32.768 | | kHz |
| $ESR_{LFXO}$ | Supported crystal equivalent series resistance (ESR) | | | 30 | 120 | kOhm |
| $C_{LFXOL}$ | Supported crystal external load range | | X[1] | | 25 | pF |
| $DC_{LFXO}$ | Duty cycle | | 48 | 50 | 53.5 | % |
| $I_{LFXO}$ | Current consumption for core and buffer after startup. | ESR=30 kOhm, $C_L$=10 pF, LFXOBOOST in CMU_CTRL is 1 | | 190 | | nA |
| $t_{LFXO}$ | Start- up time. | ESR=30 kOhm, $C_L$=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1 | | 400 | | ms |

[1] See Minimum Load Capacitance ($C_{LFXOL}$) Requirement For Safe Crystal Startup in energyAware Designer in Simplicity Studio

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

### 3.9.2 HFXO

*Table 3.9. HFXO*

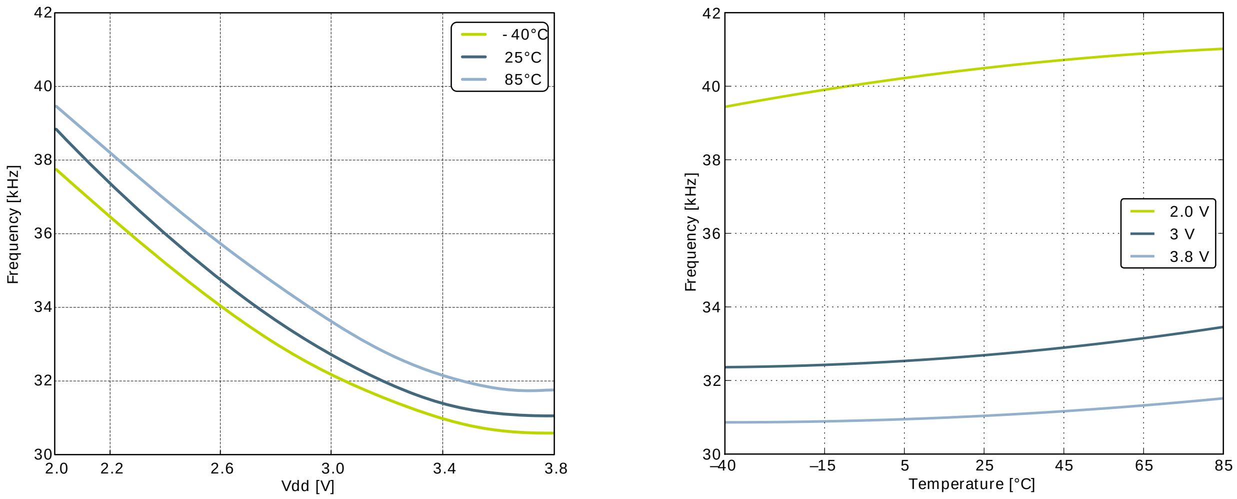
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HFXO}$ | Supported nominal crystal Frequency | | 4 | | 48 | MHz |
| $ESR_{HFXO}$ | Supported crystal equivalent series resistance (ESR) | Crystal frequency 48 MHz | | | 50 | Ohm |
| | | Crystal frequency 32 MHz | | 30 | 60 | Ohm |
| | | Crystal frequency 4 MHz | | 400 | 1500 | Ohm |
| $g_{mHFXO}$ | The transconductance of the HFXO input transistor at crystal startup | HFXOBOOST in CMU_CTRL equals 0b11 | 20 | | | mS |
| $C_{HFXOL}$ | Supported crystal external load range | | 5 | | 25 | pF |
| $I_{HFXO}$ | Current consumption for HFXO after startup | 4 MHz: ESR=400 Ohm, $C_L$=20 pF, HFXOBOOST in CMU_CTRL equals 0b11 | | 85 | | µA |
| | | 32 MHz: ESR=30 Ohm, $C_L$=10 pF, HFXOBOOST in CMU_CTRL equals 0b11 | | 165 | | µA |
| $t_{HFXO}$ | Startup time | 32 MHz: ESR=30 Ohm, $C_L$=10 pF, HFXOBOOST in CMU_CTRL equals 0b11 | | 400 | | µs |

## 3.9.3 LFRCO

*Table 3.10. LFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LFRCO}$ | Oscillation frequency , $V_{DD}$= 3.0 V, $T_{AMB}$=25°C |  | 31.29 | 32.768 | 34.28 | kHz |
| $t_{LFRCO}$ | Startup time not including software calibration |  |  | 150 |  | µs |
| $I_{LFRCO}$ | Current consumption |  |  | 300 | 900 | nA |
| $TUNESTEP_{LFRCO}$ | Frequency step for LSB change in TUNING value |  |  | 1.5 |  | % |

*Figure 3.10. Calibrated LFRCO Frequency vs Temperature and Supply Voltage*



## 3.9.4 HFRCO

*Table 3.11. HFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HFRCO}$ | Oscillation frequency, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | 28 MHz frequency band | 27.5 | 28.0 | 28.5 | MHz |
|  |  | 21 MHz frequency band | 20.6 | 21.0 | 21.4 | MHz |
|  |  | 14 MHz frequency band | 13.7 | 14.0 | 14.3 | MHz |
|  |  | 11 MHz frequency band | 10.8 | 11.0 | 11.2 | MHz |
|  |  | 7 MHz frequency band | 6.48[1] | 6.60[1] | 6.72[1] | MHz |
|  |  | 1 MHz frequency band | 1.15[2] | 1.20[2] | 1.25[2] | MHz |
| $t_{HFRCO\_settling}$ | Settling time after start-up | $f_{HFRCO}$ = 14 MHz |  | 0.6 |  | Cycles |
|  | Settling time after band switch |  |  | 25 |  | Cycles |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{HFRCO}$ | Current consumption (Production test condition = 14MHz) | $f_{HFRCO}$ = 28 MHz | | 165 | 190 | µA |
| | | $f_{HFRCO}$ = 21 MHz | | 134 | 155 | µA |
| | | $f_{HFRCO}$ = 14 MHz | | 106 | 120 | µA |
| | | $f_{HFRCO}$ = 11 MHz | | 94 | 110 | µA |
| | | $f_{HFRCO}$ = 6.6 MHz | | 77 | 90 | µA |
| | | $f_{HFRCO}$ = 1.2 MHz | | 25 | 32 | µA |
| $TUNESTEP_{HFRCO}$ | Frequency step for LSB change in TUNING value | | | 0.3[3] | | % |

[1] For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

[2] For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

[3] The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

**Figure 3.11. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature**

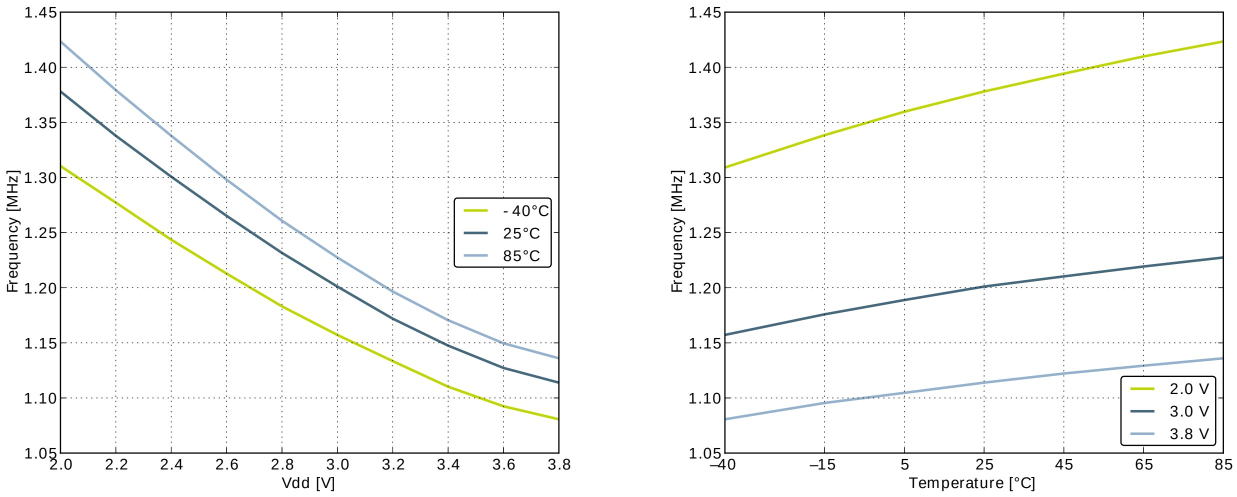


**Figure 3.12. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature**

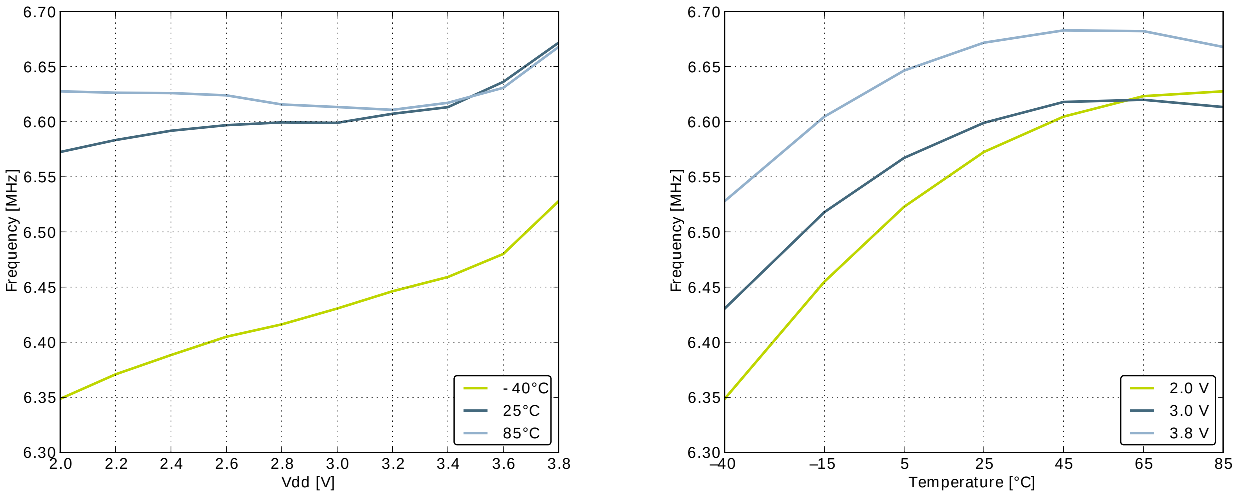


Figure 3.13. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature

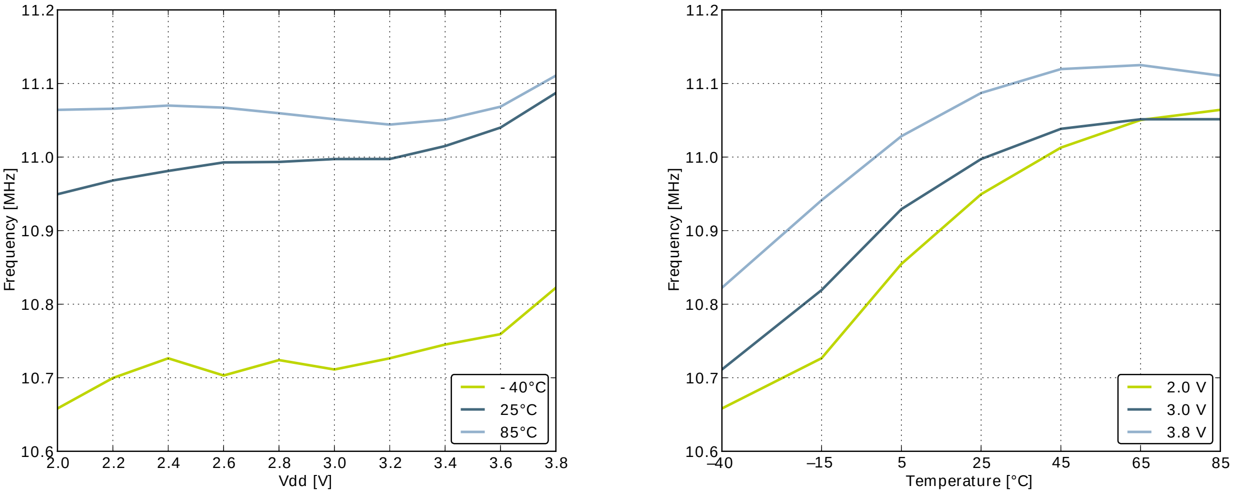


Figure 3.14. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature

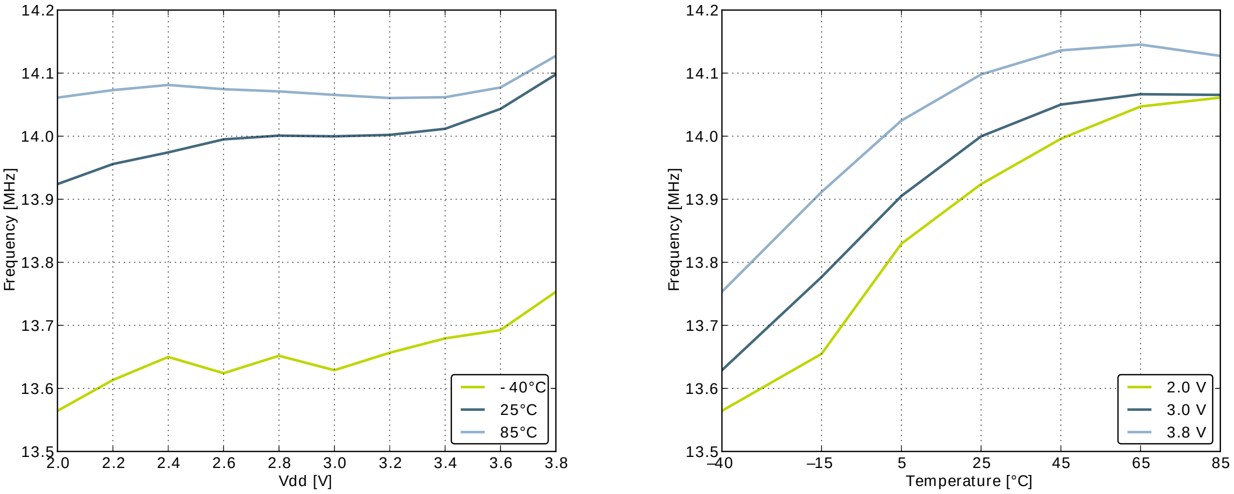


Figure 3.15. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature

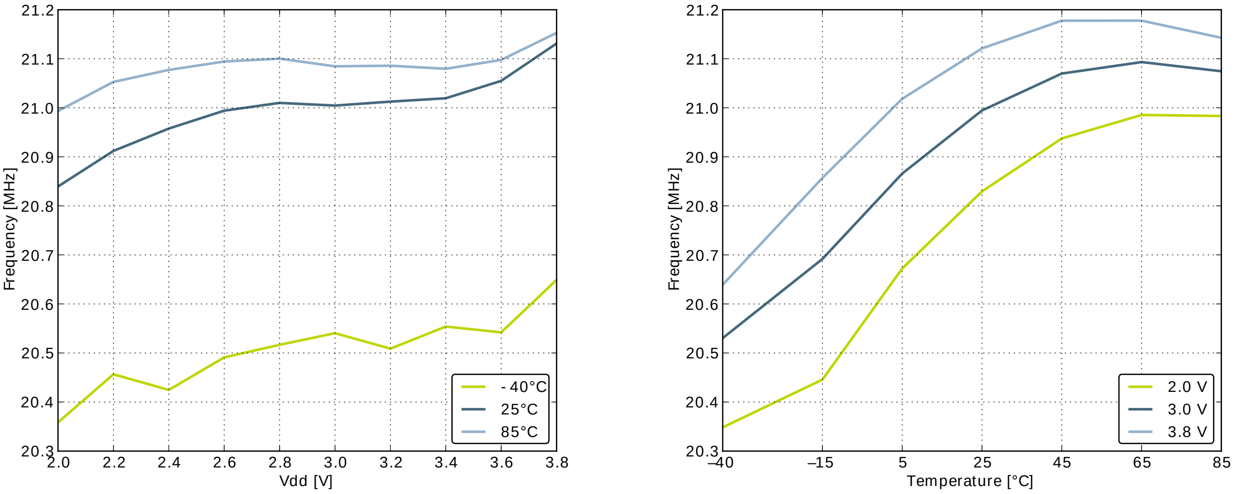
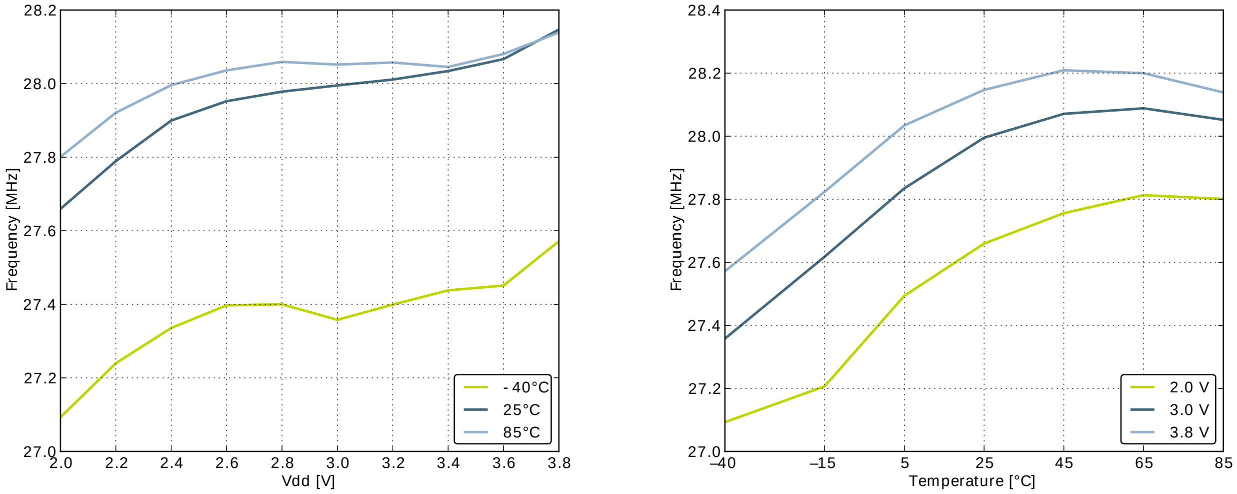


*Figure 3.16. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature*



## 3.9.5 AUXHFRCO

*Table 3.12. AUXHFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{AUXHFRCO}$ | Oscillation frequency, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | 28 MHz frequency band | 27.5 | 28.0 | 28.5 | MHz |
| | | 21 MHz frequency band | 20.6 | 21.0 | 21.4 | MHz |
| | | 14 MHz frequency band | 13.7 | 14.0 | 14.3 | MHz |
| | | 11 MHz frequency band | 10.8 | 11.0 | 11.2 | MHz |
| | | 7 MHz frequency band | 6.48[1] | 6.60[1] | 6.72[1] | MHz |
| | | 1 MHz frequency band | 1.15[2] | 1.20[2] | 1.25[2] | MHz |
| $t_{AUXHFRCO\_settling}$ | Settling time after start-up | $f_{AUXHFRCO}$ = 14 MHz | | 0.6 | | Cycles |
| $DC_{AUXHFRCO}$ | Duty cycle | $f_{AUXHFRCO}$ = 14 MHz | 48.5 | 50 | 51 | % |
| $TUNESTEP_{AUXHFRCO}$ | Frequency step for LSB change in TUNING value | | | 0.3[3] | | % |

[1] For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

[2] For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

[3] The TUNING field in the CMU_AUXHFRCOCTRL register may be used to adjust the AUXHFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

### 3.9.6 ULFRCO

*Table 3.13. ULFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{ULFRCO}$ | Oscillation frequency | 25°C, 3V | 0.70 | | 1.75 | kHz |
| $TC_{ULFRCO}$ | Temperature coefficient | | | 0.05 | | %/°C |
| $VC_{ULFRCO}$ | Supply voltage coefficient | | | -18.2 | | %/V |

## 3.10 Analog Digital Converter (ADC)

*Table 3.14. ADC*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ADCIN}$ | Input voltage range | Single ended | 0 | | $V_{REF}$ | V |
| | | Differential | $-V_{REF}/2$ | | $V_{REF}/2$ | V |
| $V_{ADCREFIN}$ | Input range of external reference voltage, single ended and differential | | 1.25 | | $V_{DD}$ | V |
| $V_{ADCREFIN\_CH7}$ | Input range of external negative reference voltage on channel 7 | See $V_{ADCREFIN}$ | 0 | | $V_{DD}$ - 1.1 | V |
| $V_{ADCREFIN\_CH6}$ | Input range of external positive reference voltage on channel 6 | See $V_{ADCREFIN}$ | 0.625 | | $V_{DD}$ | V |
| $V_{ADCCMIN}$ | Common mode input range | | 0 | | $V_{DD}$ | V |
| $I_{ADCIN}$ | Input current | 2pF sampling capacitors | | <100 | | nA |
| $CMRR_{ADC}$ | Analog input common mode rejection ratio | | | 65 | | dB |
| $I_{ADC}$ | Average active current | 1 MSamples/s, 12 bit, external reference | | 351 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00 | | 67 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01 | | 63 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10 | | 64 | | µA |
| $I_{ADCREF}$ | Current consumption of internal voltage reference | Internal voltage reference | | 65 | | µA |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_{ADCIN}$ | Input capacitance | | | 2 | | pF |
| $R_{ADCIN}$ | Input ON resistance | | 1 | | | MOhm |
| $R_{ADCFILT}$ | Input RC filter resistance | | | 10 | | kOhm |
| $C_{ADCFILT}$ | Input RC filter/decoupling capacitance | | | 250 | | fF |
| $f_{ADCCLK}$ | ADC Clock Frequency | | | | 13 | MHz |
| $t_{ADCCONV}$ | Conversion time | 6 bit | 7 | | | ADC-CLK Cycles |
| | | 8 bit | 11 | | | ADC-CLK Cycles |
| | | 12 bit | 13 | | | ADC-CLK Cycles |
| $t_{ADCACQ}$ | Acquisition time | Programmable | 1 | | 256 | ADC-CLK Cycles |
| $t_{ADCACQVDD3}$ | Required acquisition time for VDD/3 reference | | 2 | | | µs |
| $t_{ADCSTART}$ | Startup time of reference generator and ADC core in NORMAL mode | | | 5 | | µs |
| | Startup time of reference generator and ADC core in KEEPADCWARM mode | | | 1 | | µs |
| $SNR_{ADC}$ | Signal to Noise Ratio (SNR) | 1 MSamples/s, 12 bit, single ended, internal 1.25V reference | | 59 | | dB |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5V reference | | 63 | | dB |
| | | 1 MSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 65 | | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25V reference | | 60 | | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5V reference | | 65 | | dB |
| | | 1 MSamples/s, 12 bit, differential, 5V reference | | 54 | | dB |
| | | 1 MSamples/s, 12 bit, differential, $V_{DD}$ reference | | 67 | | dB |
| | | 1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference | | 69 | | dB |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 62 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 63 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 67 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | | 63 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference | 63 | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference | | 70 | | dB |
| $\text{SINAD}_{ADC}$ | SIgnal-to-Noise And Distortion-ratio (SINAD) | 1 MSamples/s, 12 bit, single ended, internal 1.25V reference | | 58 | | dB |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5V reference | | 62 | | dB |
| | | 1 MSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 64 | | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25V reference | | 60 | | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5V reference | | 64 | | dB |
| | | 1 MSamples/s, 12 bit, differential, 5V reference | | 54 | | dB |
| | | 1 MSamples/s, 12 bit, differential, $V_{DD}$ reference | | 66 | | dB |
| | | 1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference | | 68 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 61 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 65 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | | 63 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference | 62 | 65 | | dB |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 200 kSamples/s, 12 bit, differential, 2x$V_{DD}$ reference | | 69 | | dB |
| $SFDR_{ADC}$ | Spurious-Free Dynamic Range (SFDR) | 1 MSamples/s, 12 bit, single ended, internal 1.25V reference | | 64 | | dBc |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5V reference | | 76 | | dBc |
| | | 1 MSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 73 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25V reference | | 66 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5V reference | | 77 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, $V_{DD}$ reference | | 76 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, 2x$V_{DD}$ reference | | 75 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, 5V reference | | 69 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 75 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 75 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 76 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | | 78 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference | 68 | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, 2x$V_{DD}$ reference | | 79 | | dBc |
| $V_{ADCOFFSET}$ | Offset voltage | After calibration, single ended | | 0.3 | | mV |
| | | After calibration, differential | -3 | 0.3 | 3 | mV |
| $TGRAD_{ADCTH}$ | Thermometer output gradient | | | -1.92 | | mV/°C |
| | | | | -6.3 | | ADC Codes/°C |
| $DNL_{ADC}$ | Differential non-linearity (DNL) | $V_{DD}$= 3.0 V, external 2.5V reference | -1 | ±0.7 | 4 | LSB |
| $INL_{ADC}$ | Integral non-linearity (INL), End point method | | | ±1.2 | ±3.0 | LSB |
| $MC_{ADC}$ | No missing codes | | 11.999[1] | 12 | | bits |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $GAIN_{ED}$ | Gain error drift | 1.25V reference | | 0.01[2] | 0.033[3] | %/°C |
| | | 2.5V reference | | 0.01[2] | 0.03[3] | %/°C |
| $OFFSET_{ED}$ | Offset error drift | 1.25V reference | | 0.2[2] | 0.7[3] | LSB/°C |
| | | 2.5V reference | | 0.2[2] | 0.62[3] | LSB/°C |

[1] On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

[2] Typical numbers given by abs(Mean) / (85 - 25).

[3] Max number given by (abs(Mean) + 3x stddev) / (85 - 25).

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.17 (p. 32) and Figure 3.18 (p. 33) , respectively.

*Figure 3.17. Integral Non-Linearity (INL)*

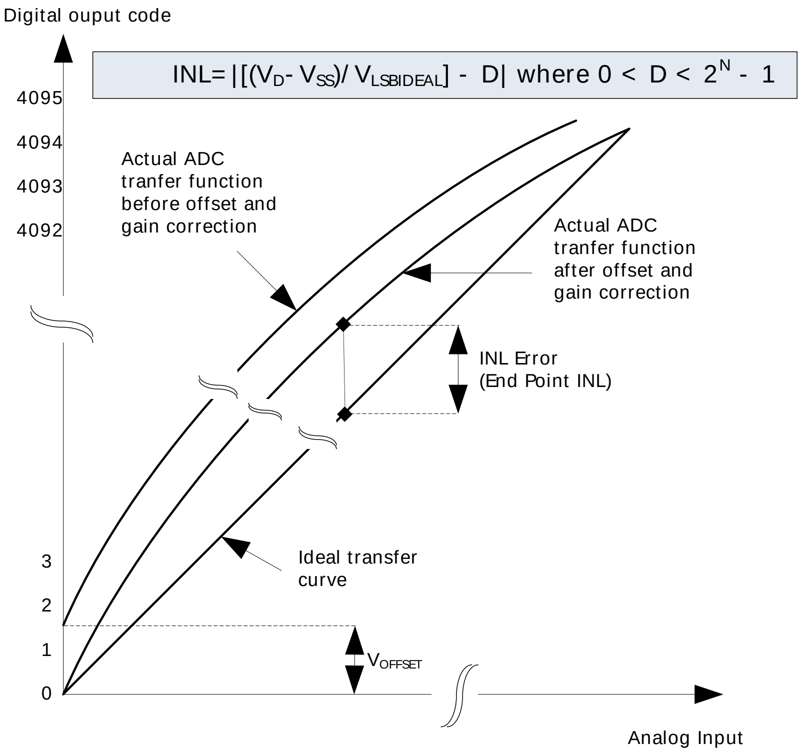
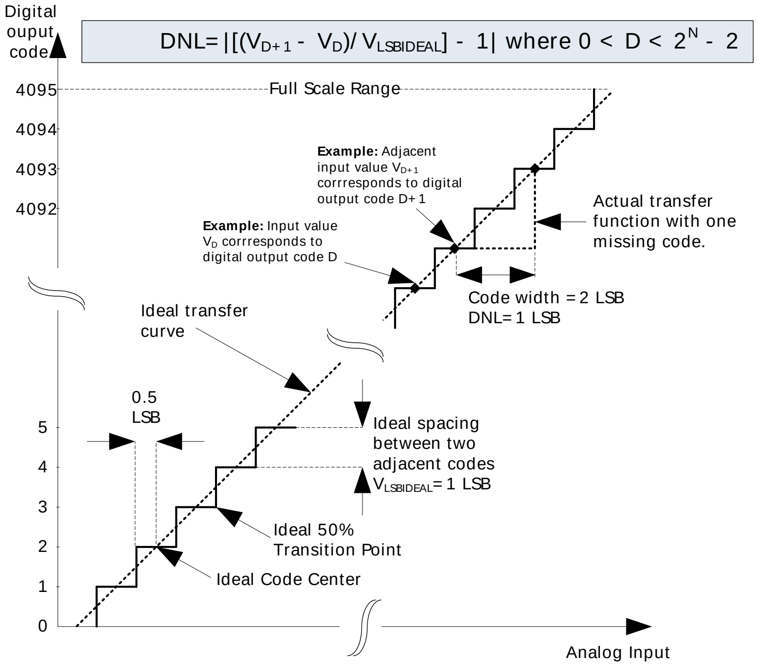
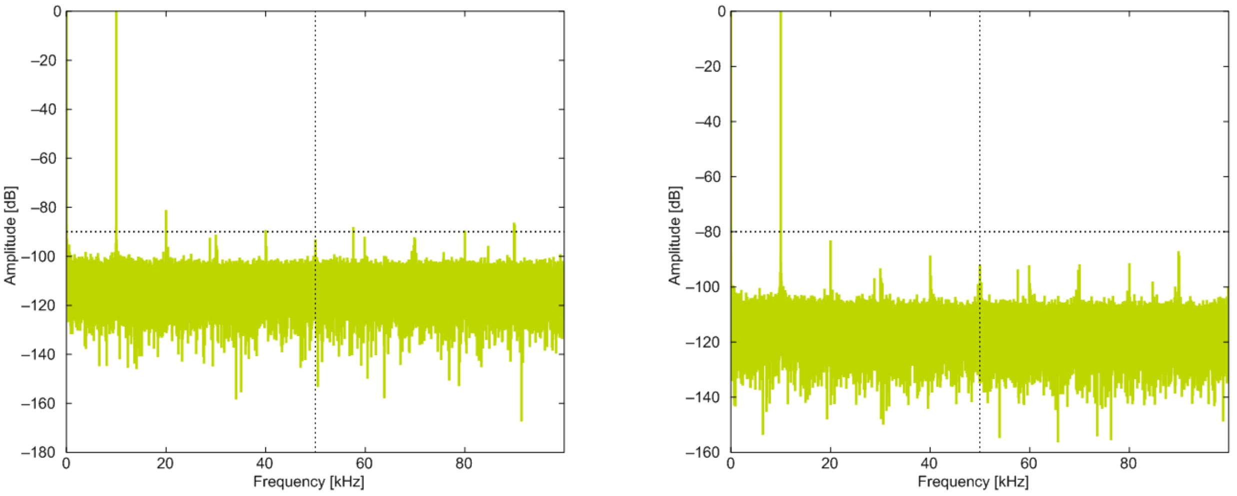

Digital ouput code
$INL = |[(V_D - V_{SS})/V_{LSBIDEAL}] - D|$ where $0 < D < 2^N - 1$
4095
4094
4093
4092
Actual ADC tranfer function before offset and gain correction
Actual ADC tranfer function after offset and gain correction
INL Error (End Point INL)
Ideal transfer curve
3
2
1
0
$V_{OFFSET}$
Analog Input

***Figure 3.18. Differential Non-Linearity (DNL)***


Digital ouput code
DNL=|[(V_{D+1} - V_D)/V_{LSBIDEAL}] - 1| where 0 < D < 2^N - 2
4095
Full Scale Range
4094
4093
4092
Example: Adjacent input value V_{D+1} corrresponds to digital output code D+1
Example: Input value V_D corrresponds to digital output code D
Actual transfer function with one missing code.
Code width = 2 LSB
DNL= 1 LSB
Ideal transfer curve
0.5 LSB
5
4
3
2
1
0
Ideal spacing between two adjacent codes V_{LSBIDEAL}= 1 LSB
Ideal 50% Transition Point
Ideal Code Center
Analog Input

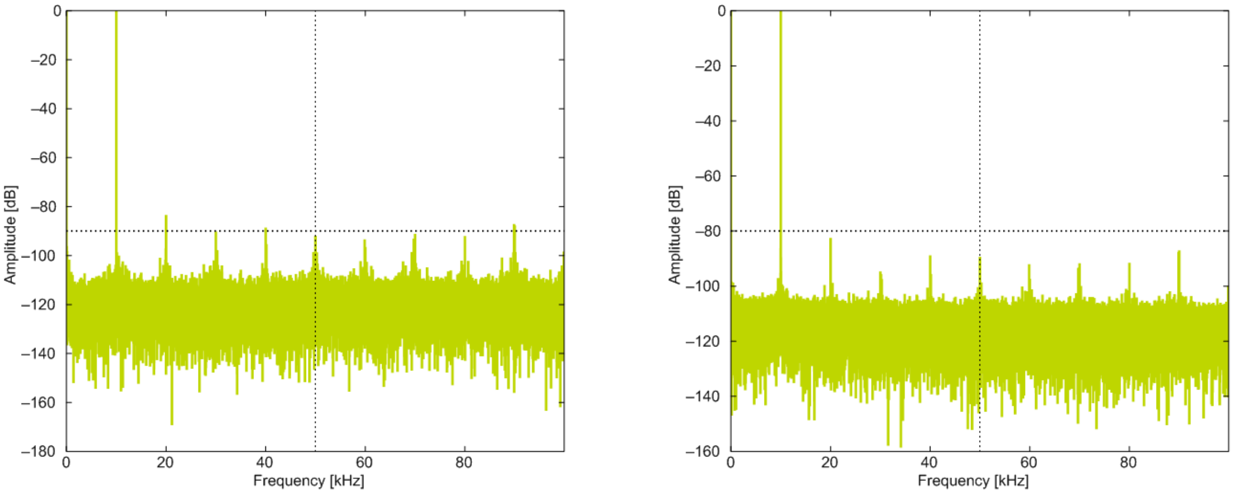
### 3.10.1 Typical performance

*Figure 3.19. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C*



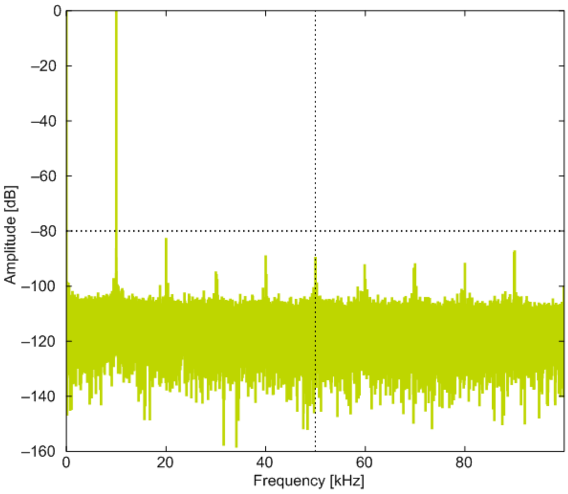
1.25V Reference

2.5V Reference



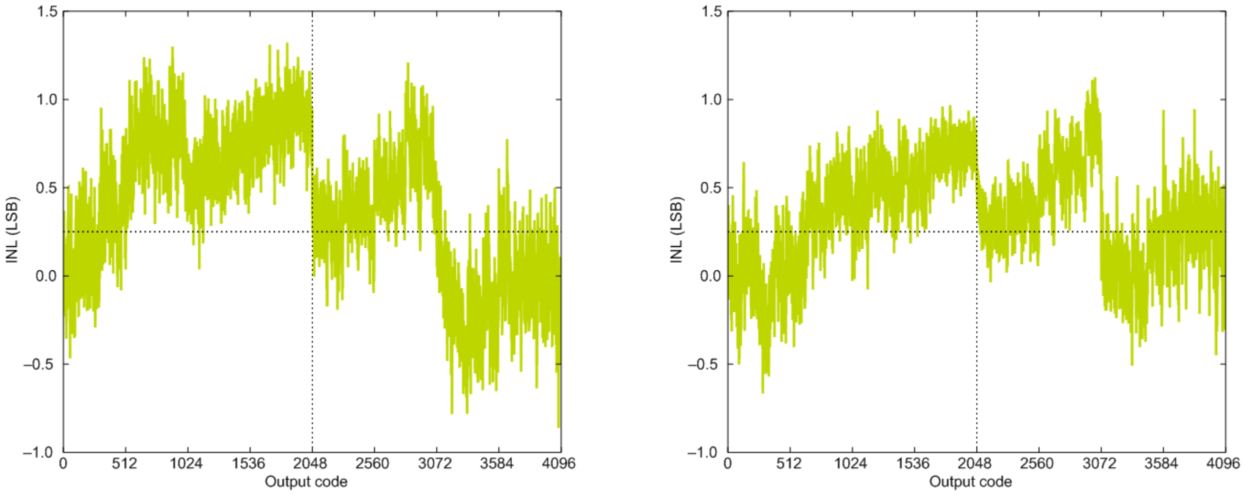
2XVDDVSS Reference

5VDIFF Reference



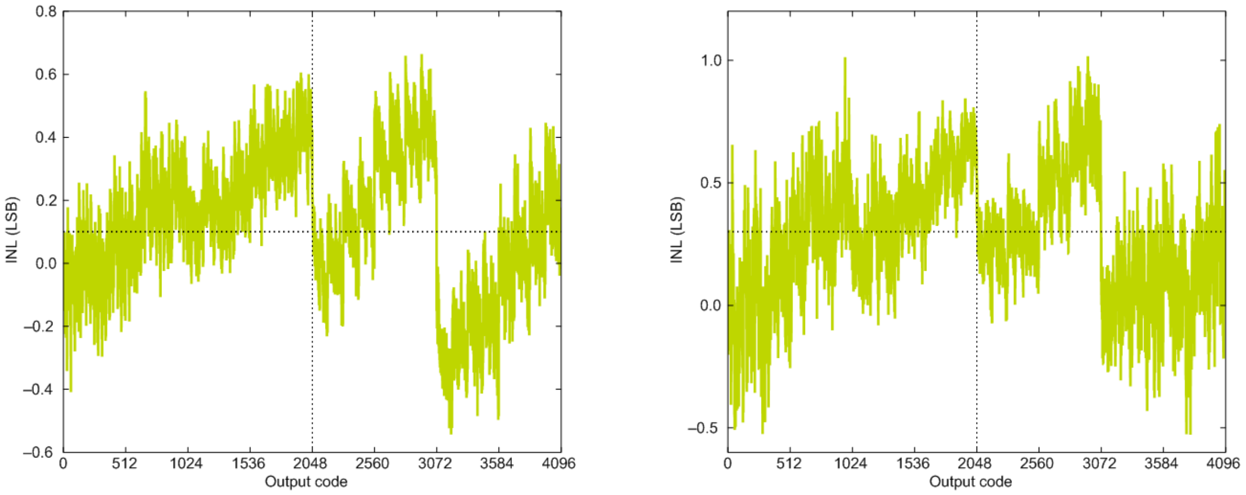
VDD Reference

Figure 3.20. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C



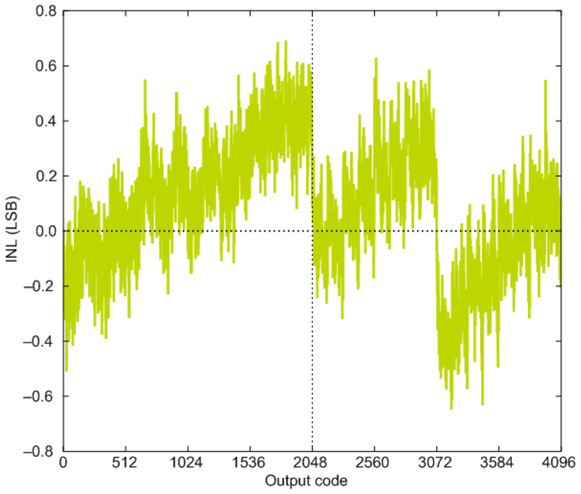
1.25V Reference

2.5V Reference



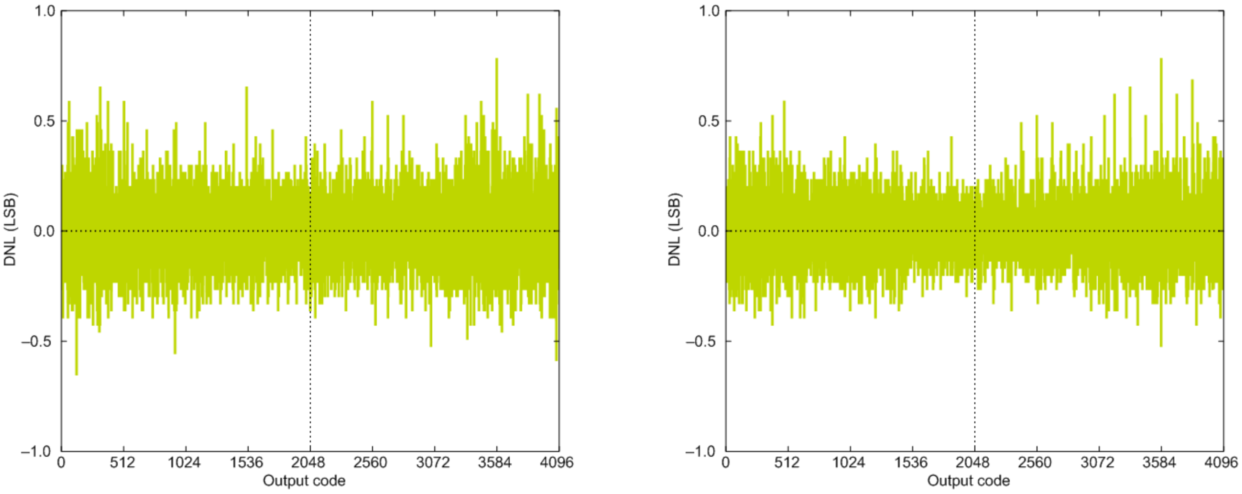
2XVDDVSS Reference

5VDIFF Reference



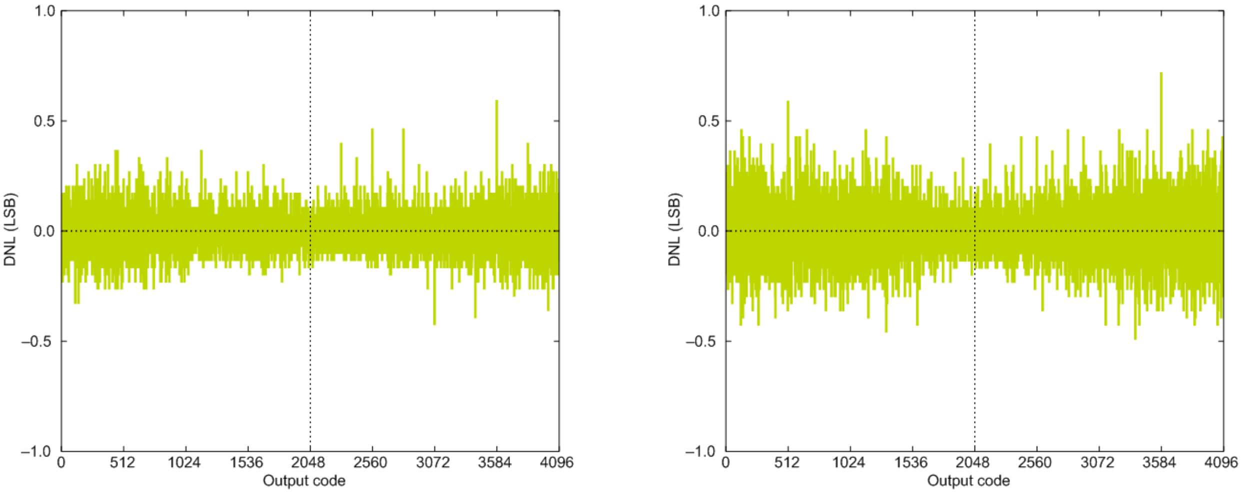
VDD Reference

**Figure 3.21. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C**



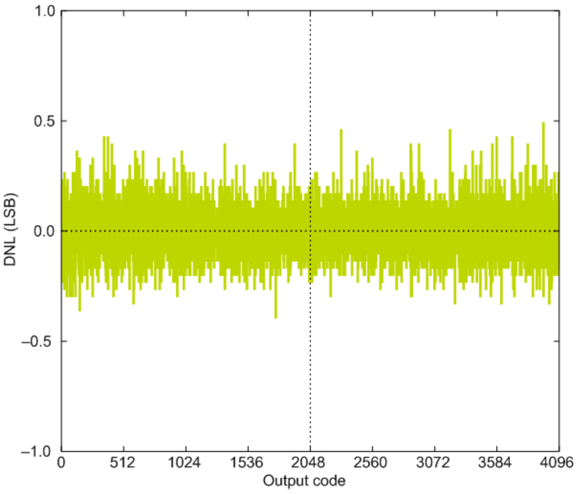
1.25V Reference

2.5V Reference



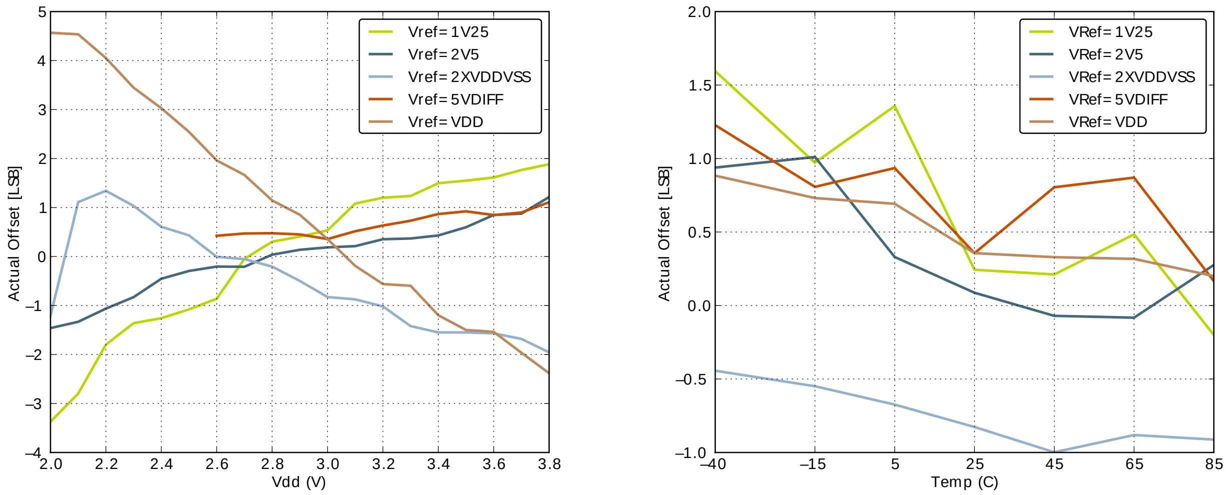
2XVDDVSS Reference

5VDIFF Reference



VDD Reference

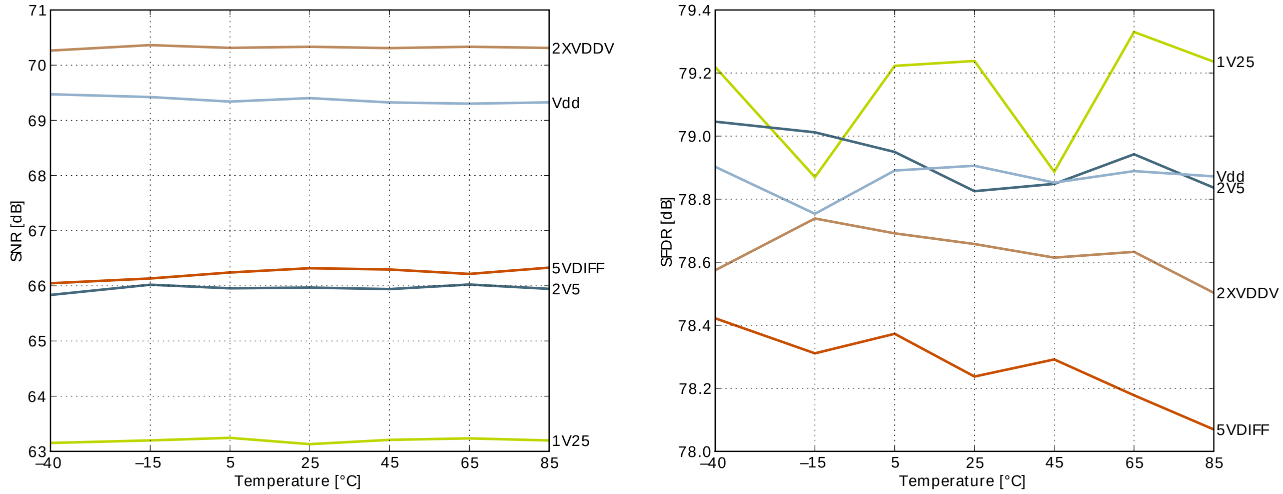
*Figure 3.22. ADC Absolute Offset, Common Mode = Vdd /2*



Offset vs Supply Voltage, Temp = 25°C

Offset vs Temperature, Vdd = 3V

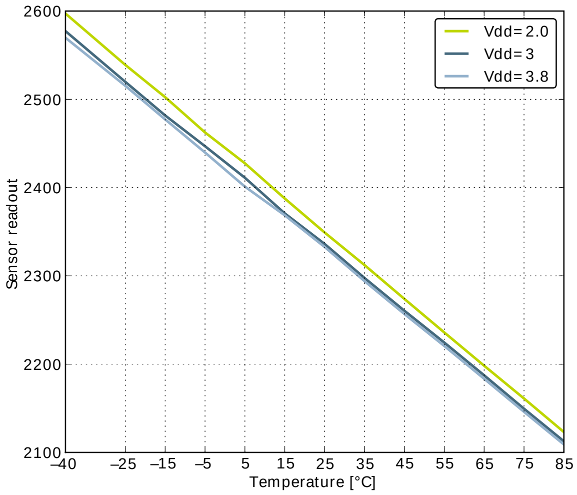
*Figure 3.23. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V*



Signal to Noise Ratio (SNR)

Spurious-Free Dynamic Range (SFDR)

*Figure 3.24.  ADC Temperature sensor readout*



## 3.11 Digital Analog Converter (DAC)

*Table 3.15. DAC*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DACOUT}$ | Output voltage range | VDD voltage reference, single ended | 0 | | $V_{DD}$ | V |
| | | VDD voltage reference, differential | $-V_{DD}$ | | $V_{DD}$ | V |
| $V_{DACCM}$ | Output common mode voltage range | | 0 | | $V_{DD}$ | V |
| $I_{DAC}$ | Active current including references for 2 channels | 500 kSamples/s, 12 bit | | 400[1] | 600[1] | µA |
| | | 100 kSamples/s, 12 bit | | 200[1] | 260[1] | µA |
| | | 1 kSamples/s 12 bit NORMAL | | 17[1] | 25[1] | µA |
| $SR_{DAC}$ | Sample rate | | | | 500 | ksamples/s |
| $f_{DAC}$ | DAC clock frequency | Continuous Mode | | | 1000 | kHz |
| | | Sample/Hold Mode | | | 250 | kHz |
| | | Sample/Off Mode | | | 250 | kHz |
| $CYC_{DACCONV}$ | Clock cyckles per conversion | | | 2 | | |
| $t_{DACCONV}$ | Conversion time | | 2 | | | µs |
| $t_{DACSETTLE}$ | Settling time | | | 5 | | µs |
| $SNR_{DAC}$ | Signal to Noise Ratio (SNR) | 500 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 58 | | dB |
| | | 500 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 59 | | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25V reference | | 58 | | dB |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 500 kSamples/s, 12 bit, differential, internal 2.5V reference | | 58 | | dB |
| | | 500 kSamples/s, 12 bit, differential, $V_{DD}$ reference | | 59 | | dB |
| $SNDR_{DAC}$ | Signal to Noise-pulse Distortion Ratio (SNDR) | 500 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 57 | | dB |
| | | 500 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 54 | | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25V reference | | 56 | | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 2.5V reference | | 53 | | dB |
| | | 500 kSamples/s, 12 bit, differential, $V_{DD}$ reference | | 55 | | dB |
| $SFDR_{DAC}$ | Spurious-Free Dynamic Range(SFDR) | 500 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 62 | | dBc |
| | | 500 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 56 | | dBc |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25V reference | | 61 | | dBc |
| | | 500 kSamples/s, 12 bit, differential, internal 2.5V reference | | 55 | | dBc |
| | | 500 kSamples/s, 12 bit, differential, $V_{DD}$ reference | | 60 | | dBc |
| $V_{DACOFFSET}$ | Offset voltage | After calibration, single ended | | 2 | 12 | mV |
| | | After calibration, differential | | 2 | | mV |
| $DNL_{DAC}$ | Differential non-linearity | | | ±1 | | LSB |
| $INL_{DAC}$ | Integral non-linearity | | | ±5 | | LSB |
| $MC_{DAC}$ | No missing codes | | | 12 | | bits |

[1] Measured with a static input code and no loading on the output.

## 3.12 Operational Amplifier (OPAMP)

The electrical characteristics for the Operational Amplifiers are based on simulations.

*Table 3.16. OPAMP*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{OPAMP}$ | Active Current | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, Unity Gain | | 350 | 405 | µA |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, Unity Gain | | 95 | 115 | µA |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, Unity Gain | | 13 | 17 | µA |
| $G_{OL}$ | Open Loop Gain | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0 | | 101 | | dB |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1 | | 98 | | dB |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1 | | 91 | | dB |
| $GBW_{OPAMP}$ | Gain Bandwidth Product | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0 | | 6.1 | | MHz |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1 | | 1.8 | | MHz |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1 | | 0.25 | | MHz |
| $PM_{OPAMP}$ | Phase Margin | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, $C_L$=75 pF | | 64 | | ° |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, $C_L$=75 pF | | 58 | | ° |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, $C_L$=75 pF | | 58 | | ° |
| $R_{INPUT}$ | Input Resistance | | | 100 | | Mohm |
| $R_{LOAD}$ | Load Resistance | | 200 | | | Ohm |
| $I_{LOAD\_DC}$ | DC Load Current | | | | 11 | mA |
| $V_{INPUT}$ | Input Voltage | OPAxHCMDIS=0 | $V_{SS}$ | | $V_{DD}$ | V |
| | | OPAxHCMDIS=1 | $V_{SS}$ | | $V_{DD}$-1.2 | V |
| $V_{OUTPUT}$ | Output Voltage | | $V_{SS}$ | | $V_{DD}$ | V |
| $V_{OFFSET}$ | Input Offset Voltage | Unity Gain, $V_{SS}<V_{in}<V_{DD}$, OPAxHCMDIS=0 | -13 | 0 | 11 | mV |
| | | Unity Gain, $V_{SS}<V_{in}<V_{DD}-1.2$, OPAxHCMDIS=1 | | 1 | | mV |
| $V_{OFFSET\_DRIFT}$ | Input Offset Voltage Drift | | | | 0.02 | mV/°C |
| $SR_{OPAMP}$ | Slew Rate | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0 | | 3.2 | | V/µs |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1 | | 0.8 | | V/µs |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1 | | 0.1 | | V/µs |
| $N_{OPAMP}$ | Voltage Noise | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx-HCMDIS=0 | | 101 | | µ$V_{RMS}$ |
| | | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx-HCMDIS=1 | | 141 | | µ$V_{RMS}$ |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAxHCMDIS=0 | | 196 | | $\mu V_{RMS}$ |
| | | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAxHCMDIS=1 | | 229 | | $\mu V_{RMS}$ |
| | | RESSEL=7, 0.1 Hz<f<10 kHz, OPAxHCMDIS=0 | | 1230 | | $\mu V_{RMS}$ |
| | | RESSEL=7, 0.1 Hz<f<10 kHz, OPAxHCMDIS=1 | | 2130 | | $\mu V_{RMS}$ |
| | | RESSEL=7, 0.1 Hz<f<1 MHz, OPAxHCMDIS=0 | | 1630 | | $\mu V_{RMS}$ |
| | | RESSEL=7, 0.1 Hz<f<1 MHz, OPAxHCMDIS=1 | | 2590 | | $\mu V_{RMS}$ |

*Figure 3.25. OPAMP Common Mode Rejection Ratio*

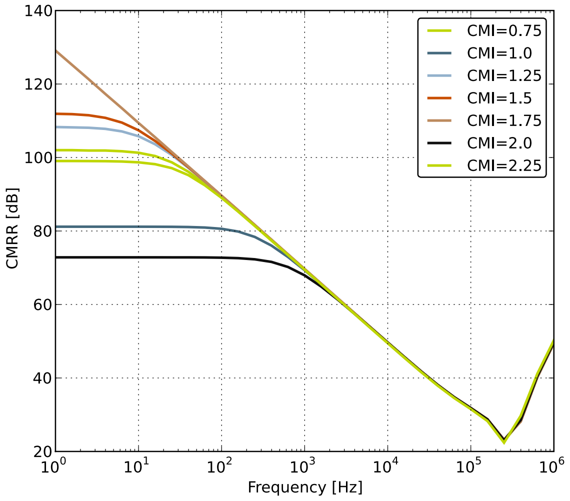
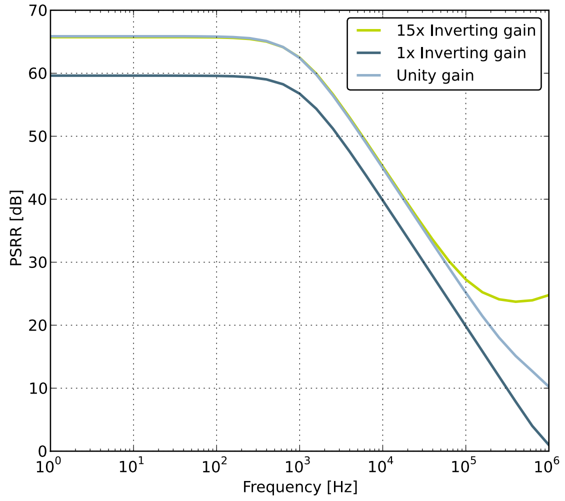
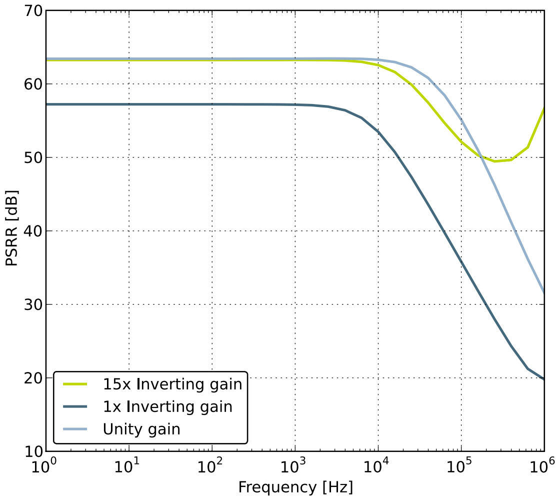


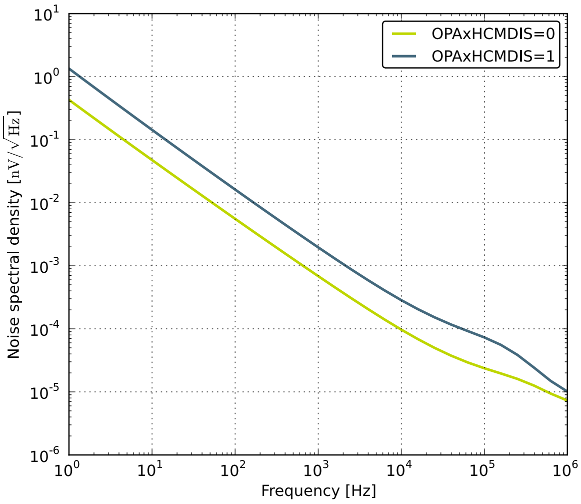
*Figure 3.26. OPAMP Positive Power Supply Rejection Ratio*



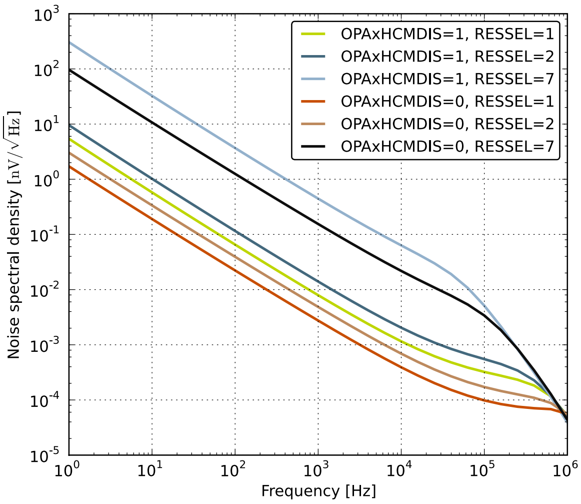
### Figure 3.27. OPAMP Negative Power Supply Rejection Ratio



### Figure 3.28. OPAMP Voltage Noise Spectral Density (Unity Gain) $V_{out}$=1V



### Figure 3.29. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)



## 3.13 Analog Comparator (ACMP)

*Table 3.17. ACMP*

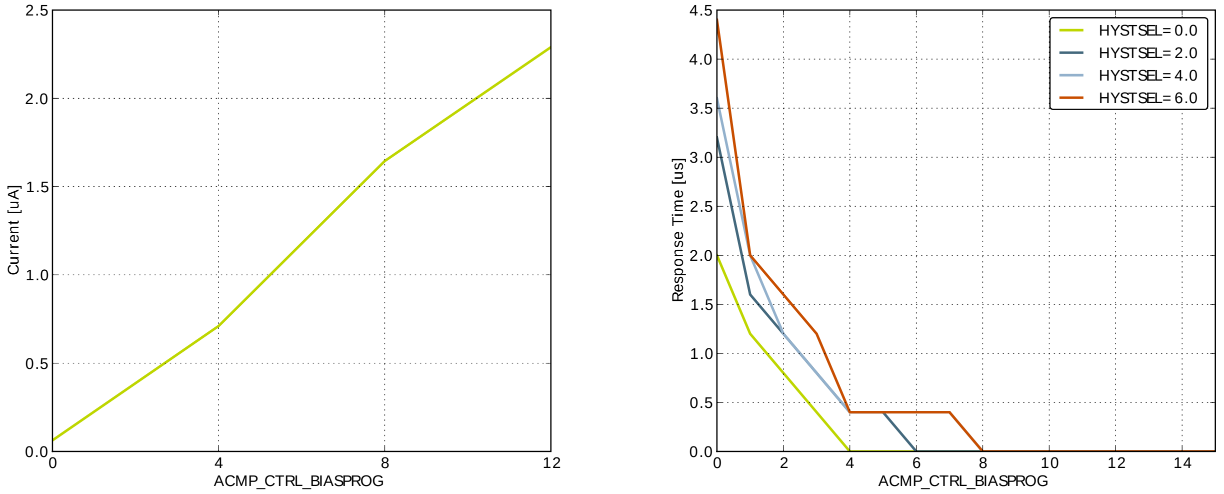
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ACMPIN}$ | Input voltage range | | 0 | | $V_{DD}$ | V |
| $V_{ACMPCM}$ | ACMP Common Mode voltage range | | 0 | | $V_{DD}$ | V |
| $I_{ACMP}$ | Active current | BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register | | 0.1 | 0.6 | µA |
| | | BIASPROG=0b1111, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register | | 2.87 | 12 | µA |
| | | BIASPROG=0b1111, FULLBIAS=1 and HALFBIAS=0 in ACMPn_CTRL register | | 250 | 520 | µA |
| $I_{ACMPREF}$ | Current consumption of internal voltage reference | Internal voltage reference off. Using external voltage reference | | 0 | | µA |
| | | Internal voltage reference | | 5 | | µA |
| $V_{ACMPOFFSET}$ | Offset voltage | BIASPROG= 0b1010, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register | -12 | 0 | 12 | mV |
| $V_{ACMPHYST}$ | ACMP hysteresis | Programmable | | 17 | | mV |
| $R_{CSRES}$ | Capacitive Sense Internal Resistance | CSRESSEL=0b00 in ACMPn_INPUTSEL | | 43 | | kOhm |
| | | CSRESSEL=0b01 in ACMPn_INPUTSEL | | 78 | | kOhm |
| | | CSRESSEL=0b10 in ACMPn_INPUTSEL | | 111 | | kOhm |
| | | CSRESSEL=0b11 in ACMPn_INPUTSEL | | 145 | | kOhm |
| $t_{ACMPSTART}$ | Startup time | | | | 10 | µs |

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 43) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

**Total ACMP Active Current**

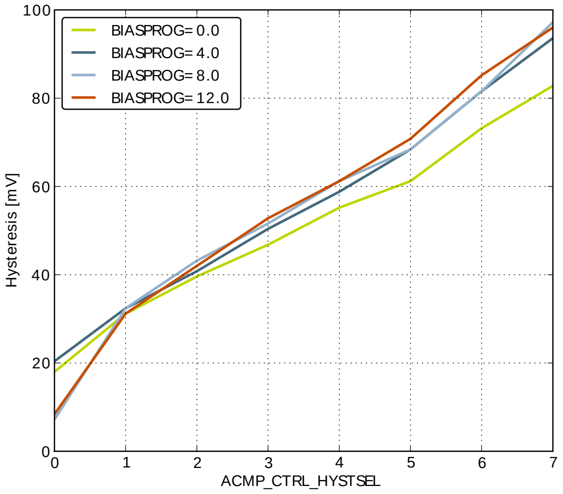
$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \qquad (3.1)$$

***Figure 3.30. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1***



Current consumption, HYSTSEL = 4

Response time



Hysteresis

## 3.14 Voltage Comparator (VCMP)

*Table 3.18. VCMP*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{VCMPIN}$ | Input voltage range | | | $V_{DD}$ | | V |
| $V_{VCMPCM}$ | VCMP Common Mode voltage range | | | $V_{DD}$ | | V |
| $I_{VCMP}$ | Active current | BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register | | 0.3 | 0.6 | µA |
| | | BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0. | | 22 | 30 | µA |
| $t_{VCMPREF}$ | Startup time reference generator | NORMAL | | 10 | | µs |
| $V_{VCMPOFFSET}$ | Offset voltage | Single ended | -230 | -40 | 190 | mV |
| | | Differential | | 10 | | mV |
| $V_{VCMPHYST}$ | VCMP hysteresis | | | 40 | | mV |
| $t_{VCMPSTART}$ | Startup time | | | | 10 | µs |

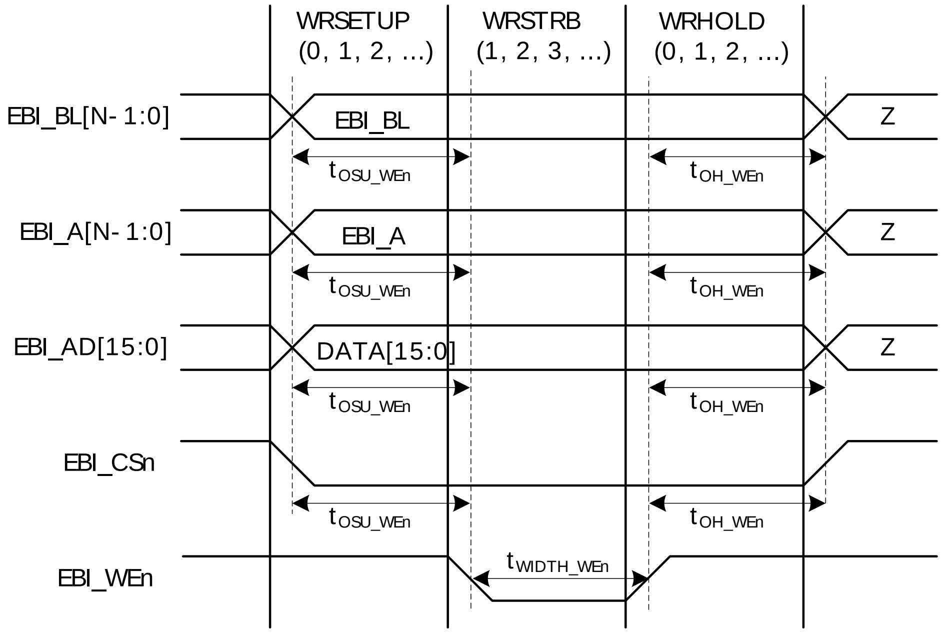
The $V_{DD}$ trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

***VCMP Trigger Level as a Function of Level Setting***

$$V_{DD\ Trigger\ Level}=1.667V+0.034\times TRIGLEVEL \qquad (3.2)$$

## 3.15 EBI

*Figure 3.31. EBI Write Enable Timing*



WRSETUP
(0, 1, 2, ...)
WRSTRB
(1, 2, 3, ...)
WRHOLD
(0, 1, 2, ...)
EBI_BL[N-1:0]
EBI_BL
Z
$t_{OSU\_WEn}$
$t_{OH\_WEn}$
EBI_A[N-1:0]
EBI_A
Z
$t_{OSU\_WEn}$
$t_{OH\_WEn}$
EBI_AD[15:0]
DATA[15:0]
Z
$t_{OSU\_WEn}$
$t_{OH\_WEn}$
EBI_CSn
$t_{OSU\_WEn}$
$t_{OH\_WEn}$
EBI_WEn
$t_{WIDTH\_WEn}$

### Table 3.19. EBI Write Enable Timing

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{OH\_WEn}$ [1,2,3,4] | Output hold time, from trailing EBI_WEn/ EBI_NANDWEn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid | -6.00 + (WRHOLD * $t_{HFCORECLK}$) | | | ns |
| $t_{OSU\_WEn}$ [1,2,3,4,5] | Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_WEn/ EBI_NANDWEn edge | -14.00 + (WRSETUP * $t_{HFCORECLK}$) | | | ns |
| $t_{WIDTH\_WEn}$ [1,2,3,4,5] | EBI_WEn/EBI_NANDWEn pulse width | -7.00 + ((WRSTRB +1) * $t_{HFCORECLK}$) | | | ns |

[1] Applies for all addressing modes (figure only shows D16 addressing mode)

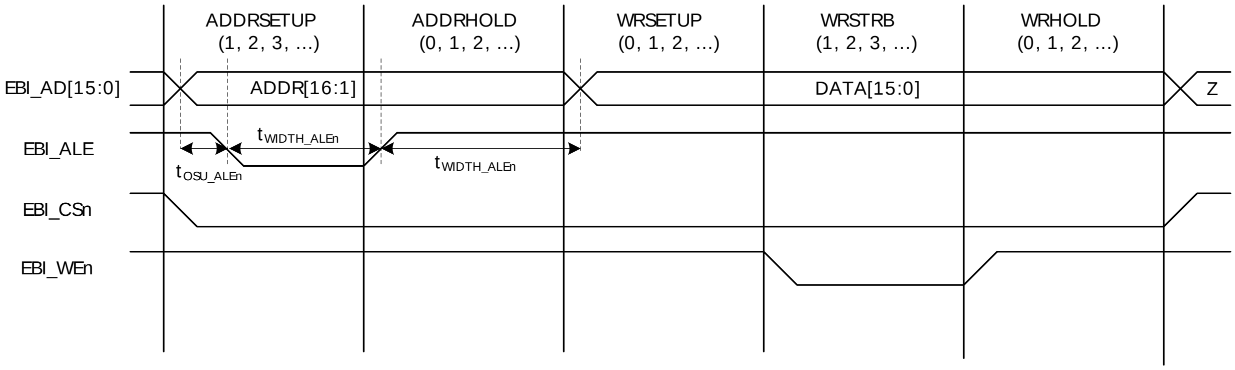
[2] Applies for both EBI_WEn and EBI_NANWEn (figure only shows EBI_WEn)

[3] Applies for all polarities (figure only shows active low signals)

[4] Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $_{VDD}$)

[5] The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFWE=0. The leading edge of EBI_WEn can be moved to the right by setting HALFWE=1. This decreases the length of $t_{WIDTH\_WEn}$ and increases the length of $t_{OSU\_WEn}$ by 1/2 * $t_{HFCLKNODIV}$.

### Figure 3.32. EBI Address Latch Enable Related Output Timing



### Table 3.20. EBI Address Latch Enable Related Output Timing

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{OH\_ALEn}$ [1,2,3,4] | Output hold time, from trailing EBI_ALE edge to EBI_AD invalid | -6.00 + (ADDRHOLD[5] * $t_{HFCORECLK}$) | | | ns |
| $t_{OSU\_ALEn}$ [1,2,4] | Output setup time, from EBI_AD valid to leading EBI_ALE edge | -13.00 + (0 * $t_{HFCORECLK}$) | | | ns |
| $t_{WIDTH\_ALEn}$ [1,2,3,4] | EBI_ALEn pulse width | -7.00 + (ADDRSETUP+1) * $t_{HFCORECLK}$) | | | ns |

[1] Applies to addressing modes D8A24ALE and D16A16ALE (figure only shows D16A16ALE)

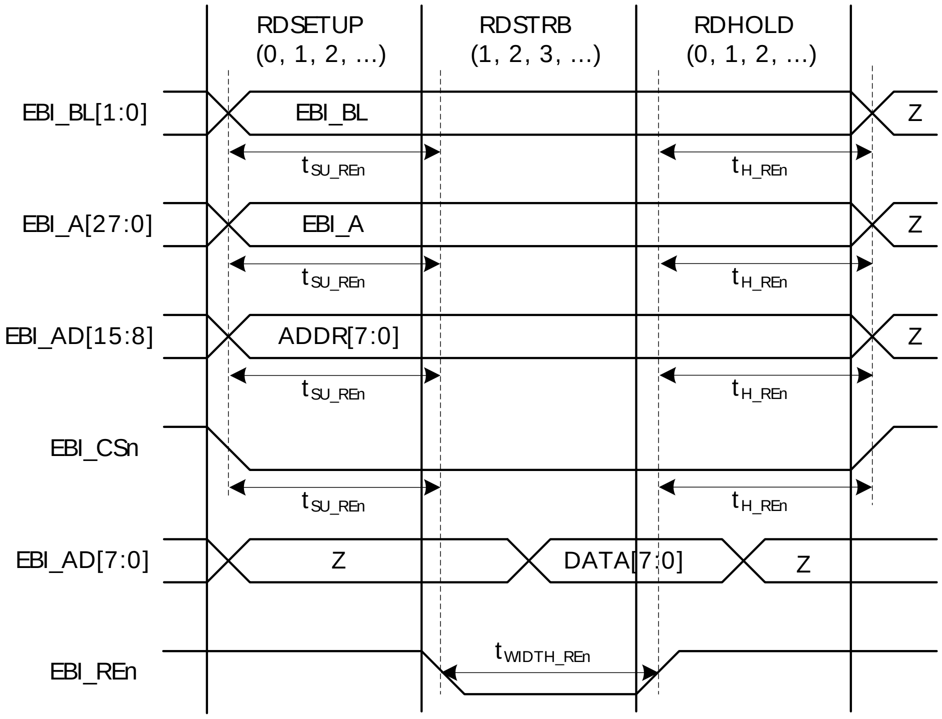
[2] Applies for all polarities (figure only shows active low signals)

[3] The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFALE=0. The trailing edge of EBI_ALE can be moved to the left by setting HALFALE=1. This decreases the length of $t_{WIDTH\_ALEn}$ and increases the length of tOH_ALEn by $t_{HFCORECLK}$ - 1/2 * $t_{HFCLKNODIV}$.

[4] Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $_{VDD}$)

[5] Figure only shows a write operation. For a multiplexed read operation the address hold time is controlled via the RDSETUP state instead of via the ADDRHOLD state.

## Figure 3.33. EBI Read Enable Related Output Timing



## Table 3.21. EBI Read Enable Related Output Timing

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{OH\_REn}$ [1 2 3 4] | Output hold time, from trailing EBI_REn/ EBI_NANDREn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid | -10.00 + (RDHOLD * $t_{HFCORECLK}$) | | | ns |
| $t_{OSU\_REn}$ [1 2 3 4 5] | Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_REn/EBI_NANDREn edge | -10.00 + (RDSETUP * $t_{HFCORECLK}$) | | | ns |
| $t_{WIDTH\_REn}$ [1 2 3 4 5 6] | EBI_REn pulse width | -9.00 + ((RDSTRB+1) * $t_{HFCORECLK}$) | | | ns |

[1] Applies for all addressing modes (figure only shows D8A8. Output timing for EBI_AD only applies to multiplexed addressing modes D8A24ALE and D16A16ALE)

[2] Applies for both EBI_REn and EBI_NANDREn (figure only shows EBI_REn)

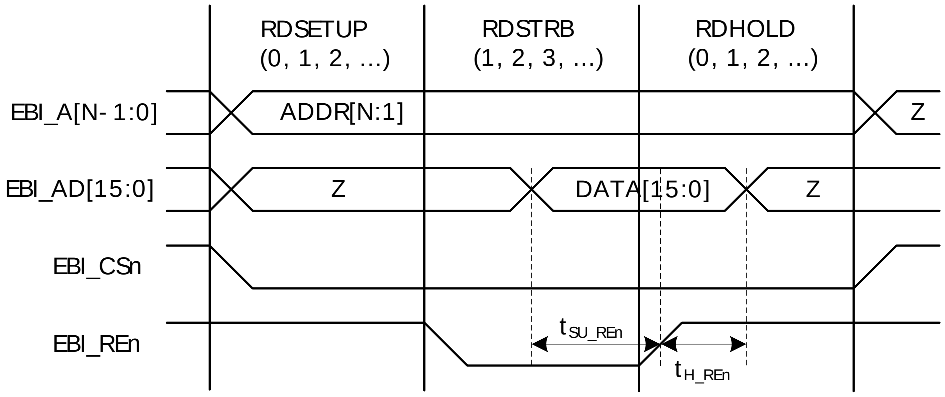
[3] Applies for all polarities (figure only shows active low signals)

[4] Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $_{VDD}$)

[5] The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFRE=0. The leading edge of EBI_REn can be moved to the right by setting HALFRE=1. This decreases the length of $t_{WIDTH\_REn}$ and increases the length of $t_{OSU\_REn}$ by 1/2 * $t_{HFCLKNODIV}$.

[6] When page mode is used, RDSTRB is replaced by RDPA for page hits.

### Figure 3.34. EBI Read Enable Related Timing Requirements


RDSETUP
(0, 1, 2, ...)
RDSTRB
(1, 2, 3, ...)
RDHOLD
(0, 1, 2, ...)
EBI_A[N-1:0]
ADDR[N:1]
Z
EBI_AD[15:0]
Z
DATA[15:0]
Z
EBI_CSn
EBI_REn
tSU_REn
tH_REn

### Table 3.22. EBI Read Enable Related Timing Requirements

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SU\_REn}$ [1 2 3 4] | Setup time, from EBI_AD valid to trailing EBI_REn edge | 37 | | | ns |
| $t_{H\_Ren}$ [1 2 3 4] | Hold time, from trailing EBI_REn edge to EBI_AD invalid | -1 | | | ns |

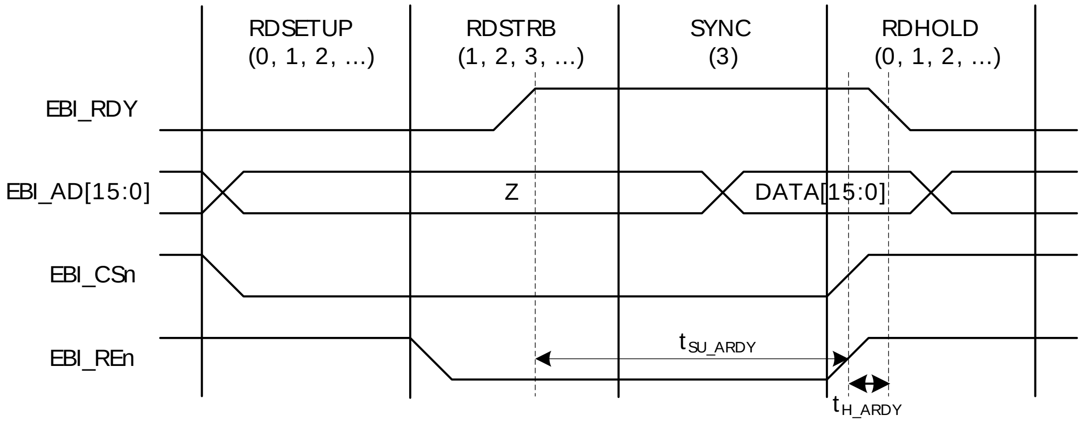
[1] Applies for all addressing modes (figure only shows D16A8).

[2] Applies for both EBI_REn and EBI_NANDREn (figure only shows EBI_REn)

[3] Applies for all polarities (figure only shows active low signals)

[4] Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $_{VDD}$)

### Figure 3.35. EBI Ready/Wait Related Timing Requirements


RDSETUP
(0, 1, 2, ...)
RDSTRB
(1, 2, 3, ...)
SYNC
(3)
RDHOLD
(0, 1, 2, ...)
EBI_RDY
EBI_AD[15:0]
Z
DATA[15:0]
EBI_CSn
EBI_REn
tSU_ARDY
tH_ARDY

### Table 3.23. EBI Ready/Wait Related Timing Requirements

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SU\_ARDY}$ [1 2 3 4] | Setup time, from EBI_ARDY valid to trailing EBI_REn, EBI_WEn edge | 37 + (3 * $t_{HFCORECLK}$) | | | ns |

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{H\_ARDY}$ [1,2,3,4] | Hold time, from trailing EBI_REn, EBI_WEn edge to EBI_ARDY invalid | -1 | | | ns |

[1] Applies for all addressing modes (figure only shows D16A8.)

[2] Applies for EBI_REn, EBI_WEn (figure only shows EBI_REn)

[3] Applies for all polarities (figure only shows active low signals)

[4] Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $_{VDD}$)

## 3.16 LCD

***Table 3.24. LCD***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LCDFR}$ | Frame rate | | 30 | | 200 | Hz |
| $NUM_{SEG}$ | Number of segments supported | | | 34×8 | | seg |
| $V_{LCD}$ | LCD supply voltage range | Internal boost circuit enabled | 2.0 | | 3.8 | V |
| $I_{LCD}$ | Steady state current consumption. | Display disconnected, static mode, framerate 32 Hz, all segments on. | | 250 | | nA |
| | | Display disconnected, quadruplex mode, framerate 32 Hz, all segments on, bias mode to ONETHIRD in LCD_DISPCTRL register. | | 550 | | nA |
| $I_{LCDBOOST}$ | Steady state Current contribution of internal boost. | Internal voltage boost off | | 0 | | µA |
| | | Internal voltage boost on, boosting from 2.2 V to 3.0 V. | | 8.4 | | µA |
| $V_{BOOST}$ | Boost Voltage | VBLEV of LCD_DISPCTRL register to LEVEL0 | | 3.02 | | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL1 | | 3.15 | | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL2 | | 3.28 | | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL3 | | 3.41 | | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL4 | | 3.54 | | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL5 | | 3.67 | | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL6 | | 3.73 | | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL7 | | 3.74 | | V |

The total LCD current is given by Equation 3.3 (p. 49) . $I_{LCDBOOST}$ is zero if internal boost is off.

***Total LCD Current Based on Operational Mode and Internal Boost***

$$I_{LCDTOTAL} = I_{LCD} + I_{LCDBOOST} \tag{3.3}$$

## 3.17 I2C

### *Table 3.25. I2C Standard-mode (Sm)*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | 0 | | 100[1] | kHz |
| $t_{LOW}$ | SCL clock low time | 4.7 | | | µs |
| $t_{HIGH}$ | SCL clock high time | 4.0 | | | µs |
| $t_{SU,DAT}$ | SDA set-up time | 250 | | | ns |
| $t_{HD,DAT}$ | SDA hold time | 8 | | 3450[2,3] | ns |
| $t_{SU,STA}$ | Repeated START condition set-up time | 4.7 | | | µs |
| $t_{HD,STA}$ | (Repeated) START condition hold time | 4.0 | | | µs |
| $t_{SU,STO}$ | STOP condition set-up time | 4.0 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 4.7 | | | µs |

[1] For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32GG Reference Manual.

[2] The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).

[3] When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*$10^{-9}$ [s] * $f_{HFPERCLK}$ [Hz]) - 4).

### *Table 3.26. I2C Fast-mode (Fm)*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | 0 | | 400[1] | kHz |
| $t_{LOW}$ | SCL clock low time | 1.3 | | | µs |
| $t_{HIGH}$ | SCL clock high time | 0.6 | | | µs |
| $t_{SU,DAT}$ | SDA set-up time | 100 | | | ns |
| $t_{HD,DAT}$ | SDA hold time | 8 | | 900[2,3] | ns |
| $t_{SU,STA}$ | Repeated START condition set-up time | 0.6 | | | µs |
| $t_{HD,STA}$ | (Repeated) START condition hold time | 0.6 | | | µs |
| $t_{SU,STO}$ | STOP condition set-up time | 0.6 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 1.3 | | | µs |

[1] For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32GG Reference Manual.

[2] The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).

[3] When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*$10^{-9}$ [s] * $f_{HFPERCLK}$ [Hz]) - 4).

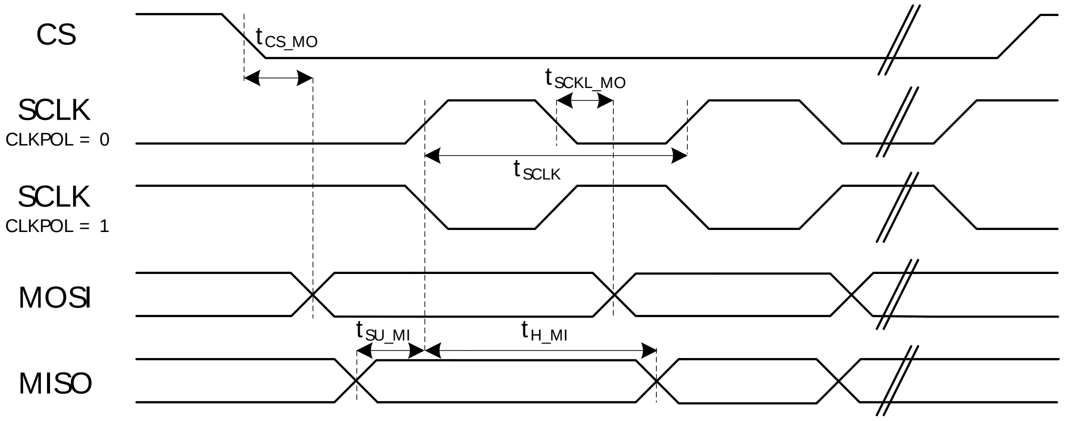
### Table 3.27. I2C Fast-mode Plus (Fm+)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | 0 | | 1000[1] | kHz |
| $t_{LOW}$ | SCL clock low time | 0.5 | | | µs |
| $t_{HIGH}$ | SCL clock high time | 0.26 | | | µs |
| $t_{SU,DAT}$ | SDA set-up time | 50 | | | ns |
| $t_{HD,DAT}$ | SDA hold time | 8 | | | ns |
| $t_{SU,STA}$ | Repeated START condition set-up time | 0.26 | | | µs |
| $t_{HD,STA}$ | (Repeated) START condition hold time | 0.26 | | | µs |
| $t_{SU,STO}$ | STOP condition set-up time | 0.26 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 0.5 | | | µs |

[1] For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32GG Reference Manual.

## 3.18 USART SPI

### Figure 3.36. SPI Master Timing



### Table 3.28. SPI Master Timing

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{SCLK}$ [1] [2] | SCLK period | | $2 * t_{HFPERCLK}$ | | | ns |
| $t_{CS\_MO}$ [1] [2] | CS to MOSI | | -2.00 | | 1.00 | ns |
| $t_{SCLK\_MO}$ [1] [2] | SCLK to MOSI | | -4.00 | | 3.00 | ns |
| $t_{SU\_MI}$ [1] [2] | MISO setup time | IOVDD = 1.98 V | 36.00 | | | ns |
| | | IOVDD = 3.0 V | 29.00 | | | ns |
| $t_{H\_MI}$ [1] [2] | MISO hold time | | -4.00 | | | ns |

[1] Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

[2] Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$)

*Figure 3.37. SPI Slave Timing*

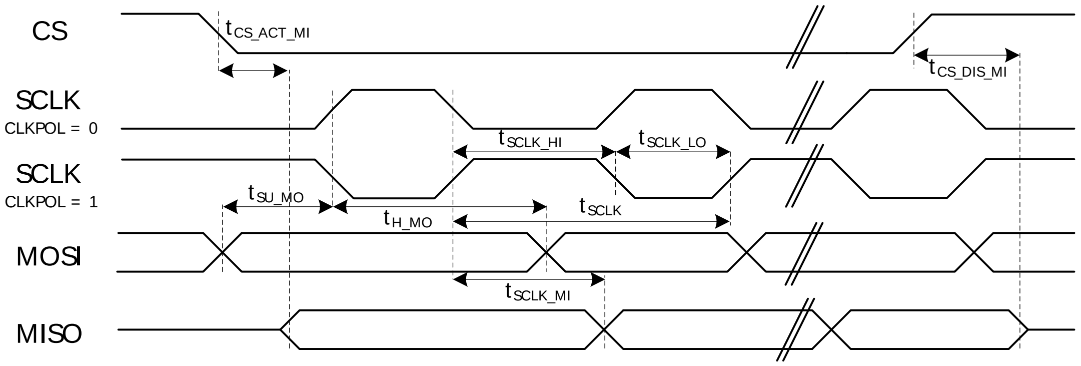


*Table 3.29. SPI Slave Timing*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SCLK\_sl}$ [1] [2] | SCKL period | 2 * $t_{HFPERCLK}$ | | | ns |
| $t_{SCLK\_hi}$ [1] [2] | SCLK high period | 3 * $t_{HFPERCLK}$ | | | ns |
| $t_{SCLK\_lo}$ [1] [2] | SCLK low period | 3 * $t_{HFPERCLK}$ | | | ns |
| $t_{CS\_ACT\_MI}$ [1] [2] | CS active to MISO | 4.00 | | 30.00 | ns |
| $t_{CS\_DIS\_MI}$ [1] [2] | CS disable to MISO | 4.00 | | 30.00 | ns |
| $t_{SU\_MO}$ [1] [2] | MOSI setup time | 4.00 | | | ns |
| $t_{H\_MO}$ [1] [2] | MOSI hold time | 2 + 2* $t_{HFPERCLK}$ | | | ns |
| $t_{SCLK\_MI}$ [1] [2] | SCLK to MISO | 9 + $t_{HFPERCLK}$ | | 36 + 2*$t_{HFPERCLK}$ | ns |

[1] Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

[2] Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$)

## 3.19 USB

The USB hardware in the EFM32GG980 passes all tests for USB 2.0 Full Speed certification. See the test-report distributed with application note "AN0046 - USB Hardware Design Guide".

## 3.20 Digital Peripherals

*Table 3.30. Digital Peripherals*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{USART}$ | USART current | USART idle current, clock enabled | | 4.9 | | µA/MHz |
| $I_{UART}$ | UART current | UART idle current, clock enabled | | 3.4 | | µA/MHz |
| $I_{LEUART}$ | LEUART current | LEUART idle current, clock enabled | | 140 | | nA |
| $I_{I2C}$ | I2C current | I2C idle current, clock enabled | | 6.1 | | µA/MHz |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{TIMER}$ | TIMER current | TIMER_0 idle current, clock enabled | | 6.9 | | µA/ MHz |
| $I_{LETIMER}$ | LETIMER current | LETIMER idle current, clock enabled | | 119 | | nA |
| $I_{PCNT}$ | PCNT current | PCNT idle current, clock enabled | | 54 | | nA |
| $I_{RTC}$ | RTC current | RTC idle current, clock enabled | | 54 | | nA |
| $I_{LCD}$ | LCD current | LCD idle current, clock enabled | | 68 | | nA |
| $I_{AES}$ | AES current | AES idle current, clock enabled | | 3.2 | | µA/ MHz |
| $I_{GPIO}$ | GPIO current | GPIO idle current, clock enabled | | 3.7 | | µA/ MHz |
| $I_{EBI}$ | EBI current | EBI idle current, clock enabled | | 11.8 | | µA/ MHz |
| $I_{PRS}$ | PRS current | PRS idle current | | 3.5 | | µA/ MHz |
| $I_{DMA}$ | DMA current | Clock enable | | 11.0 | | µA/ MHz |

# 4 Pinout and Package

**Note**

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32GG980.

## 4.1 Pinout

The *EFM32GG980* pinout is shown in Figure 4.1 (p. 54) and Table 4.1 (p. 54). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

*Figure 4.1. EFM32GG980 Pinout (top view, not to scale)*

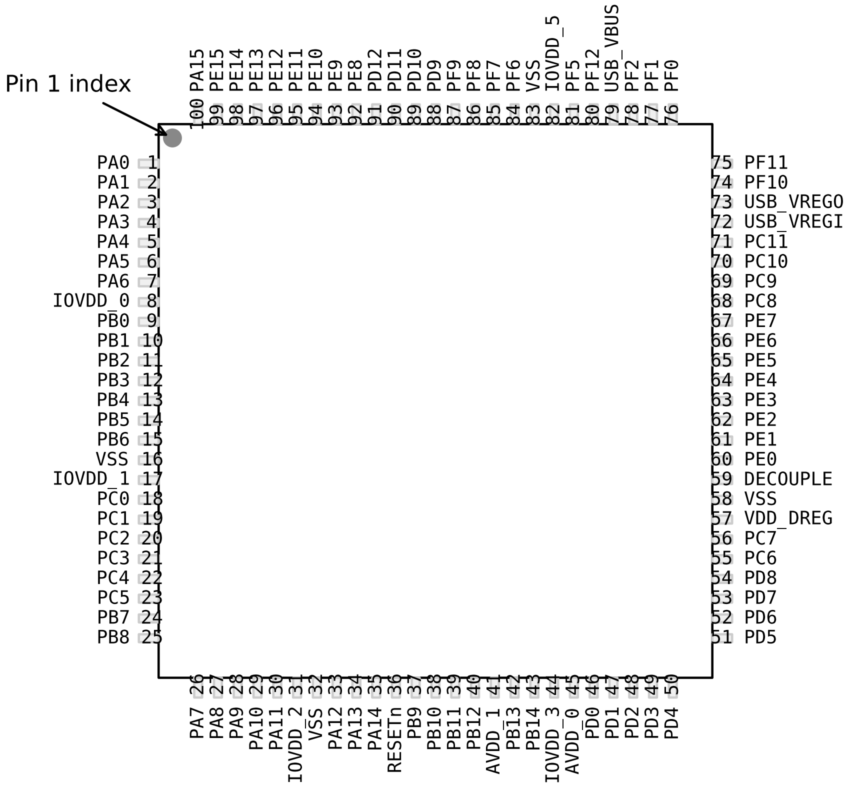

Pin 1 index
100 PA15
99 PE15
98 PE14
97 PE13
96 PE12
95 PE11
94 PE10
93 PE9
92 PE8
91 PD12
90 PD11
89 PD10
88 PD9
87 PF9
86 PF8
85 PF7
84 PF6
83 VSS
82 IOVDD_5
81 PF5
80 PF12
79 USB_VBUS
78 PF2
77 PF1
76 PF0
PA0 1
PA1 2
PA2 3
PA3 4
PA4 5
PA5 6
PA6 7
IOVDD_0 8
PB0 9
PB1 10
PB2 11
PB3 12
PB4 13
PB5 14
PB6 15
VSS 16
IOVDD_1 17
PC0 18
PC1 19
PC2 20
PC3 21
PC4 22
PC5 23
PB7 24
PB8 25
PA7 26
PA8 27
PA9 28
PA10 29
PA11 30
IOVDD_2 31
VSS 32
PA12 33
PA13 34
PA14 35
RESETn 36
PB9 37
PB10 38
PB11 39
PB12 40
AVDD_1 41
PB13 42
PB14 43
IOVDD_3 44
AVDD_0 45
PD0 46
PD1 47
PD2 48
PD3 49
PD4 50
75 PF11
74 PF10
73 USB_VREGO
72 USB_VREGI
71 PC11
70 PC10
69 PC9
68 PC8
67 PE7
66 PE6
65 PE5
64 PE4
63 PE3
62 PE2
61 PE1
60 PE0
59 DECOUPLE
58 VSS
57 VDD_DREG
56 PC7
55 PC6
54 PD8
53 PD7
52 PD6
51 PD5

*Table 4.1. Device Pinout*

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 1 | PA0 | LCD_SEG13 | EBI_AD09 #0/1/2 | TIM0_CC0 #0/1/4 | I2C0_SDA #0<br>LEU0_RX #4 | PRS_CH0 #0<br>GPIO_EM4WU0 |
| 2 | PA1 | LCD_SEG14 | EBI_AD10 #0/1/2 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |
| 3 | PA2 | LCD_SEG15 | EBI_AD11 #0/1/2 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| | | | | | | ETM_TD0 #3 |
| 4 | PA3 | LCD_SEG16 | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0<br>ETM_TD1 #3 |
| 5 | PA4 | LCD_SEG17 | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0<br>ETM_TD2 #3 |
| 6 | PA5 | LCD_SEG18 | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0<br>ETM_TD3 #3 |
| 7 | PA6 | LCD_SEG19 | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3<br>GPIO_EM4WU1 |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | | |
| 9 | PB0 | LCD_SEG32 | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| 10 | PB1 | LCD_SEG33 | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |
| 11 | PB2 | LCD_SEG34 | EBI_A18 #0/1/2 | TIM1_CC2 #2 | | |
| 12 | PB3 | LCD_SEG20/ LCD_COM4 | EBI_A19 #0/1/2 | PCNT1_S0IN #1 | US2_TX #1 | |
| 13 | PB4 | LCD_SEG21/ LCD_COM5 | EBI_A20 #0/1/2 | PCNT1_S1IN #1 | US2_RX #1 | |
| 14 | PB5 | LCD_SEG22/ LCD_COM6 | EBI_A21 #0/1/2 | | US2_CLK #1 | |
| 15 | PB6 | LCD_SEG23/ LCD_COM7 | EBI_A22 #0/1/2 | | US2_CS #1 | |
| 16 | VSS | Ground. | | | | |
| 17 | IOVDD_1 | Digital IO power supply 1. | | | | |
| 18 | PC0 | ACMP0_CH0<br>DAC0_OUT0ALT #0/<br>OPAMP_OUT0ALT | EBI_A23 #0/1/2 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5<br>US1_TX #0<br>I2C0_SDA #4 | LES_CH0 #0<br>PRS_CH2 #0 |
| 19 | PC1 | ACMP0_CH1<br>DAC0_OUT0ALT #1/<br>OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5<br>US1_RX #0<br>I2C0_SCL #4 | LES_CH1 #0<br>PRS_CH3 #0 |
| 20 | PC2 | ACMP0_CH2<br>DAC0_OUT0ALT #2/<br>OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| 21 | PC3 | ACMP0_CH3<br>DAC0_OUT0ALT #3/<br>OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| 22 | PC4 | ACMP0_CH4<br>OPAMP_P0 | EBI_A26 #0/1/2 | TIM0_CDTI2 #4<br>LETIM0_OUT0 #3<br>PCNT1_S0IN #0 | US2_CLK #0<br>I2C1_SDA #0 | LES_CH4 #0 |
| 23 | PC5 | ACMP0_CH5<br>OPAMP_N0 | EBI_NANDWEn #0/1/2 | LETIM0_OUT1 #3<br>PCNT1_S1IN #0 | US2_CS #0<br>I2C1_SCL #0 | LES_CH5 #0 |
| 24 | PB7 | LFXTAL_P | | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| 25 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| 26 | PA7 | LCD_SEG35 | EBI_CSTFT #0/1/2 | | | |
| 27 | PA8 | LCD_SEG36 | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| 28 | PA9 | LCD_SEG37 | EBI_DTEN #0/1/2 | TIM2_CC1 #0 | | |
| 29 | PA10 | LCD_SEG38 | EBI_VSNC #0/1/2 | TIM2_CC2 #0 | | |
| 30 | PA11 | LCD_SEG39 | EBI_HSNC #0/1/2 | | | |
| 31 | IOVDD_2 | Digital IO power supply 2. | | | | |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 32 | VSS | Ground. | | | | |
| 33 | PA12 | LCD_BCAP_P | EBI_A00 #0/1/2 | TIM2_CC0 #1 | | |
| 34 | PA13 | LCD_BCAP_N | EBI_A01 #0/1/2 | TIM2_CC1 #1 | | |
| 35 | PA14 | LCD_BEXT | EBI_A02 #0/1/2 | TIM2_CC2 #1 | | |
| 36 | RESETn | Reset input, active low.<br>To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| 37 | PB9 | | EBI_A03 #0/1/2 | | U1_TX #2 | |
| 38 | PB10 | | EBI_A04 #0/1/2 | | U1_RX #2 | |
| 39 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | | LETIM0_OUT0 #1<br>TIM1_CC2 #3 | I2C1_SDA #1 | |
| 40 | PB12 | DAC0_OUT1 / OPAMP_OUT1 | | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| 41 | AVDD_1 | Analog power supply 1. | | | | |
| 42 | PB13 | HFXTAL_P | | | US0_CLK #4/5<br>LEU0_TX #1 | |
| 43 | PB14 | HFXTAL_N | | | US0_CS #4/5<br>LEU0_RX #1 | |
| 44 | IOVDD_3 | Digital IO power supply 3. | | | | |
| 45 | AVDD_0 | Analog power supply 0. | | | | |
| 46 | PD0 | ADC0_CH0<br>DAC0_OUT0ALT #4/<br>OPAMP_OUT0ALT<br>OPAMP_OUT2 #1 | | PCNT2_S0IN #0 | US1_TX #1 | |
| 47 | PD1 | ADC0_CH1<br>DAC0_OUT1ALT #4/<br>OPAMP_OUT1ALT | | TIM0_CC0 #3<br>PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| 48 | PD2 | ADC0_CH2 | EBI_A27 #0/1/2 | TIM0_CC1 #3 | USB_DMPU #0<br>US1_CLK #1 | DBG_SWO #3 |
| 49 | PD3 | ADC0_CH3<br>OPAMP_N2 | | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| 50 | PD4 | ADC0_CH4<br>OPAMP_P2 | | | LEU0_TX #0 | ETM_TD2 #0/2 |
| 51 | PD5 | ADC0_CH5<br>OPAMP_OUT2 #0 | | | LEU0_RX #0 | ETM_TD3 #0/2 |
| 52 | PD6 | ADC0_CH6<br>OPAMP_P1 | | LETIM0_OUT0 #0<br>TIM1_CC0 #4<br>PCNT0_S0IN #3 | US1_RX #2<br>I2C0_SDA #1 | LES_ALTEX0 #0<br>ACMP0_O #2<br>ETM_TD0 #0 |
| 53 | PD7 | ADC0_CH7<br>OPAMP_N1 | | LETIM0_OUT1 #0<br>TIM1_CC1 #4<br>PCNT0_S1IN #3 | US1_TX #2<br>I2C0_SCL #1 | CMU_CLK0 #2<br>LES_ALTEX1 #0<br>ACMP1_O #2<br>ETM_TCLK #0 |
| 54 | PD8 | BU_VIN | | | | CMU_CLK1 #1 |
| 55 | PC6 | ACMP0_CH6 | EBI_A05 #0/1/2 | | I2C0_SDA #2<br>LEU1_TX #0 | LES_CH6 #0<br>ETM_TCLK #2 |
| 56 | PC7 | ACMP0_CH7 | EBI_A06 #0/1/2 | | I2C0_SCL #2<br>LEU1_RX #0 | LES_CH7 #0<br>ETM_TD0 #2 |
| 57 | VDD_DREG | Power supply for on-chip voltage regulator. | | | | |
| 58 | VSS | Ground. | | | | |
| 59 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | | |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 60 | PE0 | | EBI_A07 #0/1/2 | TIM3_CC0 #1<br>PCNT0_S0IN #1 | U0_TX #1<br>I2C1_SDA #2 | |
| 61 | PE1 | | EBI_A08 #0/1/2 | TIM3_CC1 #1<br>PCNT0_S1IN #1 | U0_RX #1<br>I2C1_SCL #2 | |
| 62 | PE2 | BU_VOUT | EBI_A09 #0 | TIM3_CC2 #1 | U1_TX #3 | ACMP0_O #1 |
| 63 | PE3 | BU_STAT | EBI_A10 #0 | | U1_RX #3 | ACMP1_O #1 |
| 64 | PE4 | LCD_COM0 | EBI_A11 #0/1/2 | | US0_CS #1 | |
| 65 | PE5 | LCD_COM1 | EBI_A12 #0/1/2 | | US0_CLK #1 | |
| 66 | PE6 | LCD_COM2 | EBI_A13 #0/1/2 | | US0_RX #1 | |
| 67 | PE7 | LCD_COM3 | EBI_A14 #0/1/2 | | US0_TX #1 | |
| 68 | PC8 | ACMP1_CH0 | EBI_A15 #0/1/2 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| 69 | PC9 | ACMP1_CH1 | EBI_A09 #1/2 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0<br>GPIO_EM4WU2 |
| 70 | PC10 | ACMP1_CH2 | EBI_A10 #1/2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| 71 | PC11 | ACMP1_CH3 | EBI_ALE #1/2 | | US0_TX #2 | LES_CH11 #0 |
| 72 | USB_VREGI | | | | | |
| 73 | USB_VREGO | | | | | |
| 74 | PF10 | | | | U1_TX #1<br>USB_DM | |
| 75 | PF11 | | | | U1_RX #1<br>USB_DP | |
| 76 | PF0 | | | TIM0_CC0 #5<br>LETIM0_OUT0 #2 | US1_CLK #2<br>I2C0_SDA #5<br>LEU0_TX #3 | DBG_SWCLK #0/1/2/3 |
| 77 | PF1 | | | TIM0_CC1 #5<br>LETIM0_OUT1 #2 | US1_CS #2<br>I2C0_SCL #5<br>LEU0_RX #3 | DBG_SWDIO #0/1/2/3<br>GPIO_EM4WU3 |
| 78 | PF2 | LCD_SEG0 | EBI_ARDY #0/1/2 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0<br>DBG_SWO #0<br>GPIO_EM4WU4 |
| 79 | USB_VBUS | USB 5.0 V VBUS input. | | | | |
| 80 | PF12 | | | | USB_ID | |
| 81 | PF5 | LCD_SEG3 | EBI_REn #0/2 | TIM0_CDTI2 #2/5 | USB_VBUSEN #0 | PRS_CH2 #1 |
| 82 | IOVDD_5 | Digital IO power supply 5. | | | | |
| 83 | VSS | Ground. | | | | |
| 84 | PF6 | LCD_SEG24 | EBI_BL0 #0/1/2 | TIM0_CC0 #2 | U0_TX #0 | |
| 85 | PF7 | LCD_SEG25 | EBI_BL1 #0/1/2 | TIM0_CC1 #2 | U0_RX #0 | |
| 86 | PF8 | LCD_SEG26 | EBI_WEn #1 | TIM0_CC2 #2 | | ETM_TCLK #1 |
| 87 | PF9 | LCD_SEG27 | EBI_REn #1 | | | ETM_TD0 #1 |
| 88 | PD9 | LCD_SEG28 | EBI_CS0 #0/1/2 | | | |
| 89 | PD10 | LCD_SEG29 | EBI_CS1 #0/1/2 | | | |
| 90 | PD11 | LCD_SEG30 | EBI_CS2 #0/1/2 | | | |
| 91 | PD12 | LCD_SEG31 | EBI_CS3 #0/1/2 | | | |
| 92 | PE8 | LCD_SEG4 | EBI_AD00 #0/1/2 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| 93 | PE9 | LCD_SEG5 | EBI_AD01 #0/1/2 | PCNT2_S1IN #1 | | |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 94 | PE10 | LCD_SEG6 | EBI_AD02 #0/1/2 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 95 | PE11 | LCD_SEG7 | EBI_AD03 #0/1/2 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0<br>BOOT_RX |
| 96 | PE12 | LCD_SEG8 | EBI_AD04 #0/1/2 | TIM1_CC2 #1 | US0_RX #3<br>US0_CLK #0<br>I2C0_SDA #6 | CMU_CLK1 #2<br>LES_ALTEX6 #0 |
| 97 | PE13 | LCD_SEG9 | EBI_AD05 #0/1/2 | | US0_TX #3<br>US0_CS #0<br>I2C0_SCL #6 | LES_ALTEX7 #0<br>ACMP0_O #0<br>GPIO_EM4WU5 |
| 98 | PE14 | LCD_SEG10 | EBI_AD06 #0/1/2 | TIM3_CC0 #0 | LEU0_TX #2 | |
| 99 | PE15 | LCD_SEG11 | EBI_AD07 #0/1/2 | TIM3_CC1 #0 | LEU0_RX #2 | |
| 100 | PA15 | LCD_SEG12 | EBI_AD08 #0/1/2 | TIM3_CC2 #0 | | |

## 4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 58). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note**

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

*Table 4.2. Alternate functionality overview*

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 / OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | | | | | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |
| EBI_A04 | PB10 | PB10 | PB10 | | | | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | PC6 | PC6 | PC6 | | | | | External Bus Interface (EBI) address output pin 05. |
| EBI_A06 | PC7 | PC7 | PC7 | | | | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | PE0 | PE0 | PE0 | | | | | External Bus Interface (EBI) address output pin 07. |
| EBI_A08 | PE1 | PE1 | PE1 | | | | | External Bus Interface (EBI) address output pin 08. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_A09 | PE2 | PC9 | PC9 | | | | | External Bus Interface (EBI) address output pin 09. |
| EBI_A10 | PE3 | PC10 | PC10 | | | | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | PE4 | PE4 | PE4 | | | | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | PE5 | PE5 | PE5 | | | | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | PE6 | PE6 | PE6 | | | | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | PE7 | PE7 | PE7 | | | | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | PC8 | PC8 | PC8 | | | | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | PB0 | PB0 | PB0 | | | | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | PB1 | PB1 | PB1 | | | | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | PB2 | PB2 | PB2 | | | | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | PB3 | PB3 | PB3 | | | | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | PB4 | PB4 | PB4 | | | | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | PB5 | PB5 | PB5 | | | | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | PB6 | PB6 | PB6 | | | | | External Bus Interface (EBI) address output pin 22. |
| EBI_A23 | PC0 | PC0 | PC0 | | | | | External Bus Interface (EBI) address output pin 23. |
| EBI_A24 | PC1 | PC1 | PC1 | | | | | External Bus Interface (EBI) address output pin 24. |
| EBI_A25 | PC2 | PC2 | PC2 | | | | | External Bus Interface (EBI) address output pin 25. |
| EBI_A26 | PC4 | PC4 | PC4 | | | | | External Bus Interface (EBI) address output pin 26. |
| EBI_A27 | PD2 | PD2 | PD2 | | | | | External Bus Interface (EBI) address output pin 27. |
| EBI_AD00 | PE8 | PE8 | PE8 | | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | PE9 | PE9 | | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | PE10 | PE10 | | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | PE11 | PE11 | | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | PE12 | PE12 | | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | PE13 | PE13 | | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | PE14 | PE14 | | | | | External Bus Interface (EBI) address and data input / output pin 06. |
| EBI_AD07 | PE15 | PE15 | PE15 | | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | PA15 | PA15 | | | | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | PA0 | PA0 | PA0 | | | | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | PA1 | PA1 | PA1 | | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | PA2 | PA2 | | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | PA3 | PA3 | | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | PA4 | PA4 | | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | PA5 | PA5 | | | | | External Bus Interface (EBI) address and data input / output pin 14. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_AD15 | PA6 | PA6 | PA6 | | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | | PC11 | PC11 | | | | | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | PF2 | PF2 | PF2 | | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | PF6 | PF6 | PF6 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | PF7 | PF7 | PF7 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | PD9 | PD9 | PD9 | | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | PD10 | PD10 | | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | PD11 | PD11 | | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | PD12 | PD12 | | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | PA7 | PA7 | PA7 | | | | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | PA8 | PA8 | PA8 | | | | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | PA9 | PA9 | PA9 | | | | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | PA11 | PA11 | PA11 | | | | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | PC3 | PC3 | PC3 | | | | | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | PC5 | PC5 | PC5 | | | | | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |
| EBI_WEn | | PF8 | | | | | | External Bus Interface (EBI) Write Enable output. |
| ETM_TCLK | PD7 | PF8 | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | PF9 | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | PE1 | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | PE0 | | | | | I2C1 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_BEXT | PA14 | | | | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.<br>An external LCD voltage may also be applied to this pin if the booster is not enabled.<br>If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG12 | PA15 | | | | | | | LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG13 | PA0 | | | | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG18 | PA5 | | | | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG19 | PA6 | | | | | | | LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20/ LCD_COM4 | PB3 | | | | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4 |
| LCD_SEG21/ LCD_COM5 | PB4 | | | | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5 |
| LCD_SEG22/ LCD_COM6 | PB5 | | | | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6 |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_SEG23/<br>LCD_COM7 | PB6 | | | | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7 |
| LCD_SEG24 | PF6 | | | | | | | LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG25 | PF7 | | | | | | | LCD segment line 25. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG26 | PF8 | | | | | | | LCD segment line 26. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG27 | PF9 | | | | | | | LCD segment line 27. Segments 24, 25, 26 and 27 are controlled by SEGEN6. |
| LCD_SEG28 | PD9 | | | | | | | LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG29 | PD10 | | | | | | | LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG30 | PD11 | | | | | | | LCD segment line 30. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG31 | PD12 | | | | | | | LCD segment line 31. Segments 28, 29, 30 and 31 are controlled by SEGEN7. |
| LCD_SEG32 | PB0 | | | | | | | LCD segment line 32. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG33 | PB1 | | | | | | | LCD segment line 33. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG34 | PB2 | | | | | | | LCD segment line 34. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG35 | PA7 | | | | | | | LCD segment line 35. Segments 32, 33, 34 and 35 are controlled by SEGEN8. |
| LCD_SEG36 | PA8 | | | | | | | LCD segment line 36. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG37 | PA9 | | | | | | | LCD segment line 37. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG38 | PA10 | | | | | | | LCD segment line 38. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LCD_SEG39 | PA11 | | | | | | | LCD segment line 39. Segments 36, 37, 38 and 39 are controlled by SEGEN9. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | PE0 | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | | PE1 | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | | | | PC2 | | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | | | | PC3 | | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | | PF5 | | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | | PE10 | PB0 | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | | PE11 | PB1 | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | | PE12 | PB2 | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | PA13 | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | PE0 | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | PE1 | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | | | | | UART0 Receive input. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| U0_TX | PF6 | PE0 | PA3 | | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_RX | | PF11 | PB10 | PE3 | | | | UART1 Receive input. |
| U1_TX | | PF10 | PB9 | PE2 | | | | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | PF10 | | | | | | | USB D- pin. |
| USB_DMPU | PD2 | | | | | | | USB D- Pullup control. |
| USB_DP | PF11 | | | | | | | USB D+ pin. |
| USB_ID | PF12 | | | | | | | USB ID pin. Used in OTG mode. |
| USB_VBUS | USB_VBUS | | | | | | | USB 5 V VBUS input. |
| USB_VBUSEN | PF5 | | | | | | | USB 5 V VBUS enable. |
| USB_VREGI | USB_VREGI | | | | | | | USB Input to internal 3.3 V regulator |
| USB_VREGO | USB_VREGO | | | | | | | USB Decoupling for internal 3.3 V USB regulator and regulator output |

## 4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32GG980* is shown in Table 4.3 (p. 66). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

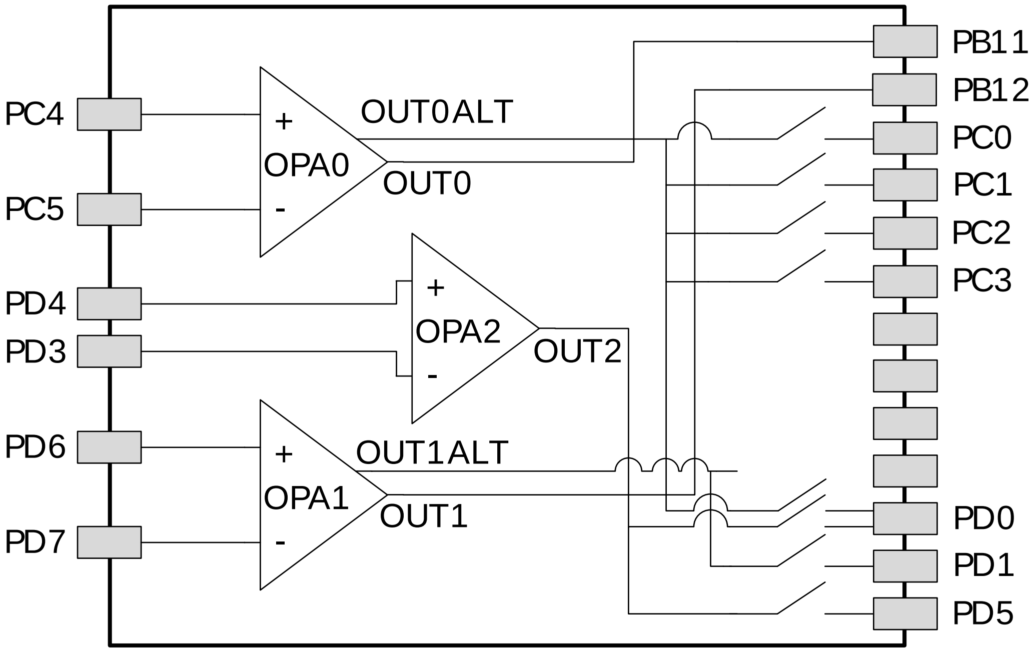
**Table 4.3. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | - | - | - | - | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | - | - | - | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | - | - | - | PF12 | PF11 | PF10 | PF9 | PF8 | PF7 | PF6 | PF5 | - | - | PF2 | PF1 | PF0 |

## 4.4 Opamp Pinout Overview

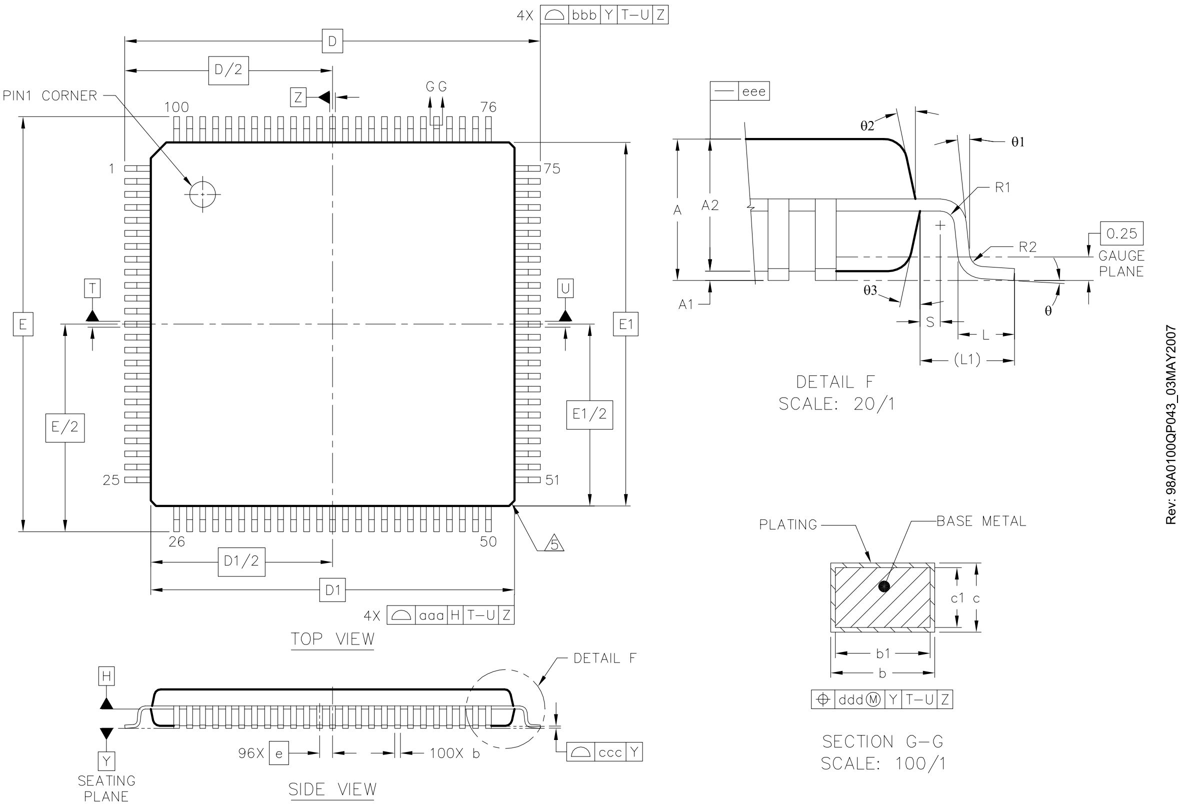
The specific opamp terminals available in *EFM32GG980* is shown in Figure 4.2 (p. 66) .

**Figure 4.2. Opamp Pinout**


PB11
PB12
PC0
PC1
PC2
PC3
PD0
PD1
PD5
PC4
PC5
PD4
PD3
PD6
PD7
OPA0
OUT0ALT
OUT0
OPA2
OUT2
OPA1
OUT1ALT
OUT1
+
-

## 4.5 LQFP100 Package

*Figure 4.3. LQFP100*


4X bbb Y T–U Z
D
D/2
PIN1 CORNER
100
Z
G G
76
1
75
T
U
E
E1
E/2
E1/2
25
51
26
50
5
D1/2
D1
4X aaa H T–U Z
TOP VIEW
eee
θ2
θ1
A
A2
R1
R2
0.25
GAUGE PLANE
A1
θ3
θ
S
L
(L1)
DETAIL F
SCALE: 20/1
Rev: 98A0100QP043_03MAY2007
PLATING
BASE METAL
c1
c
b1
b
ddd M Y T–U Z
SECTION G–G
SCALE: 100/1
H
DETAIL F
Y
SEATING PLANE
96X e
100X b
ccc Y
SIDE VIEW

Note:

1. Datum 'T', 'U' and 'Z' to be determined at datum plane 'H'.
2. Datum 'D' and 'E' to be determined at seating plane datum 'Y'.
3. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25 per side. Dimensions 'D1' and 'E1' do include mold mismatch and are determined at datum plane datum 'H'.
4. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm
5. Exact shape of each corner is optional.

### Table 4.4. LQFP100 (Dimensions in mm)

| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| total thickness | | A | -- | -- | 1.6 |
| stand off | | A1 | 0.05 | -- | 0.15 |
| mold thickness | | A2 | 1.35 | 1.4 | 1.45 |
| lead width (plating) | | b | 0.17 | 0.2 | 0.27 |
| lead width | | b1 | 0.17 | -- | 0.23 |
| L/F thickness (plating) | | c | 0.09 | -- | 0.2 |
| lead thickness | | c1 | 0.09 | -- | 0.16 |
| | x | D | 16 BSC | | |
| | y | E | 16 BSC | | |
| body size | x | D1 | 14 BSC | | |
| | y | E1 | 14 BSC | | |
| lead pitch | | e | 0.5 BSC | | |
| | | L | 0.45 | 0.6 | 0.75 |
| footprint | | L1 | 1 REF | | |
| | | θ | 0° | 3.5° | 7° |
| | | θ1 | 0° | -- | -- |
| | | θ2 | 11° | 12° | 13° |
| | | θ3 | 11° | 12° | 13° |
| | | R1 | 0.08 | -- | -- |
| | | R1 | 0.08 | -- | 0.2 |
| | | S | 0.2 | -- | -- |
| package edge tolerance | | aaa | 0.2 | | |
| lead edge tolerance | | bbb | 0.2 | | |
| coplanarity | | ccc | 0.08 | | |
| lead offset | | ddd | 0.08 | | |
| mold flatness | | eee | 0.05 | | |

The LQFP100 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see:
http://www.silabs.com/support/quality/pages/default.aspx

# 5 PCB Layout and Soldering

## 5.1 Recommended PCB Layout

*Figure 5.1. LQFP100 PCB Land Pattern*

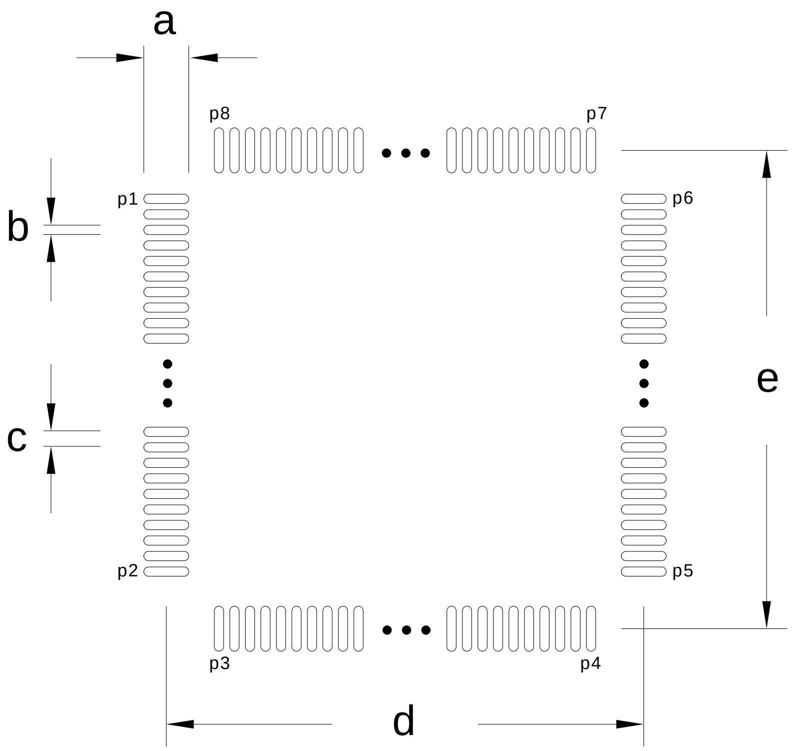


*Table 5.1. QFP100 PCB Land Pattern Dimensions (Dimensions in mm)*

| Symbol | Dim. (mm) | Symbol | Pin number | Symbol | Pin number |
|---|---|---|---|---|---|
| a | 1.45 | P1 | 1 | P6 | 75 |
| b | 0.30 | P2 | 25 | P7 | 76 |
| c | 0.50 | P3 | 26 | P8 | 100 |
| d | 15.40 | P4 | 50 | - | - |
| e | 15.40 | P5 | 51 | - | - |

Figure 5.2. LQFP100 PCB Solder Mask

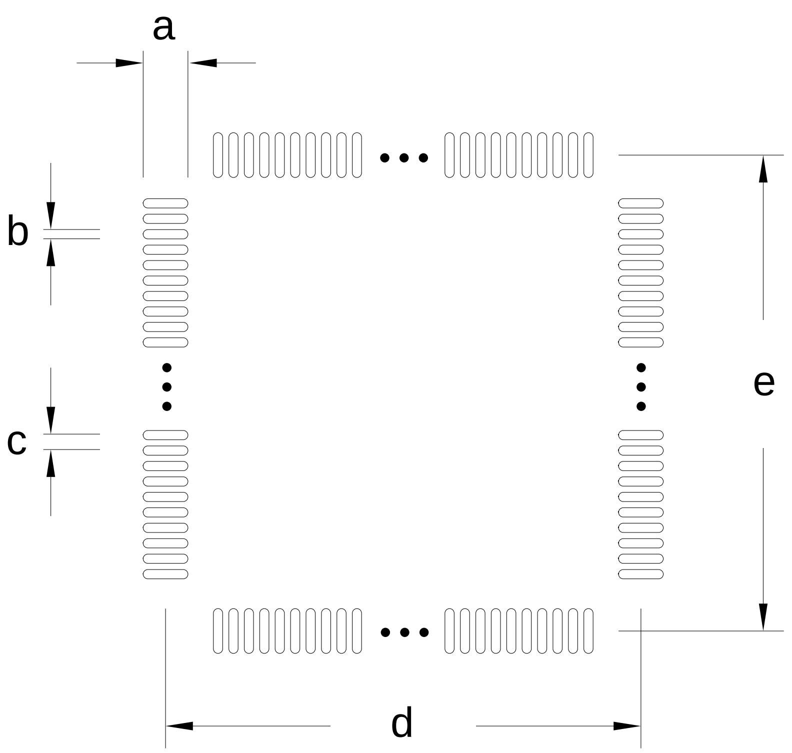


Table 5.2. QFP100 PCB Solder Mask Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|---|---|
| a | 1.57 |
| b | 0.42 |
| c | 0.50 |
| d | 15.40 |
| e | 15.40 |

*Figure 5.3. LQFP100 PCB Stencil Design*

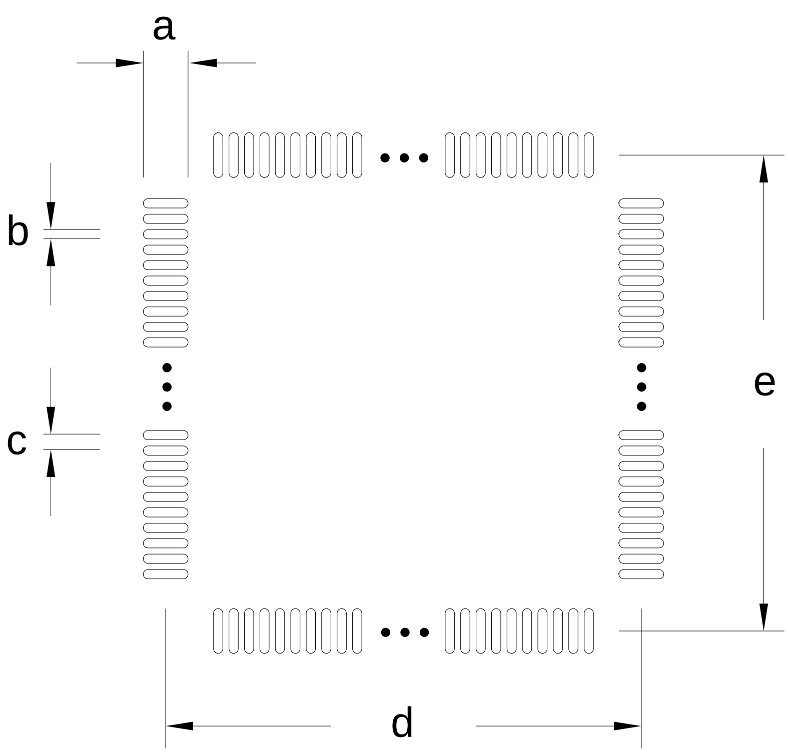


*Table 5.3. QFP100 PCB Stencil Design Dimensions (Dimensions in mm)*

| Symbol | Dim. (mm) |
|---|---|
| a | 1.35 |
| b | 0.20 |
| c | 0.50 |
| d | 15.40 |
| e | 15.40 |

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.3 (p. 67) .

## 5.2 Soldering Information

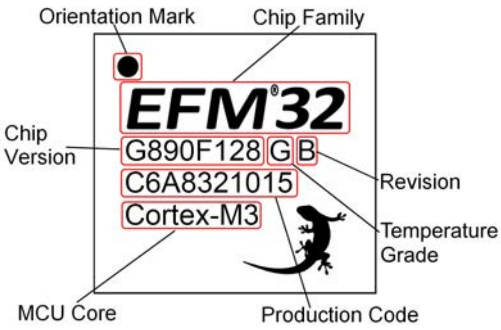
The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

# 6 Chip Marking, Revision and Errata

## 6.1 Chip Marking

In the illustration below package fields and position are shown.

***Figure 6.1. Example Chip Marking (top view)***


Orientation Mark
Chip Family
Chip Version
EFM32
G890F128
G
B
C6A8321015
Cortex-M3
Revision
Temperature Grade
MCU Core
Production Code

## 6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 72) .

## 6.3 Errata

Please see the errata document for EFM32GG980 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:
http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

# 7 Revision History

## 7.1 Revision 1.40

March 21st, 2016

Added clarification on conditions for $INL_{ADC}$ and $DNL_{ADC}$ parameters.

Reduced maximum and typical current consumption for all EM0 entries except 48 MHz in the Current Consumption table in the Electrical Characteristics section.

Increased maximum specifications for EM2 current, EM3 current, and EM4 current in the Current Consumption table in the Electrical Characteristics section.

Increased typical specification for EM2 and EM3 current at 85 C in the Current Consumption table in the Electrical Characteristics section.

Added EM2, EM3, and EM4 current consumption vs. temperature graphs.

Added a new EM2 entry and specified the existing specification is for EM0 for the BOD threshold on falling external supply voltage in the Power Management table in the Electrical Characteristics section.

Reduced maximum input leakage current in the GPIO table in the Electrical Characteristics section.

Added a maximum current consumption specification to the LFRCO table in the Electrical Characteristics section.

Added maximum specifications for the active current including references for two channels to the DAC table in the Electrical Characteristics section.

Increased the maximum specification for DAC offset voltage in the DAC table in the Electrical Characteristics section.

Increased the typical specifications for active current with FULLBIAS=1 and capacitive sense internal resistance in the ACMP table in the Electrical Characteristics section.

Added minimum and maximum specifications and updated the typical value for the VCMP offset voltage in the VCMP table in the Electrical Characteristics section.

Removed the maximum specification and reduced the typical value for hysteresis in the VCMP table in the Electrical Characteristics section.

Updated all graphs in the Electrical Characteristics section to display data for 2.0 V as the minimum voltage.

## 7.2 Revision 1.30

May 23rd, 2014

Removed "preliminary" markings

Updated HFRCO figures.

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Updated Current Consumption information.

Updated Power Management information.

Updated GPIO information.

Updated LFRCO information.

Updated HFRCO information.

Updated ULFRCO information.

Updated ADC information.

Updated DAC information.

Updated OPAMP information.

Updated ACMP information.

Updated VCMP information.

Added AUXHFRCO information.

## 7.3 Revision 1.21

November 21st, 2013

Updated figures.

Updated errata-link.

Updated chip marking.

Added link to Environmental and Quality information.

Re-added missing DAC-data.

## 7.4 Revision 1.20

September 30th, 2013

Added I2C characterization data.

Added SPI characterization data.

Added EBI characterization data.

Corrected the DAC and OPAMP2 pin sharing information in the Alternate Functionality Pinout section.

Corrected GPIO operating voltage from 1.8 V to 1.85 V.

Added the USB bootloader information.

Updated that the EM2 current consumption test was carried out with only one RAM block enabled.

Corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

## 7.5 Revision 1.10

June 28th, 2013

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

## 7.6 Revision 1.00

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Other minor corrections.

## 7.7 Revision 0.98

May 25th, 2012

Corrected EM3 current consumption in the Electrical Characteristics section.

## 7.8 Revision 0.96

February 28th, 2012

Added reference to errata document.

Corrected LQFP100 package drawing.

Updated PCB land pattern, solder mask and stencil design.

## 7.9 Revision 0.95

September 28th, 2011

Flash configuration for Giant Gecko is now 1024KB or 512KB. For flash sizes below 512KB, see the Leopard Gecko Family.

Corrected operating voltage from 1.8 V to 1.85 V.

Added rising POR level to Electrical Characteristics section.

Updated Minimum Load Capacitance ($C_{LFXOL}$) Requirement For Safe Crystal Startup.

Added Gain error drift and Offset error drift to ADC table.

Added Opamp pinout overview.

Added reference to errata document.

Corrected LQFP100 package drawing.

Updated PCB land pattern, solder mask and stencil design.

## 7.10 Revision 0.91

March 21th, 2011

Added new alternative locations for EBI and SWO.

Added new USB Pin to pinout table.

Corrected slew rate data for Opamps.

## 7.11 Revision 0.90

February 4th, 2011

Initial preliminary release.

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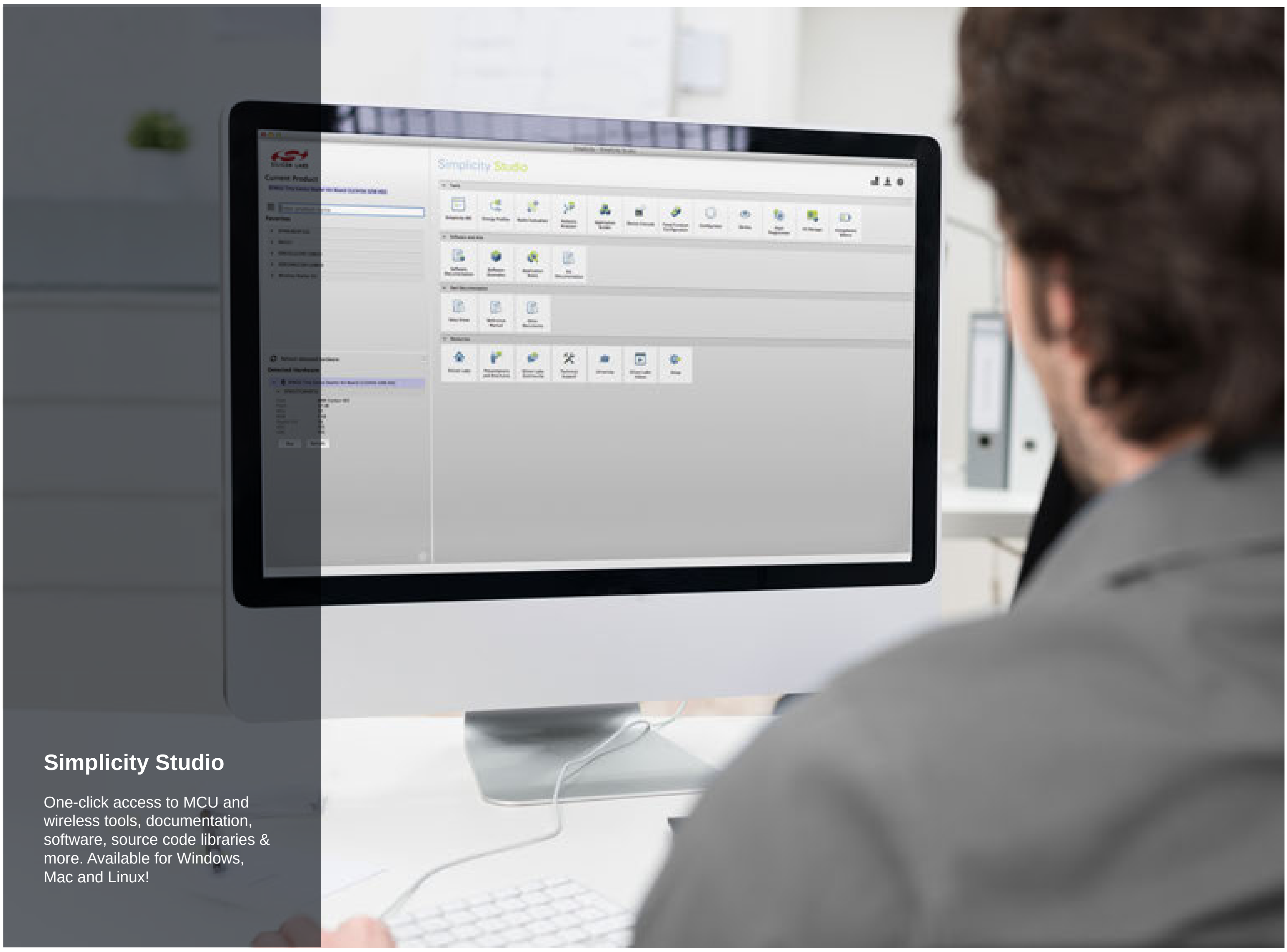

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