Absolute Maximum Ratings

Voltage on VCC Relative to Ground .....-0.5V to +6.0V
Voltage on SPRD, PDN, OE, SDA,
SCL Relative to Ground* ..... -0.5V to (V_{CC} + 0.5V)
Operating Temperature Range..... -40°C to +85°C
Programming Temperature Range.....0°C to +70°C
Storage Temperature Range..... -55°C to +125°C
Soldering Temperature ..... See IPC/JEDEC J-STD-020A

**This voltage must not exceed 6.0V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

(T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	2.7	3.3	3.6	V
High-Level Input Voltage (SDA, SCL, SPRD, PDN, OE)	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Low-Level Input Voltage (SDA, SCL, SPRD, PDN, OE)	V_{IL}		-0.3		0.3 x V_{CC}	V

DC Electrical Characteristics

(V_{CC} = +2.7V to +3.6V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
High-Level Output Voltage (OUT)	V_{OH}	I_{OH} = -4mA, V_{CC} = min	2.4			V
Low-Level Output Voltage (OUT)	V_{OL}	I_{OL} = 4mA			0.4	V
Low-Level Output Voltage (SDA)	V_{OL1}	3mA sink current			0.4	V
	V_{OL2}	6mA sink current			0.6	
High-Level Input Current	I_{IH}	V_{IH} = V_{CC}			1	µA
Low-Level Input Current	I_{IL}	V_{IL} = 0V	-1			µA
Supply Current (Active)	I_{CC}	C_L = 15pF, f_{OUT} = $f_{MOSCmax}$			12	mA
Standby Current (Power-Down)	I_{CCQ}	Power-down mode			10	µA

Master Oscillator Characteristics

(V_{CC} = +2.7V to +3.6V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNITS
Internal Master Oscillator Frequency	f_{MOSC}			33.3		66.6	MHz
Master Oscillator Frequency Tolerance	$\frac{\Delta f_{MOSC}}{f_{MOSC}}$	V_{CC} = 3.3V, T_A = +25°C (Notes 2, 10)		-0. 5		+0. 5	%
Voltage Frequency Variation	$\frac{\Delta f}{f_{MOSC}}$	T_A = +25°C (Note 3)		-0.75		+0.75	%
Temperature Frequency Variation (Note 4)	$\frac{\Delta f}{f_{MOSC}}$	V_{CC} = 3.3V, $f_{OUT} = f_{MOSCmax}$	T_A = 0°C to +85°C	-0.75		+0.75	%
			T_A = -40°C to 0°C	-2.00		+0.75	
Dither Frequency Range (Note 5)		J3 = J2 = GND			±1		%
		J3 = GND, J2 = V_{CC}			±2		
		J3 = V_{CC}, J2 = GND			±4		
		J3 = J2 = V_{CC}			±8		
Dither Frequency (Note 5)	f_{MOD}	J1 = GND, J0 = V_{CC}			f_{MOSC} / 2048		Hz
		J1 = V_{CC}, J0 = GND			f_{MOSC} / 4096		
		J1 = J0 = V_{CC}			f_{MOSC} / 8192		

AC Electrical Characteristics

(V_{CC} = +2.7V to +3.6V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Frequency Stable After PRESCALER Change					1	Period
Power-Up Time	t_{POR} + t_{STAB}	(Note 6)		40	200	µs
Enable of OUT After Exiting Power-Down Mode	t_{STAB}	(Note 6)			512	clock cycles
OUT Disabled After Entering Power-Down Mode	t_{PDN}			7		µs
Load Capacitance	C_L			15	50	pF
Output Duty Cycle (f_{OUT})				50		%

AC Electrical Characteristics—I²c Interface

(V_{CC} = +2.7V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 7)	0		400	kHz
Bus Free Time Between Stop and Start Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) Start Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Start Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 8)	20 + 0.1C_B		300	ns
SDA and SCL Fall Time	t_F	(Note 8)	20 + 0.1C_B		300	ns
Stop Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 8)			400	pF
EEPROM Write Time	t_{WR}	(Note 9)		10	20	ms

Nonvolatile Memory Characteristics

(V_{CC} = +2.7V to +3.6V.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Writes		+70°C	10,000			

Note 1: All voltages are referenced to ground.

Note 2: This is the absolute accuracy of the master oscillator frequency at the default settings with spread disabled.

Note 3: This is the change that is observed in master oscillator frequency with changes in voltage at T_A = +25°C.

Note 4: This is the change that is observed in master oscillator frequency with changes in temperature at V_{CC} = 3.3V.

Note 5: The dither deviation of the master oscillator frequency is bidirectional and results in an output frequency centered at the undithered frequency.

Note 6: This indicates the time elapsed between power-up and the output becoming active. An on-chip delay is intentionally introduced to allow the oscillator to stabilize. t_{STAB} is equivalent to 512 master clock cycles and will depend on the programmed master oscillator frequency.

Note 7: Timing shown is for fast-mode (400kHz) operation. This device is also backward compatible with I²C standard-mode timing.

Note 8: C_B—total capacitance of one bus line in picofarads.

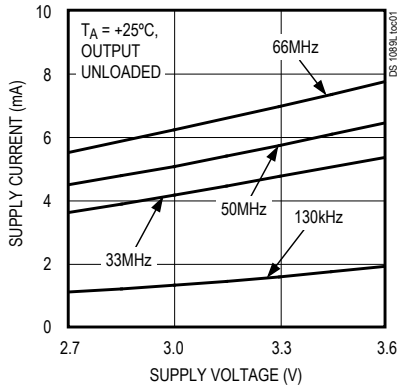
Note 9: EEPROM write time applies to all the EEPROM memory and SRAM shadowed EEPROM memory when WC = 0. The EEPROM write time begins after a stop condition occurs.

Note 10: Typical frequency shift due to aging is ±0.25%. Aging stressing includes Level 1 moisture reflow conditioning (24hr) +125°C bake, 168hr +85°C/85°RH moisture soak, and three solder reflow passes +269 +0/-5°C peak) followed by 408hr max V_{CC} biased 125°C HTOL, 500 temperature cycles at -55°C to +125°C, 96hr +130°C/85%RH/3,6V HAST and 168hr +121°C/2 ATM Steam/Unbiased Autoclave.

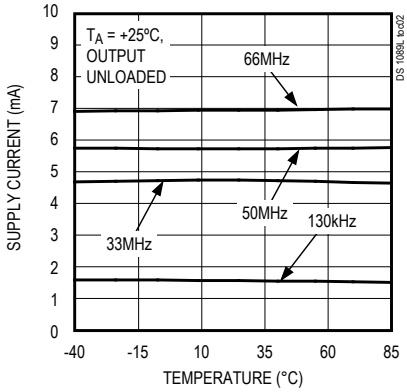
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

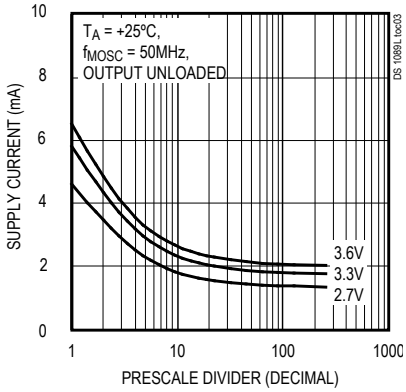
ACTIVE SUPPLY CURRENT vs. SUPPLY VOLTAGE



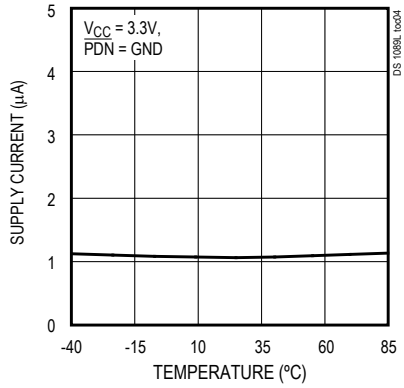
ACTIVE SUPPLY CURRENT vs. TEMPERATURE



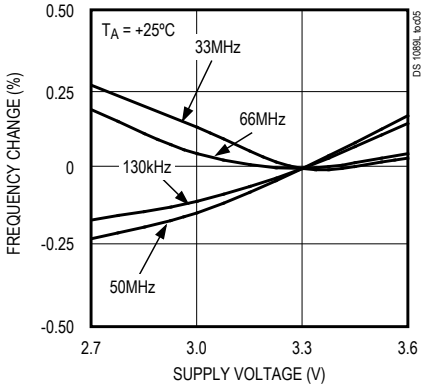
SUPPLY CURRENT vs. PRESCALER



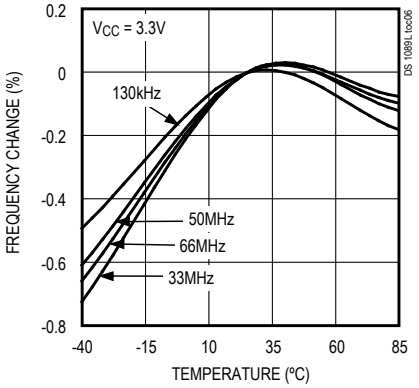
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



FREQUENCY % CHANGE vs. SUPPLY VOLTAGE



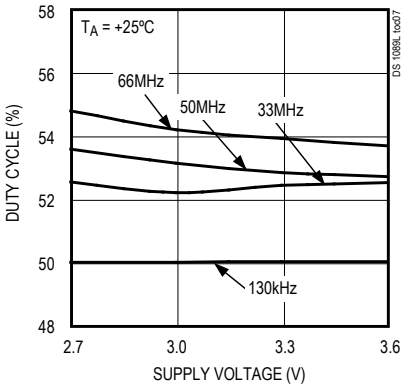
FREQUENCY % CHANGE vs. TEMPERATURE



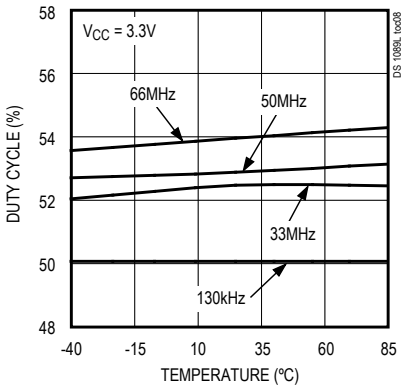
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

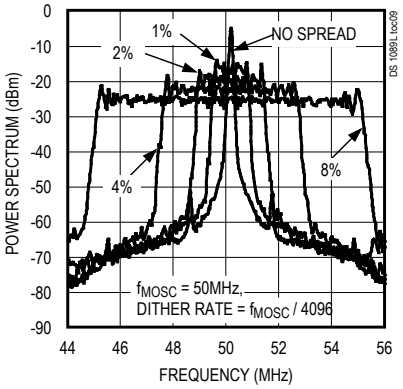
DUTY CYCLE vs. SUPPLY VOLTAGE



DUTY CYCLE vs. TEMPERATURE



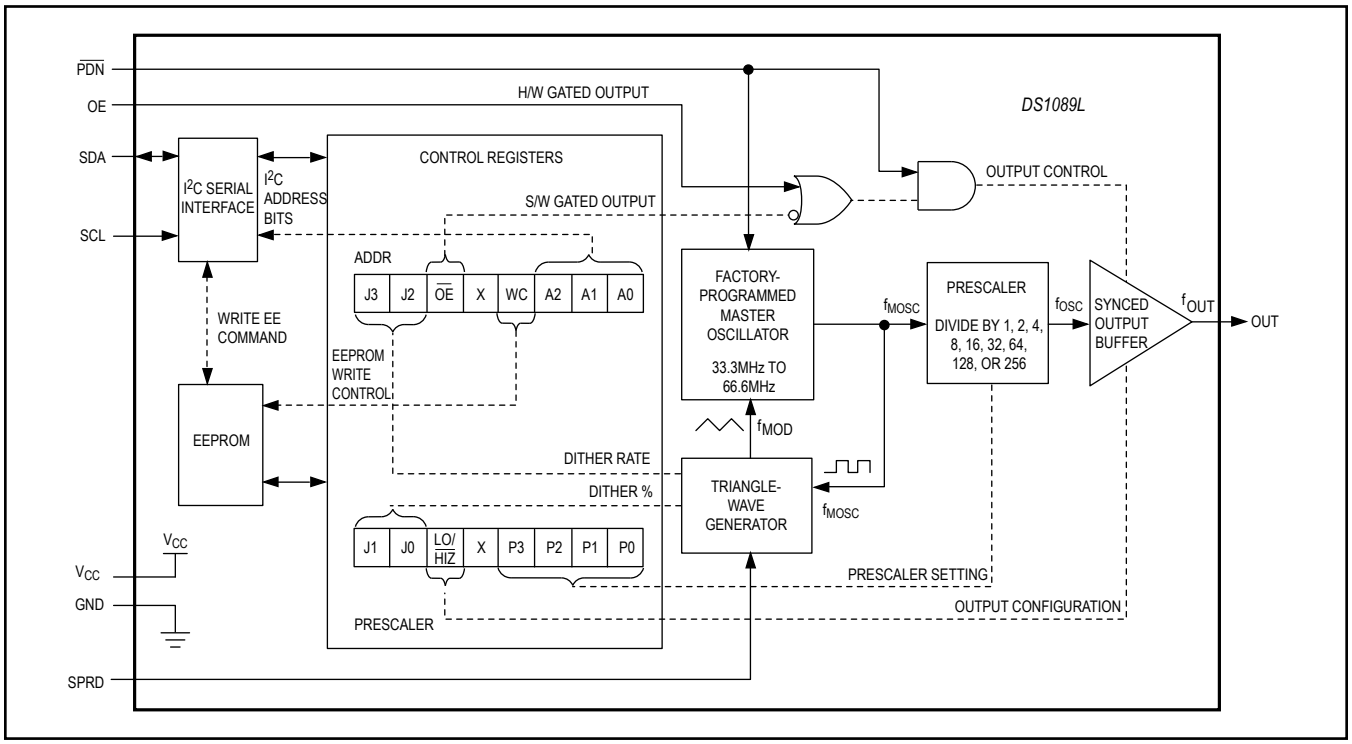
SPECTRUM COMPARISON (120kHz BW, SAMPLE DETECT)



Pin Description

PIN	NAME	FUNCTION
1	OUT	Oscillator Output
2	SPRD	Dither Enable. When the pin is high, the dither is enabled. When the pin is low, the dither is disabled.
3	V_{CC}	Power Supply
4	GND	Ground
5	OE	Output Enable. When the pin is high, the output buffer is enabled. When the pin is low, the output is disabled but the internal master oscillator is still on.
6	$\overline{PDN}$	Power-Down. When the pin is high, the master oscillator is enabled. When the pin is low, the master oscillator and the output buffer are disabled (power-down mode).
7	SDA	I²C Serial Data. This pin is for serial data transfer to and from the device.
8	SCL	I²C Serial Clock. This pin is used to clock data into and out of the device.

Block Diagram



Detailed Description

Master Oscillator

The internal master oscillator is capable of generating a square wave with a 33.3MHz to 66.6MHz frequency range. The master oscillator frequency (f_{MOSC}) is factory programmed, and is specified in the *Ordering Information*.

Prescaler

The user can program the prescaler divider to produce an output frequency (f_{OUT}) as low as 130kHz using bits P0, P1, P2, and P3 in the PRESCALER register. The output frequency can be calculated using Equation 1. Any value programmed greater than 2^8 will be decoded as 2^8. See Table 1 for prescaler divider settings.

Equation 1

$$\text{Output Frequency (Hz)}\ f_{OSC} = \frac{f_{MOSC}}{2^x}$$

where x = P3, P2, P1, P0

Table 1. Prescaler Divider Settings

BITS P3, P2, P1, P0	2^x =	$f_{OUT} = f_{OSC}$
0000	1	f_{MOSC}
0001	2	f_{MOSC} / 2
0010	4	f_{MOSC} / 4
0011	8	f_{MOSC} / 8
0100	16	f_{MOSC} / 16
0101	32	f_{MOSC} / 32
0110	64	f_{MOSC} / 64
0111	128	f_{MOSC} / 128
1000	256	f_{MOSC} / 256
1111	256	f_{MOSC} / 256

Output Control

Two user control signals control the output. The output enable pin (OE) gates the output buffer and the power-down pin ($\overline{PDN}$) disables the master oscillator and turns off the output for power-sensitive applications. (**Note:** the power-down command must persist for at least two output frequency cycles plus 10µs for deglitching purposes.) On power-up, the output is disabled until power is stable and the master oscillator has generated 512 clock cycles.

Additionally, the OE input is OR'ed with the $\overline{OE}$ bit in the ADDR register, allowing for either hardware or software gating of the output waveform (see the *Block Diagram*).

Both controls feature a synchronous enable, which ensures that there are no output glitches when the output is enabled. The synchronous enable also ensures a constant time interval (for a given frequency setting) from an enable signal to the first output transition.

Dither Generator

The DS1089L has the ability to reduce radiated emission peaks. The output frequency can be dithered by ±1%, ±2%, ±4%, or ±8% symmetrically around the programmed center frequency. Although the output frequency changes when the dither is enabled, the duty cycle does not change.

The dither rate (f_{MOD}) is controlled by the J0 and J1 bits in the PRESCALER register and is enabled with the SPRD pin. The maximum spectral attenuation occurs when the prescaler is set to 1. The spectral attenuation is reduced by 2.7dB for every factor of 2 that is used in the prescaler. This happens because the prescaler's divider function tends to average the dither in creating the lower frequency. However, the most stringent spectral emission limits are imposed on the higher frequencies where the prescaler is set to a low divider ratio.

A triangle-wave generator injects an offset element into the master oscillator to dither its output. The dither rate can be calculated based on the master oscillator frequency (see Equation 2).

Equation 2

$$f_{MOD} = \frac{f_{MOSC}}{n}$$

where f_{MOD} = dither frequency, f_{MOSC} = master oscillator frequency, and *n* = divider setting (see Table 2).

Dither Percentage Settings

The dither amplitude (measured in percentage of the master oscillator center frequency) is set using the J2 and J3 bits in the ADDR register. This circuit uses a sense current from the master oscillator bias circuit to adjust the amplitude of the triangle-wave signal to a voltage level that modulates the master oscillator to a percentage of its factory-programmed center frequency. This percentage is set in the application to be ±1%, ±2%, ±4%, or ±8% (see Table 3).

The location of bits P3, P2, P1, P0, J1, and J0 in the PRESCALER register and bits J3 and J2 in the ADDR register are shown in the *Register Summary* section.

Table 2. Dither Frequency Settings

BITS J1, J0	DITHER FREQUENCY
00	No dither
01	$f_{MOSC}/2048$
10	$f_{MOSC}/4096$
11	$f_{MOSC}/8192$

Table 3. Dither Percentage Settings

BITS J3, J2	DITHER AMOUNT
00	±1%
01	±2%
10	±4%
11	±8%

When dither is enabled (by selecting a dither frequency setting greater than 0 with SPRD high), the master oscillator frequency is dithered around the center frequency by the selected percentage from the programmed f_{MOSC} (see Figure 2). For example, if f_{MOSC} is programmed to 40MHz (factory setting) and the dither amount is programmed to ±1%, the frequency of f_{MOSC} will dither between 39.6MHz and 40.4MHz at a modulation frequency determined by the selected dither frequency. Continuing with the same example, if J1 = 0 and J0 = 1, selecting $f_{MOSC}/2048$, then the dither frequency would be 19.531kHz.

Register Summary

The DS1089L registers are used to change the dither amount, output frequency, and slave address. A bit summary of the registers is shown in Table 4. Once programmed into EEPROM, the settings only need to be reprogrammed if it is desired to reconfigure the device.

PRESCALER Register

Bits 7 to 6: **Dither Frequency.** The J1 and J0 bits control the dither frequency applied to the output. See Table 2 for divider settings. If either of bits J1 or J0 is high and SPRD is high, dither is enabled.

Bit 5: **Output Low or Hi-Z.** The LO/$\overline{HIZ}$ bit determines the state of the output during power-down. While the output is deactivated, if the LO/$\overline{HIZ}$ bit is set to 0, the output will be high impedance (high-Z). If the LO/$\overline{HIZ}$ bit is set to 1, the output will be driven low.

Bit 4: **Reserved.**

Bits 3 to 0: **Prescaler Divider.** The prescaler bits (bits P3 to P0) divide the master oscillator frequency by 2^x where x can be from 0 to 8. Any prescaler bit value entered that is greater than 8 will decode as 8. See Table 1 for prescaler settings.

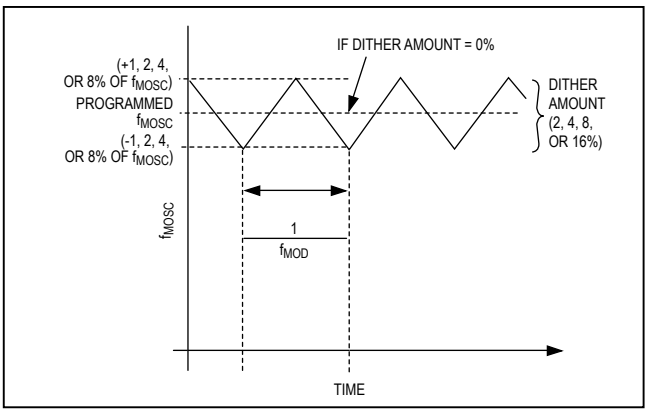


Figure 2. Output Frequency vs. Dither Rate

ADDR Register

Bits 7 to 6: **Dither Percentage.** The J3 and J2 bits control the selected dither amplitude (%). When both J3 and J2 are set to 0, the default dither rate is ±1%.

Bit 5: **Output Enable.** The $\overline{OE}$ bit and the OE pin state determine if the output is on when the device is active ($\overline{PDN}$ = V_{IH}). If (OE = 0 OR $\overline{OE}$ is high) AND the PDN pin is high, the output will be driven.

Bit 4: **Reserved.**

Bit 3: **Write Control.** The WC bit determines if the EEPROM is to be written after register contents have been changed. If WC = 0 (default), EEPROM is written automatically after a write. If WC = 1, the EEPROM is only written when the WRITE EE command is issued. See the *WRITE EE* Command section for more information.

Bits 2 to 0: **Address.** The A0, A1, A2 bits determine the lower nibble of the I^2C slave address.

Table 4. Register Summary

REGISTER	ADDR	BIT7	BINARY						BIT0	DEFAULT	ACCESS
PRESCALER	02h	J1	J0	LO/$\overline{HIZ}$	X	P3	P2	P1	P0	xx00xxxxb	R/W
ADDR	0Dh	J3	J2	$\overline{OE}$	X	WC	A2	A1	A0	xx100000b	R/W
WRITE EE	3Fh	No Data								—	—

X = "don't care"
x = values depend on custom settings

WRITE EE Command

The WRITE EE command is useful in closed-loop applications where the registers are frequently written. In applications where the register contents are frequently written, the WC bit should be set to 1 to prevent wearing out the EEPROM. Regardless of the value of the WC bit, the value of the ADDR register is always written immediately to EEPROM. When the WRITE EE command has been received, the contents of the registers are written into the EEPROM, thus locking in the register settings.

I²C Serial Port Operation

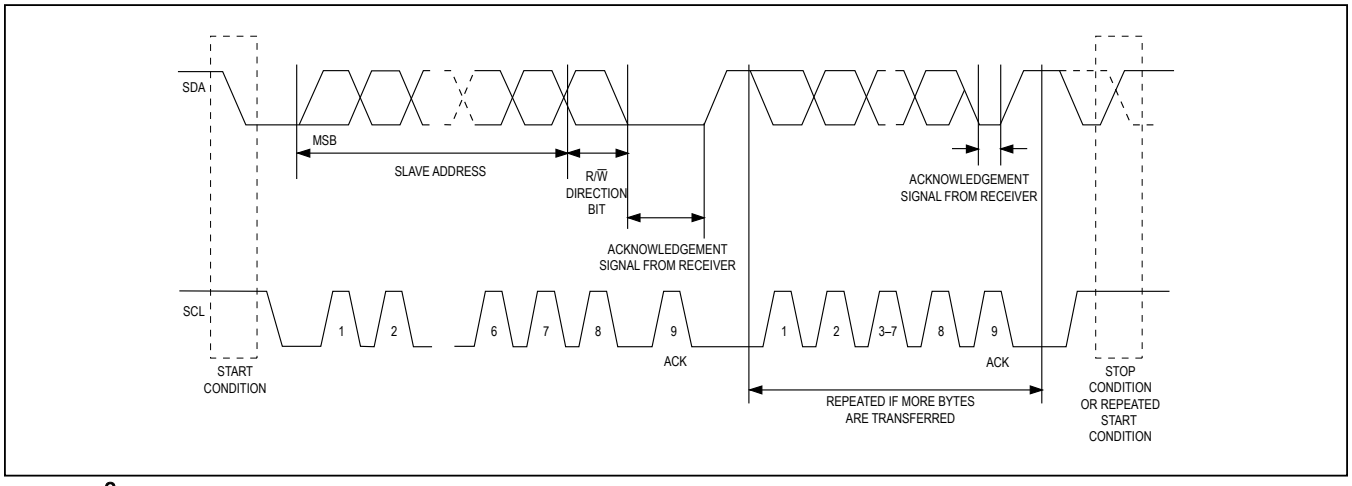


Figure 3. I²C Data Transfer Protocol

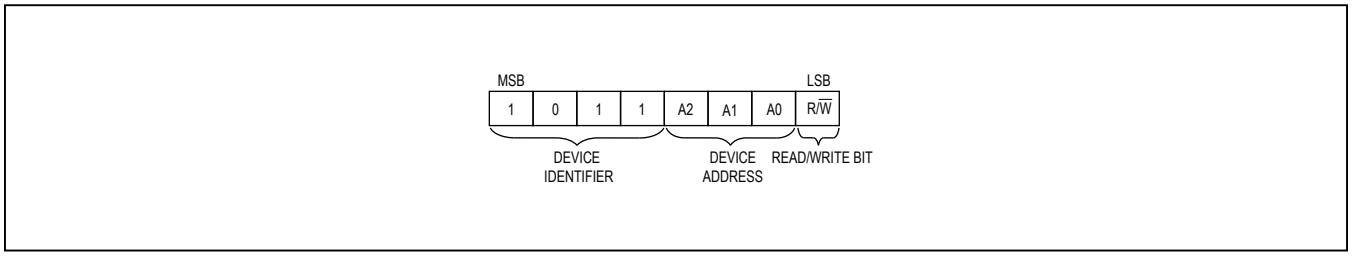


Figure 4. Slave Address Byte

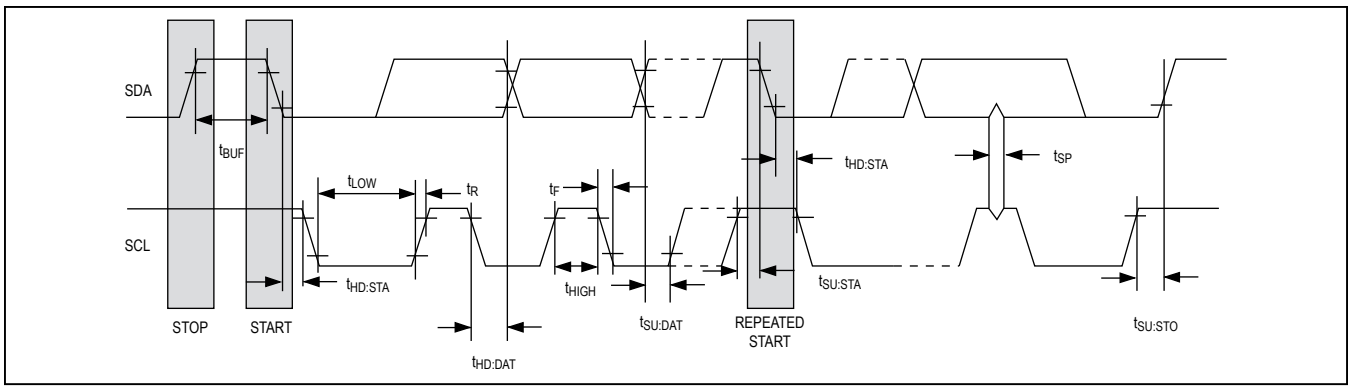


Figure 5. I²C AC Characteristics

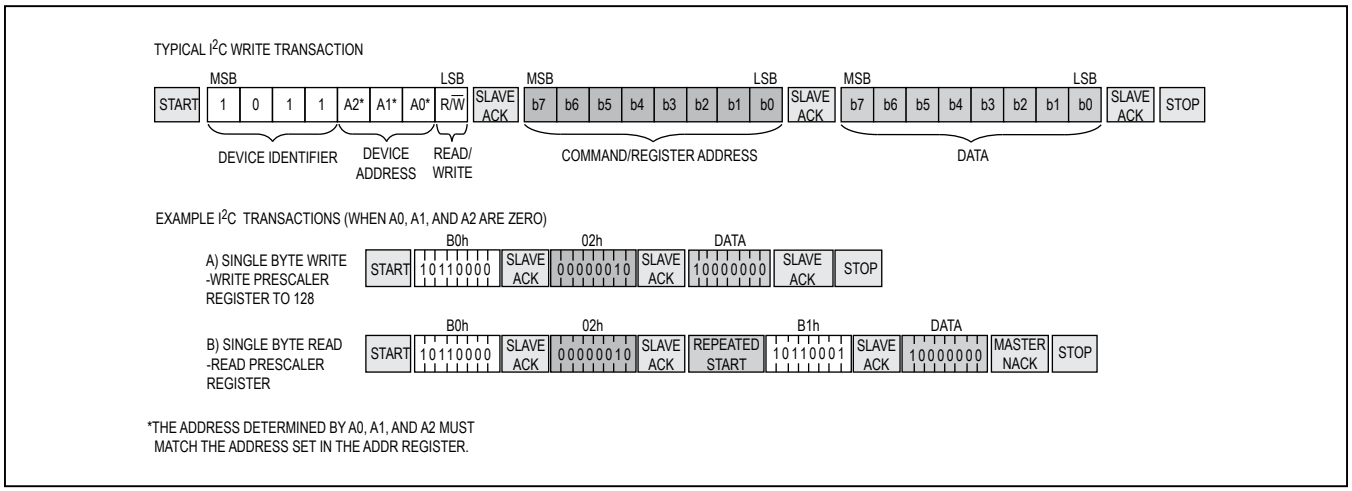


Figure 6. I²C Transactions

Applications Information

Power-Supply Decoupling

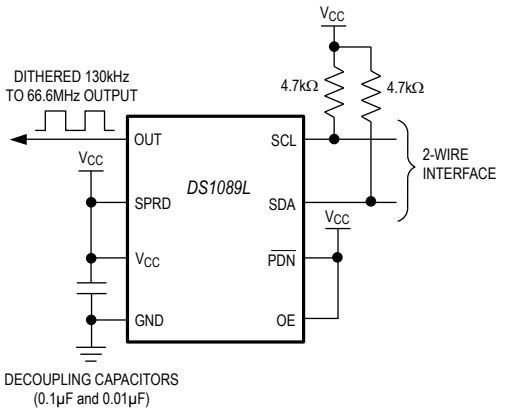
To achieve the best results when using the DS1089L, decouple the power supply with 0.01µF and 0.1µF high-quality, ceramic, surface-mount capacitors. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications. These capacitors should be placed as close to the V_{CC} and GND pins as possible.

Stand-Alone Mode

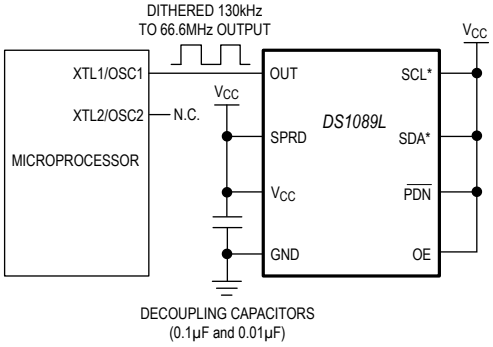
SCL and SDA cannot be left floating even in stand-alone mode. If the DS1089L will never need to be programmed in-circuit, including during production testing, SDA and SCL can be connected high.

Typical Operating Circuits

PROCESSOR-CONTROLLED MODE



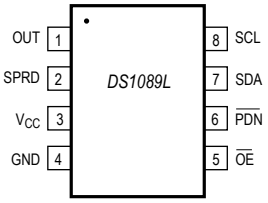
STAND-ALONE MODE



*SDA AND SCL CAN BE CONNECTED DIRECTLY HIGH IF THE DS1089L NEVER NEEDS TO BE PROGRAMMED IN-CIRCUIT, INCLUDING DURING PRODUCTION TESTING.

Pin Configuration

TOP VIEW



µSOP (118 mils)

Chip Topology

TRANSISTOR COUNT: 5985

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	5/06		—
3	2/15	Removed automotive reference from data sheet	1