Operating Modes

The CY7C245A is a CMOS electrically programmable read only memory organized as 2048 words x 8 bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The CY7C245A incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined micropro-grammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with a programmable synchronous (E_S) or asynchronous (E) output enable and asynchronous initial-ization (INIT).

Upon power-up the state of the outputs will depend on the programmed state of the enable function (E_S or E). If the synchronous enable (E_S) has been programmed, the register will be in the set condition causing the outputs (O_0–O_7) to be in the OFF or high-impedance state. If the asynchronous enable (E) is being used, the outputs will come up in the OFF or high-impedance state only if the enable (E) input is at a HIGH logic level. Data is read by applying the memory location to the address inputs (A_0–A_{10}) and a logic LOW to the enable input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs (O_0–O_7).

If the asynchronous enable (E) is being used, the outputs may be disabled at any time by switching the enable to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

If the synchronous enable (E_S) is being used, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low-to-high transition of the clock. This unique feature allows the CY7C245A decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C245A has an asynchronous initialize input (INIT). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophis-ticated functions such as a built-in "jump start" address. When activated, the initialize control input causes the contents of a user-programmed 2049th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of 1s and 0s into the register. In the unprogrammed state, activating INIT will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating INIT performs a register PRESET (all outputs HIGH).

Applying a LOW to the INIT input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable (E) LOW.

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C245A. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm2. For an ultraviolet lamp with a 12 mW/cm2 power rating the exposure time would be approximately 35 minutes. The 7C245A needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm2 is the recommended maximum dosage.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Bit Map Data

Programmer Address		RAM Data
Decimal	Hex	Contents
0	0	Data
.	.	.
.	.	.
.	.	.
2047	7FF	Data
2048	800	Init Byte
2049	801	Control Byte

Control Byte
  00   Asynchronous output enable (default state)
  01   Synchronous output enable

Table 1. Mode Selection

Mode	Read or Output Disable	Pin Function[1]							
	Other	A_{10}–A_4	A_3	A_2–A_1	A_0	CP	$\overline{E}$, $\overline{E_S}$	INIT	O_7–O_0
		A_{10}–A_4	A_3	A_2–A_1	A_0	PGM	VFY	V_{PP}	D_7–D_0
Read		A_{10}–A_4	A_3	A_2–A_1	A_0	V_{IL}/V_{IH}	V_{IL}	V_{IH}	O_7–O_0
Output Disable		A_{10}–A_4	A_3	A_2–A_1	A_0	X	V_{IH}	V_{IH}	High Z
Initialize		A_{10}–A_4	A_3	A_2–A_1	A_0	X	V_{IL}	V_{IL}	Init. Byte
Program		A_{10}–A_4	A_3	A_2–A_1	A_0	V_{ILP}	V_{IHP}	V_{PP}	D_7–D_0
Program Verify		A_{10}–A_4	A_3	A_2–A_1	A_0	V_{IHP}	V_{ILP}	V_{PP}	O_7–O_0
Program Inhibit		A_{10}–A_4	A_3	A_2–A_1	A_0	V_{IHP}	V_{IHP}	V_{PP}	High Z
Intelligent Program		A_{10}–A_4	A_3	A_2–A_1	A_0	V_{ILP}	V_{IHP}	V_{PP}	D_7–D_0
Program Synchronous Enable		A_{10}–A_4	V_{IHP}	A_2–A_1	V_{PP}	V_{ILP}	V_{IHP}	V_{PP}	High Z
Program Initialization Byte		A_{10}–A_4	V_{ILP}	A_2–A_1	V_{PP}	V_{ILP}	V_{IHP}	V_{PP}	D_7–D_0
Blank Check Zeros		A_{10}–A_4	A_3	A_2–A_1	A_0	V_{IHP}	V_{ILP}	V_{PP}	Zeros

Figure 1. Programming Pinouts

DIP Top View

LCC/PLCC (Opaque Only) Top View
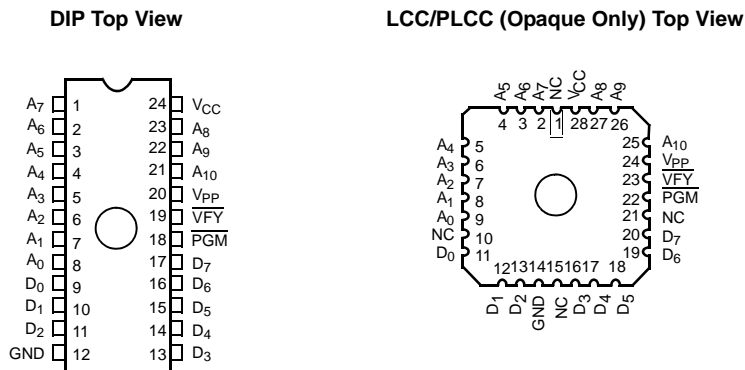
MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962-88735	033X	CY7C245A-25LMB
5962-88735	04LX	CY7C245A-25DMB

Switching Characteristics

Parameter	Subgroups
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11

Note
1. X = "don't care" but not to exceed V_{CC} + 5%.

[+] Feedback

Maximum Ratings[2]

(Above which the useful life may be impaired. For user guide-lines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied... −55°C to +125°C

Supply Voltage to Ground Potential
(Pin 24 to Pin 12).. −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 13.0V

UV Erasure .... 7258 Wsec/cm^2

Static Discharge Voltage... > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current... > 200 mA

Operating Range

Range	Ambient Temperature	V$_{CC}$
Commercial	0°C to +70°C	5V ±10%
Military[3]	−55°C to +125°C	5V ±10%
Industrial	−40°C to +85°C	5V ±10%

Electrical Characteristics Over the Operating Range[4, 5]

Parameter	Description	Test Conditions	7C245A-15 Min.	7C245A-15 Max.	7C245A-18 Min.	7C245A-18 Max.	7C245A-25 7C245A-35 7C245A-45 Min.	7C245A-25 7C245A-35 7C245A-45 Max.	Unit
V$_{OH}$	Output HIGH Voltage	V$_{CC}$ = Min., I$_{OH}$ = −4.0 mA V$_{IN}$ = V$_{IH}$ or V$_{IL}$	2.4		2.4		2.4		V
V$_{OL}$	Output LOW Voltage	V$_{CC}$ = Min., I$_{OL}$ = 16 mA V$_{IN}$ = V$_{IH}$ or V$_{IL}$		0.4		0.4		0.4	V
V$_{IH}$	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs	2.0	V$_{CC}$	2.0	V$_{CC}$	2.0	V$_{CC}$	V
V$_{IL}$	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		0.8		0.8		0.8	V
I$_{IX}$	Input Leakage Current	GND ≤ V$_{IN}$ ≤ V$_{CC}$	−10	+10	−10	+10	−10	+10	µA
V$_{CD}$	Input Clamp Diode Voltage	Note 5							
I$_{OZ}$	Output Leakage Current	GND ≤ V$_O$ ≤ V$_{CC}$ Output Disabled[6]	−10	+10	−10	+10	−10	+10	µA
I$_{OS}$	Output Short Circuit Current	V$_{CC}$ = Max., V$_{OUT}$ = 0.0V[7]	−20	−90	−20	−90	−20	−90	mA
I$_{CC}$	Power Supply Current	V$_{CC}$ = Max., I$_{OUT}$ = 0 mA — Com'l		120		120		90	mA
		V$_{CC}$ = Max., I$_{OUT}$ = 0 mA — Mil				120		120	
V$_{PP}$	Programming Supply Voltage		12	13	12	13	12	13	V
I$_{PP}$	Programming Supply Current			50		50		50	mA
V$_{IHP}$	Input HIGH Programming Voltage		3.0		3.0		3.0		V
V$_{ILP}$	Input LOW Programming Voltage			0.4		0.4		0.4	V

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C$_{IN}$	Input Capacitance	T$_A$ = 25°C, f = 1 MHz, V$_{CC}$ = 5.0V	10	pF
C$_{OUT}$	Output Capacitance		10	pF

Notes
2. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
3. T$_A$ is the "instant on" case temperature.
4. See page 3 of this data sheet for Group A subgroup testing information.
5. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
6. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
7. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

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[+] Feedback

AC Test Loads and Waveforms[4, 5]

(a) Normal Load

5V — R1 250Ω
OUTPUT
50 pF — R2 167Ω
INCLUDING JIG AND SCOPE

(b) High Z Load

5V — R1 250Ω
OUTPUT
5 pF — R2 167Ω
INCLUDING JIG AND SCOPE

ALL INPUT PULSES

3.0V — 90% / 90%
GND — 10% / 10%
≤ 5 ns   ≤ 5 ns
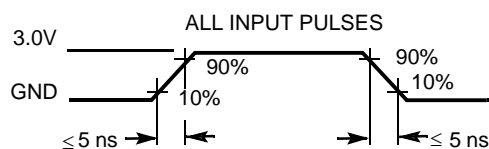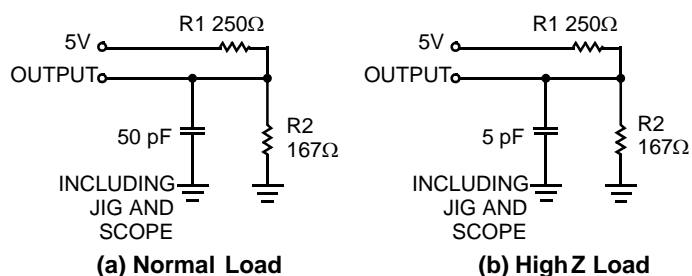
Equivalent to: THÉVENIN EQUIVALENT

OUTPUT — 100Ω — 2.0V

Switching Characteristics Over Operating Range[4, 5]

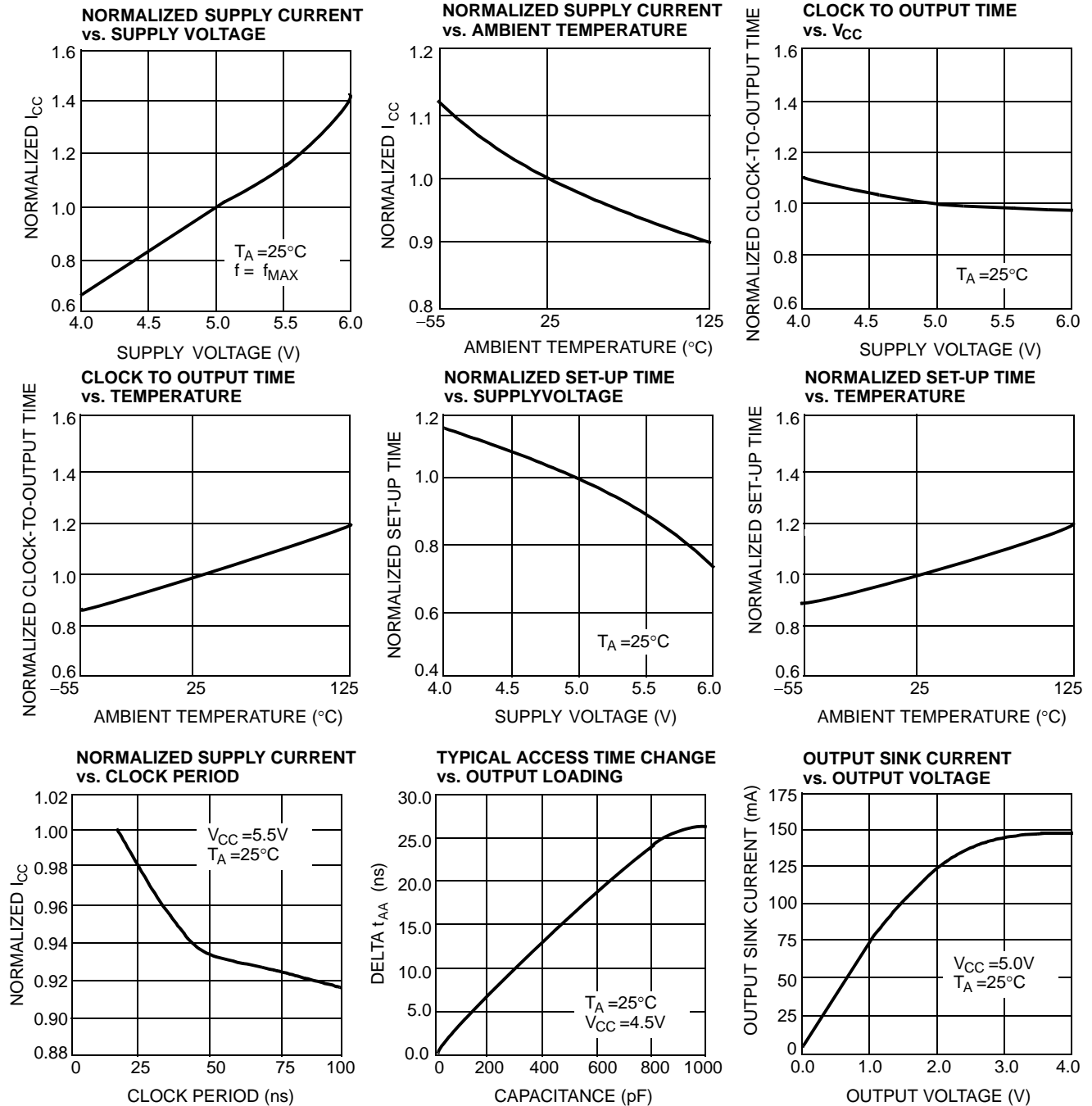| Parameter	Description	7C245A-15 Min.	7C245A-15 Max.	7C245A-18 Min.	7C245A-18 Max.	7C245A-35 Min.	7C245A-35 Max.	7C245A-25 Min.	7C245A-25 Max.	7C245A-35 Min.	7C245A-35 Max.	Unit
t_{SA}	Address Set-Up to Clock HIGH	15		18		25		35		45		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		10		12		12		15		25	ns
t_{PWC}	Clock Pulse Width	10		12		15		20		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock HIGH	10		10		12		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	5		5		5		5		5		ns
t_{DI}	Delay from INIT to Valid Output		15		20		20		20		35	ns
t_{RI}	INIT Recovery to Clock HIGH	10		12		15		20		20		ns
t_{PWI}	INIT Pulse Width	10		12		15		20		25		ns
t_{COS}	Valid Output from Clock HIGH[8]		15		15		15		20		30	ns
t_{HZC}	Inactive Output from Clock HIGH[8]		15		15		15		20		30	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW[9]		12		15		15		20		30	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH[9]		15		15		15		20		30	ns

Notes
8. Applies only when the synchronous ($\overline{E}_S$) function is used.
9. Applies only when the asynchronous ($\overline{E}$) function is used.

Switching Waveforms[5]

[+] Feedback
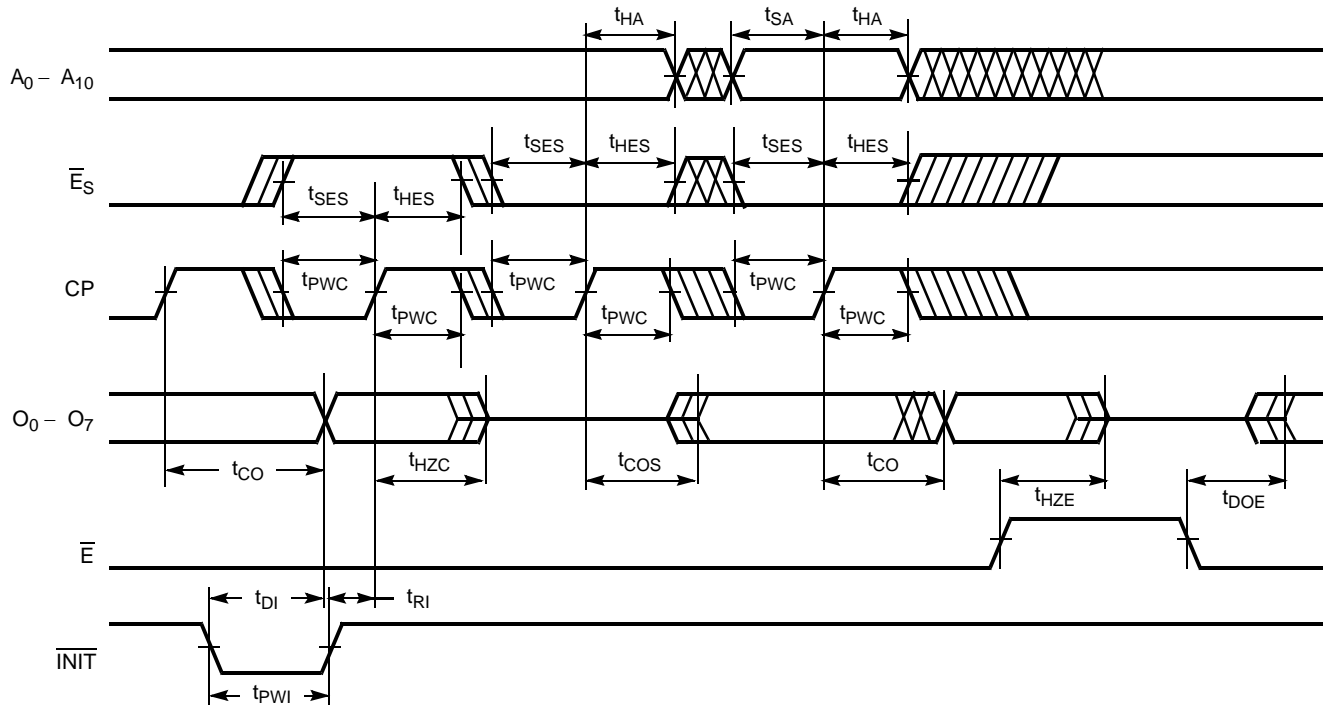
Typical DC and AC Characteristics

NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

$T_A = 25°C$
$f = f_{MAX}$

NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE

CLOCK TO OUTPUT TIME vs. V_{CC}

$T_A = 25°C$

CLOCK TO OUTPUT TIME vs. TEMPERATURE

NORMALIZED SET-UP TIME vs. SUPPLYVOLTAGE

$T_A = 25°C$

NORMALIZED SET-UP TIME vs. TEMPERATURE

NORMALIZED SUPPLY CURRENT vs. CLOCK PERIOD

$V_{CC} = 5.5V$
$T_A = 25°C$

TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING

$T_A = 25°C$
$V_{CC} = 4.5V$

OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

$V_{CC} = 5.0V$
$T_A = 25°C$

Ordering Information

Speed (ns)		I_{CC} (mA)	Ordering Code	Package Type	Package Type	Operating Range
t_{SA}	t_{CO}					
15	10	120	CY7C245A-15JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
15	10	120	CY7C245A-15JI	J64	28-Lead Plastic Leaded Chip Carrier	Industrial
18	12	120	CY7C245A-18QMB	Q64	28-Pin Windowed Leadless Chip Carrier	Military

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[+] Feedback

Ordering Information (continued)

| Speed (ns)		I_{CC} (mA)	Ordering Code	Package Type	Package Type	Operating Range
t_{SA}	t_{CO}					
18	12	120	CY7C245A-18WMB	W14	24-Lead (300-Mil) Windowed CerDIP	Military
25	15	60	CY7C245A-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
25	15	90	CY7C245A-25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
35	20	60	CY7C245A-35WC	W14	24-Lead (300-Mil) Windowed CerDIP	Commercial
		120	CY7C245A-35QMB	Q64	28-Pin Windowed Leadless Chip Carrier	Military

Package Diagrams

Figure 2. 24-Lead (300-Mil) CerDIP D14

[+] Feedback
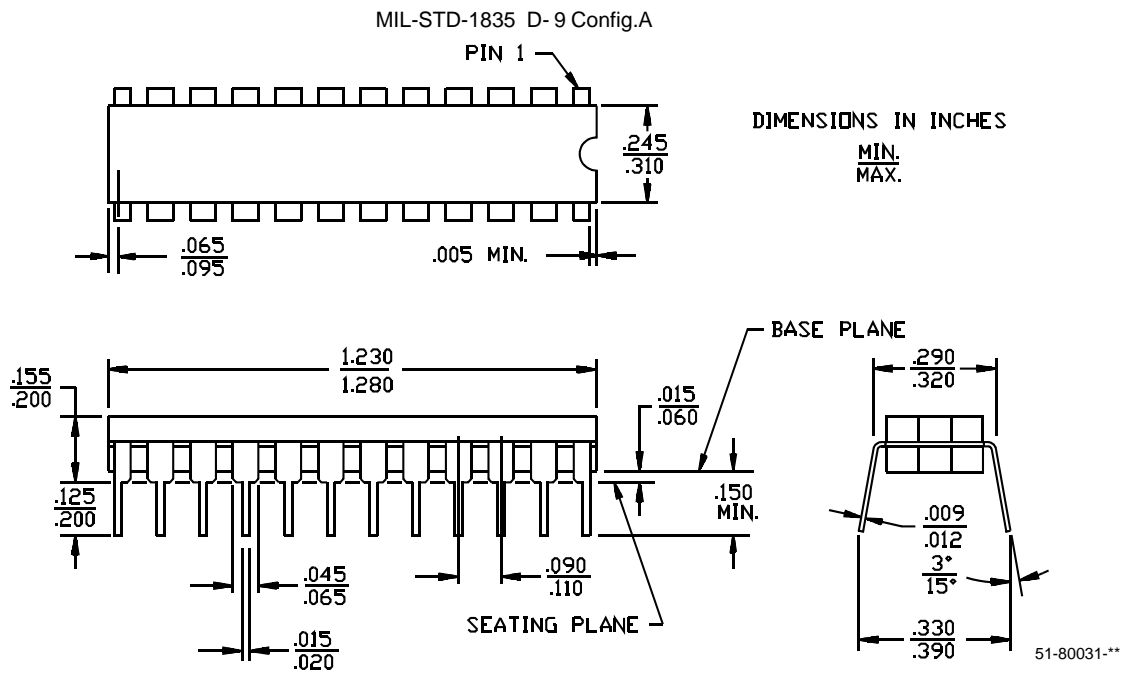
Package Diagrams (continued)

Figure 3. 28-Lead Plastic Leaded Chip Carrier J64
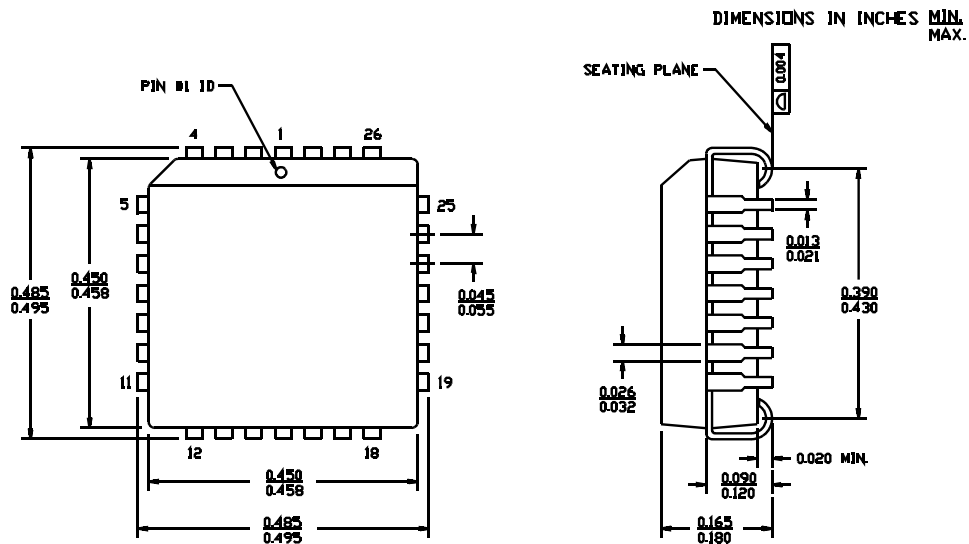
51-85001-*A

Figure 4. 24-Lead (300-Mil) PDIP P13

51-85013-*B

[+] Feedback
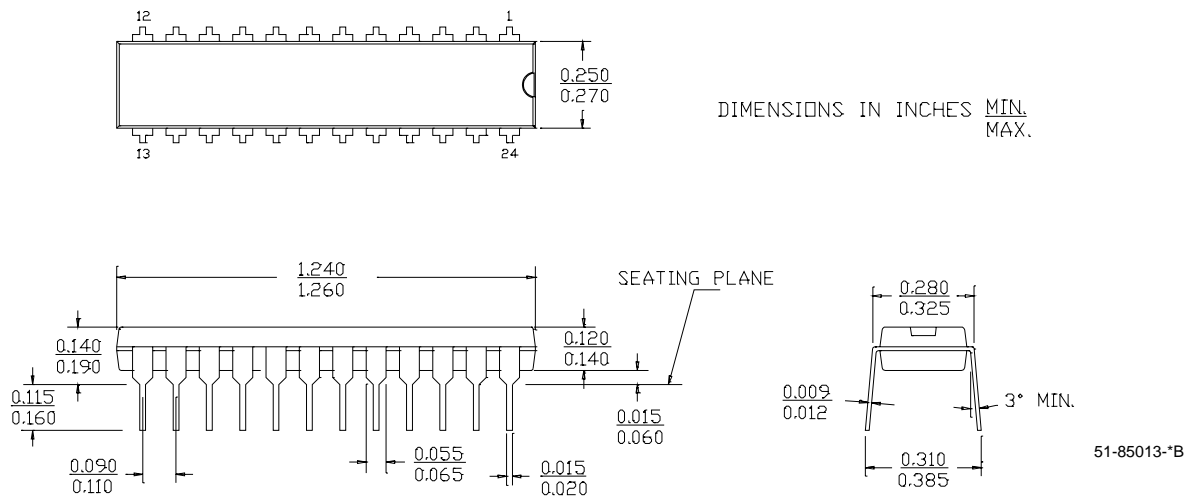
Package Diagrams (continued)

Figure 5. 28-Pin Windowed Leadless Chip Carrier Q64

MIL–STD–1835 C–4

.045 / .055

PIN #1

.022 / .028

DIMENSIONS IN INCHES
MIN.
MAX.

.045 / .055

.045 / .055

.009 R.
28 PLACES

.084 / .110

.054 / .066

.290 DIA.
LENS

.440 / .460

.440 / .460

51-80102-**

[+] Feedback
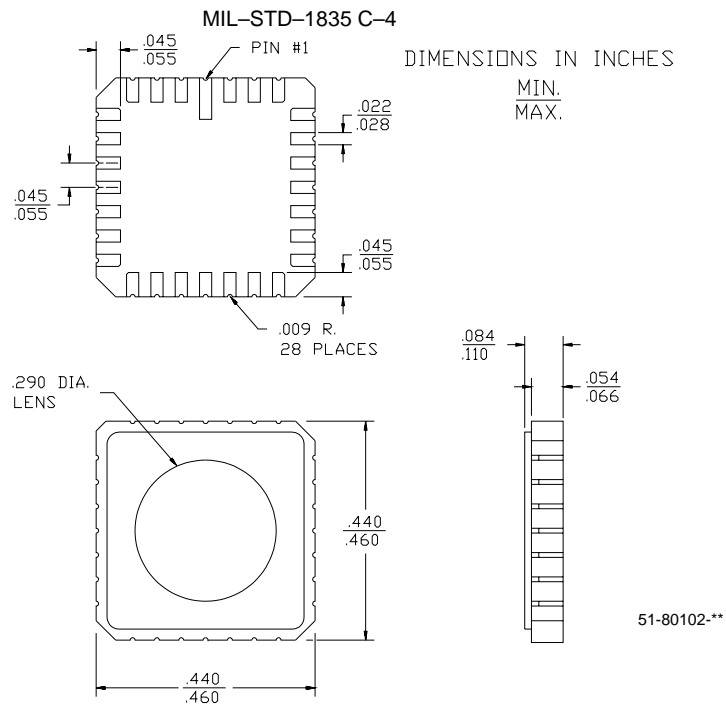
Package Diagrams (continued)

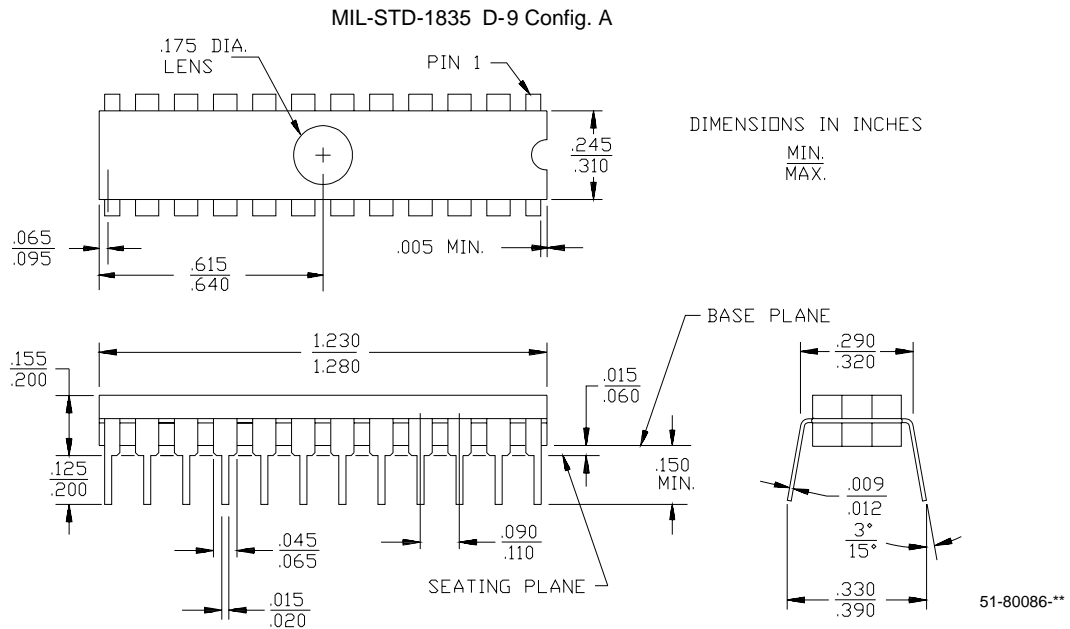**Figure 6. 24-Lead (300-Mil) SOIC S13**

NOTE :

1. JEDEC STD REF MO-119

2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH,BUT
   DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE.
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.010 in (0.254 mm) PER SIDE

3. DIMENSIONS IN INCHES   MIN.
                           MAX.

4. PACKAGE WEIGHT 0.65gms

PIN 1 ID

12   1

0.291[7.391]
0.300[7.620]

0.394[10.007]
0.419[10.642]

13   24

0.026[0.660]
0.032[0.812]

PART #		
S24.3	STANDARD PKG.	
SZ24.3	LEAD FREE PKG.	

SEATING PLANE

0.597[15.163]
0.615[15.621]

0.092[2.336]
0.105[2.667]

0.004[0.101]

0.004[0.101]
0.0118[0.299]

0.050[1.270]
TYP.

0.013[0.330]
0.019[0.482]

0.0091[0.231]
0.0125[0.317]

0.015[0.381]
0.050[1.270]

51-85025-*C

[+] Feedback

Package Diagrams (continued)

Figure 7. 24-Lead (300-Mil) Windowed CerDIP W14

MIL-STD-1835 D-9 Config. A

All product and company names mentioned in this document may be the trademarks of their respective holders.

Document History Page

Document Title: CY7C245A 2K x 8 Reprogrammable Registered PROM				
Document Number: 38-04007				

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	113863	3/6/02	DSG	Changed from Spec number: 38-00074 to 38-04007
*A	118894	10/09/02	GBI	Updated ordering information
*B	122248	12/27/02	RBI	Added power-up requirements to Operating Conditions information
*C	130688	10/30/03	LSY	Added CY7C245A-15JI part number
*D	130942	11/10/03	KKV	Minor change: soft copy became corrupted after sign off and before Tech Pubs. Replaced with correct copy
*E	499542	See ECN	PCI	Updated ordering information

[+] Feedback