4-Mbit (512K words × 8-bit) Static RAM

Features

- High speed
  - t_{AA} = 10 ns
- Low active and standby currents
  - Active current: I_{CC} = 38 mA typical
  - Standby current: I_{SB2} = 6 mA typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0 V data retention
- TTL-compatible inputs and outputs
- Pb-free 36-pin SOJ and 44-pin TSOP II packages

Functional Description

CY7C1049GN is a high-performance CMOS fast static RAM device organized as 512K words by 8-bits.

Data writes are performed by asserting the Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW, while providing the data on I/O_0 through I/O_7 and address on A_0 through A_{18} pins.

Data reads are performed by asserting the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) inputs LOW and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O_0 through I/O_7).

All I/Os (I/O_0 through I/O_7) are placed in a high-impedance state during the following events:

- The device is deselected ($\overline{CE}$ HIGH)
- The control signal $\overline{OE}$ is de-asserted

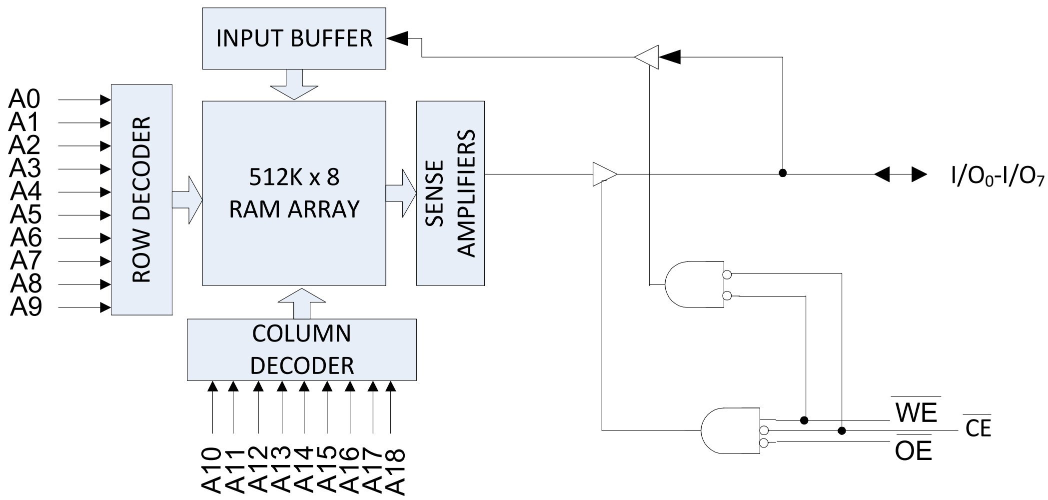
The logic block diagram is on page 2.

Product Portfolio

Product	Range	V_{CC} Range (V)	Speed (ns) 10/15	Power Dissipation			
				Operating I_{CC}, (mA) f = f_{max}		Standby, I_{SB2} (mA)	
				Typ[1]	Max	Typ[1]	Max
CY7C1049GN18	Industrial	1.65 V–2.2 V	15	–	40	6	8
CY7C1049GN30		2.2 V–3.6 V	10	38	45		
CY7C1049GN		4.5 V–5.5 V	10	38	45		

Note
1. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for a V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Logic Block Diagram – CY7C1049GN



Contents

Pin Configurations

Figure 1. 36-pin SOJ pinout [2]

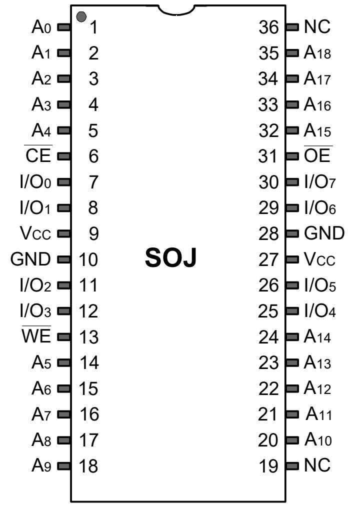
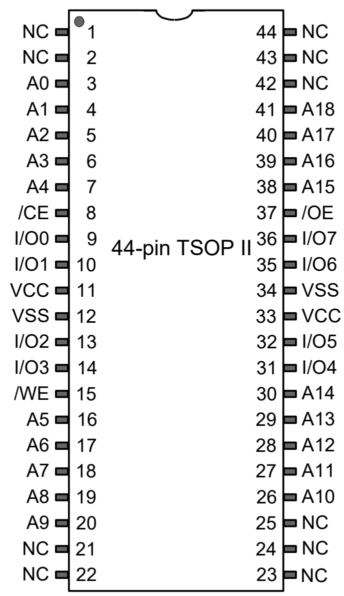


Figure 2. 44-pin TSOP II pinout, Single Chip Enable [2]



Note
2. NC pins are not connected internally to the die.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with power applied .... –55 °C to +125 °C

Supply voltage on V_{CC} relative to GND [3] .... –0.5 to V_{CC} + 0.5 V

DC voltage applied to outputs in HI-Z State [3] .... –0.5 V to V_{CC} + 0.5 V

DC input voltage [3] .... –0.5 V to V_{CC} + 0.5 V

Current into outputs (in LOW state) .... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) .... > 2001 V

Latch-up current .... > 140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description		Test Conditions		10 ns/15 ns			Unit
					Min	Typ [4]	Max	
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OH} = –0.1 mA		1.4	–	–	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –1.0 mA		2	–	–	
		2.7 V to 3.0 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.2	–	–	
		3.0 V to 3.6 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –0.1mA		V_{CC} – 0.5[5]	–	–	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.2	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 2 mA		–	–	0.4	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 8 mA		–	–	0.4	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OL} = 8 mA		–	–	0.4	
V_{IH}	Input HIGH voltage	1.65 V to 2.2 V	–		1.4	–	V_{CC} + 0.2[3]	V
		2.2 V to 2.7 V	–		2	–	V_{CC} + 0.3[3]	
		2.7 V to 3.6 V	–		2	–	V_{CC} + 0.3[3]	
		4.5 V to 5.5 V	–		2	–	V_{CC} + 0.5[3]	
V_{IL}	Input LOW voltage	1.65 V to 2.2 V	–		–0.2[3]	–	0.4	V
		2.2 V to 2.7 V	–		–0.3[3]	–	0.6	
		2.7 V to 3.6 V	–		–0.3[3]	–	0.8	
		4.5 V to 5.5 V	–		–0.5[3]	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–1	–	+1	µA
I_{CC}	Operating supply current		Max V_{CC}, I_{OUT} = 0 mA, CMOS levels	f = 100 MHz	–	38	45	mA
				f = 66.7 MHz	–	–	40	
I_{SB1}	Automatic CE power-down current – TTL inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		–	–	15	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0		–	6	8	mA

Notes

3. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V – 2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2V – 3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V – 5.5 V), T_A = 25 °C.
5. This parameter is guaranteed by design and not tested.

Capacitance

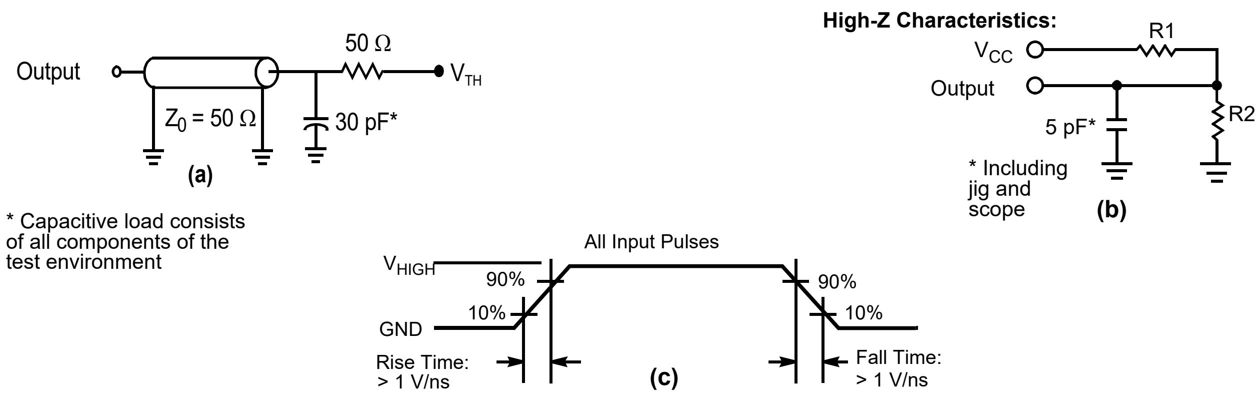
Parameter [6]	Description	Test Conditions	36-pin SOJ	44-pin TSOP II	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	10	pF
C_{OUT}	I/O capacitance		10	10	pF

Thermal Resistance

Parameter [6]	Description	Test Conditions	36-pin SOJ	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.52	68.85	°C/W
Θ_{JC}	Thermal resistance (junction to case)		31.48	15.97	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [7]



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V_{TH}	0.9	1.5	1.5	V
V_{HIGH}	1.8	3	3	V

Notes
6. Tested initially and after any design or process changes that may affect these parameters.
7. Full-device AC operation assumes a 100-µs ramp time from 0 to $V_{CC(min)}$ and a 100-µs wait time after V_{CC} stabilization.

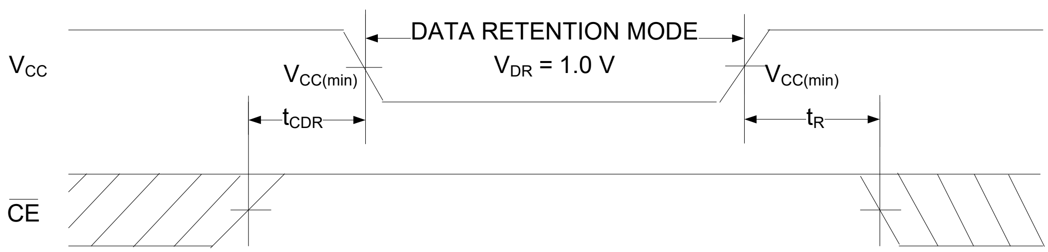
Data Retention Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention		1	–	V
I_{CCDR}	Data retention current	V_{CC} = 1.2 V, $\overline{CE} \geq V_{CC} - 0.2$ V[8], $V_{IN} \geq V_{CC} - 0.2$ V, or $V_{IN} \leq 0.2$ V	–	8	mA
t_{CDR}[9]	Chip deselect to data retention time		0	–	ns
t_R[8, 9]	Operation recovery time	$V_{CC} \geq 2.2$ V	10	–	ns
		$V_{CC} < 2.2$ V	15	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform [8]



Notes
8. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC\,(min)} \geq 100$ µs.
9. These parameters are guaranteed by design.

AC Switching Characteristics

Over the operating range of –40 °C to 85 °C

Parameter [10]	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	10	–	15	–	ns
t_{AA}	Address to data	–	10	–	15	ns
t_{OHA}	Data hold from address change	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data	–	10	–	15	ns
t_{DOE}	$\overline{OE}$ LOW to data	–	4.5	–	8	ns
t_{LZOE}	$\overline{OE}$ LOW to low impedance [11]	0	–	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z [11]	–	5	–	8	ns
t_{LZCE}	$\overline{CE}$ LOW to low impedance [11]	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z [11]	–	5	–	8	ns
t_{PU}	$\overline{CE}$ LOW to power-up [12, 13]	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down [12, 13]	–	10	–	15	ns
Write Cycle [13, 14]						
t_{WC}	Write cycle time	10	–	15	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	7	–	12	–	ns
t_{AW}	Address setup to write end	7	–	12	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7	–	12	–	ns
t_{SD}	Data setup to write end	5	–	8	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low impedance [11]	3	–	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z [11]	–	5	–	8	ns

Notes

10. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading, as shown in part (a) of Figure 3 on page 6, unless specified otherwise.
11. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{LZOE}, t_{LZCE}, and t_{LZWE} are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 3 on page 6. Transition is measured ±200 mV from steady state voltage.
12. These parameters are guaranteed by design and are not tested.
13. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
14. The minimum write cycle pulse width in Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of t_{DS} and t_{HZWE}.

Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled) [15, 16]

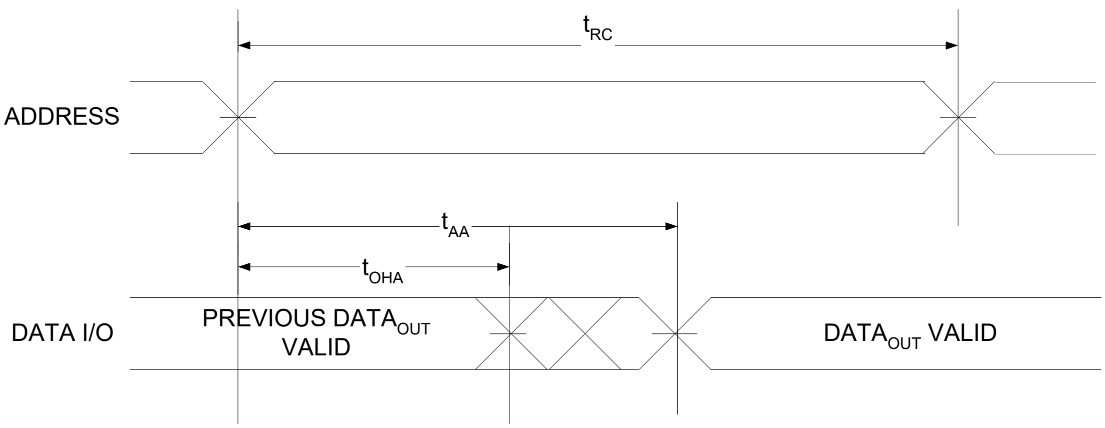
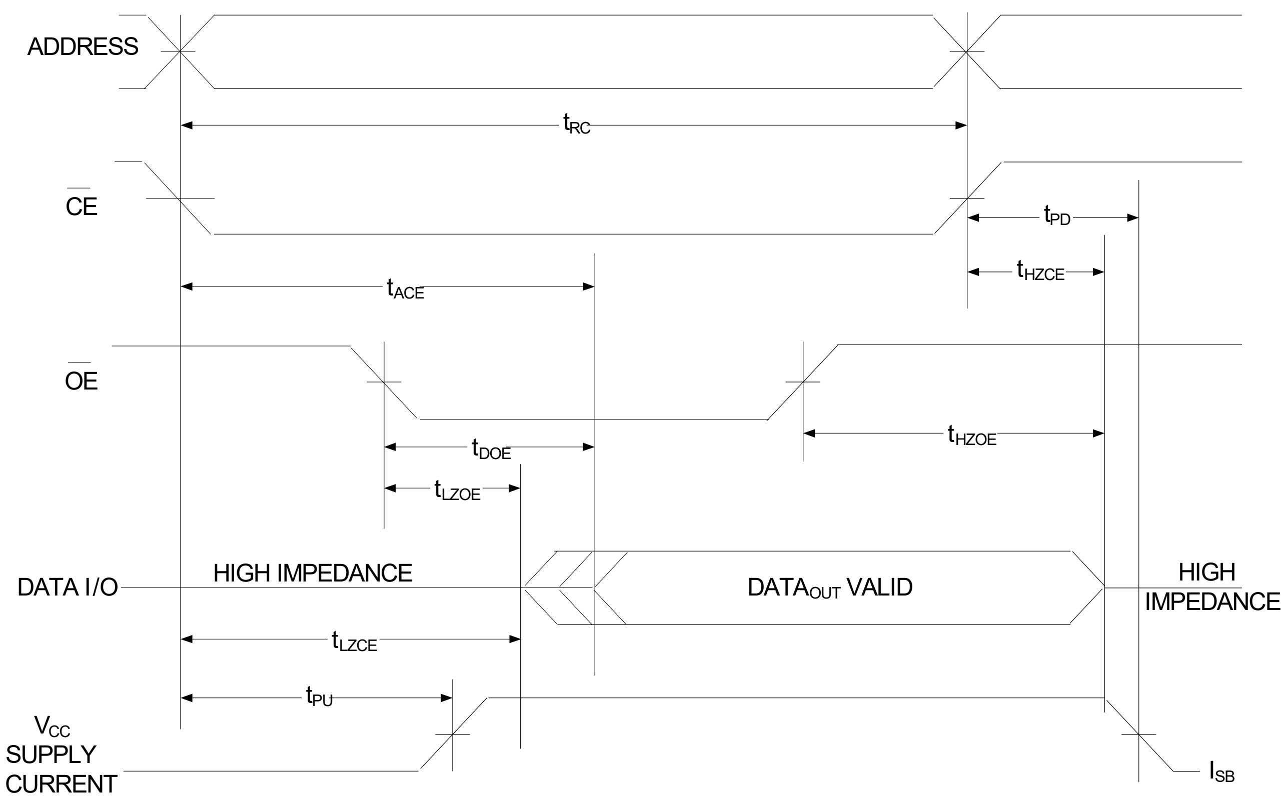


Figure 6. Read Cycle No. 2 (OE Controlled) [15, 16]



Notes
15. WE is HIGH for the read cycle.
16. Address valid prior to or coincident with CE LOW transition.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ($\overline{CE}$ Controlled) [17, 18]

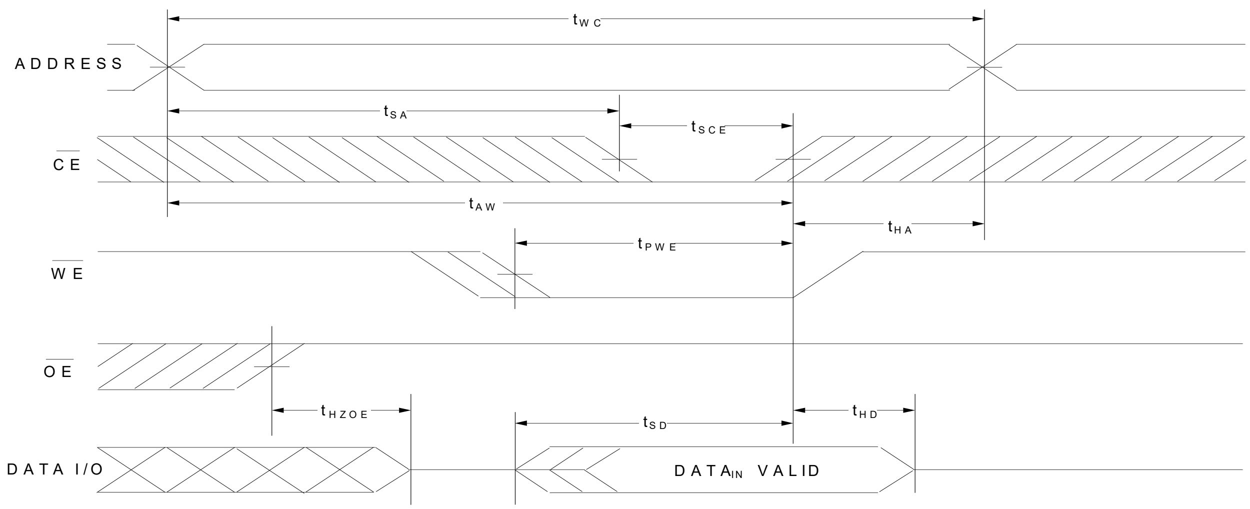
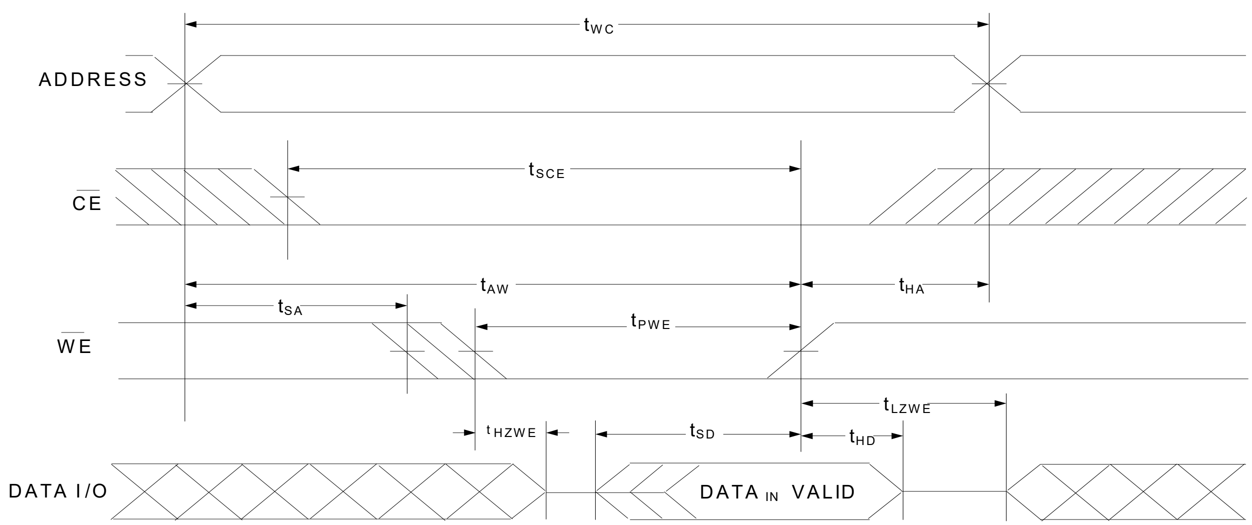


Figure 8. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [17, 18, 19]

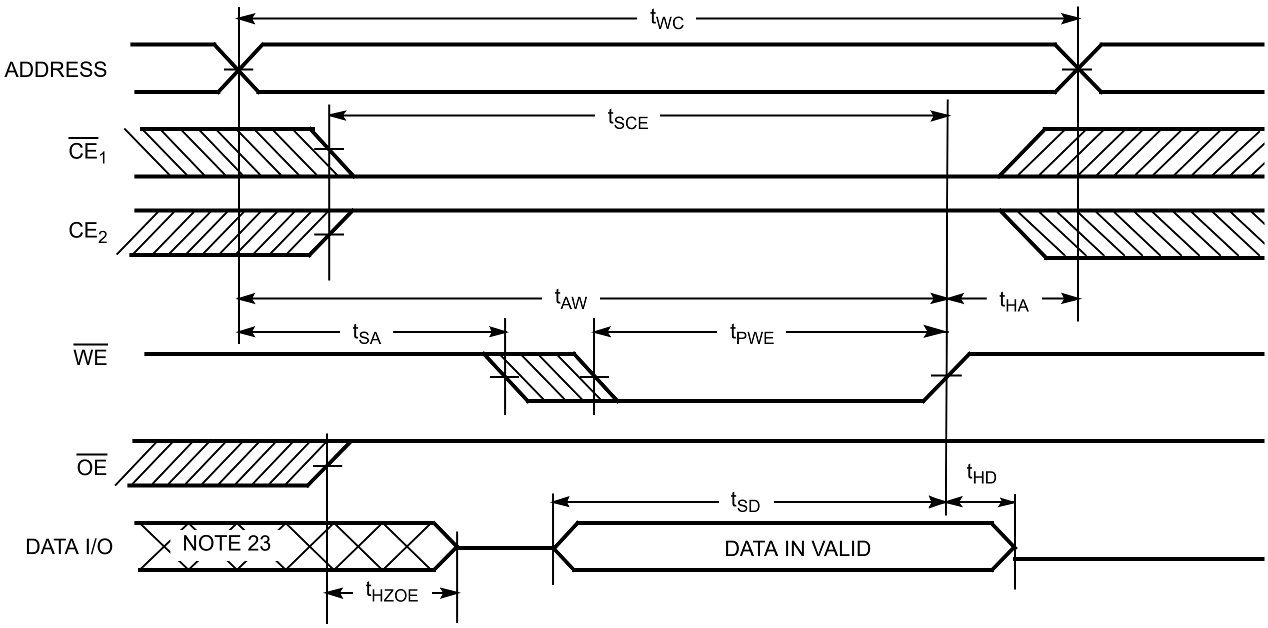


Notes

17. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
18. Data I/O is in HI-Z state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH}.
19. The minimum write cycle pulse width should be equal to sum of t_{SD} and t_{HZWE}.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ($\overline{WE}$ Controlled) [20, 21, 22]



Notes

20. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
21. Data I/O is in HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$.
22. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
23. During this period the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X[24]	X[24]	HI-Z	Power down	Standby (I_{SB})
L	L	H	Data out	Read all bits	Active (I_{CC})
L	X	L	Data in	Write all bits	Active (I_{CC})
L	H	H	HI-Z	Selected, outputs disabled	Active (I_{CC})

Note

24. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.

Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Operating Range
10	2.2 V–3.6 V	CY7C1049GN30-10ZSXI	51-85087	44-pin TSOP II	Industrial
		CY7C1049GN30-10ZSXIT	51-85087	44-pin TSOP II, Tape and Reel	
		CY7C1049GN30-10VXI	51-85090	36-pin Molded SOJ	
		CY7C1049GN30-10VXIT	51-85090	36-pin Molded SOJ, Tape and Reel	
	4.5 V–5.5 V	CY7C1049GN-10VXI	51-85090	36-pin Molded SOJ	
		CY7C1049GN-10VXIT	51-85090	36-pin Molded SOJ, Tape and Reel	

Ordering Code Definitions

CY 7 C 1 04 9 GN XX - XX XX X I X

- X = blank or T
  blank = Bulk; T = Tape and Reel
- Temperature Range: I = Industrial
- Pb-free
- Package Type: XX = ZS or V
  ZS = 44-pin TSOP II; V= 36-pin Molded SOJ
- Speed: XX = 10 ns
- Voltage Range: XX = 30 or blank
  30 = 2.2 V–3.6 V; no character = 4.5 V–5.5 V
- Process Technology: GN = 65 nm
- Data Width: 9 = × 8-bits
- Density: 04 = 4-Mbit
- Family Code: 1 = Fast Asynchronous SRAM family
- Technology Code: C = CMOS
- Marketing Code: 7 = SRAM
- Company ID: CY = Cypress

Package Diagrams

Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087

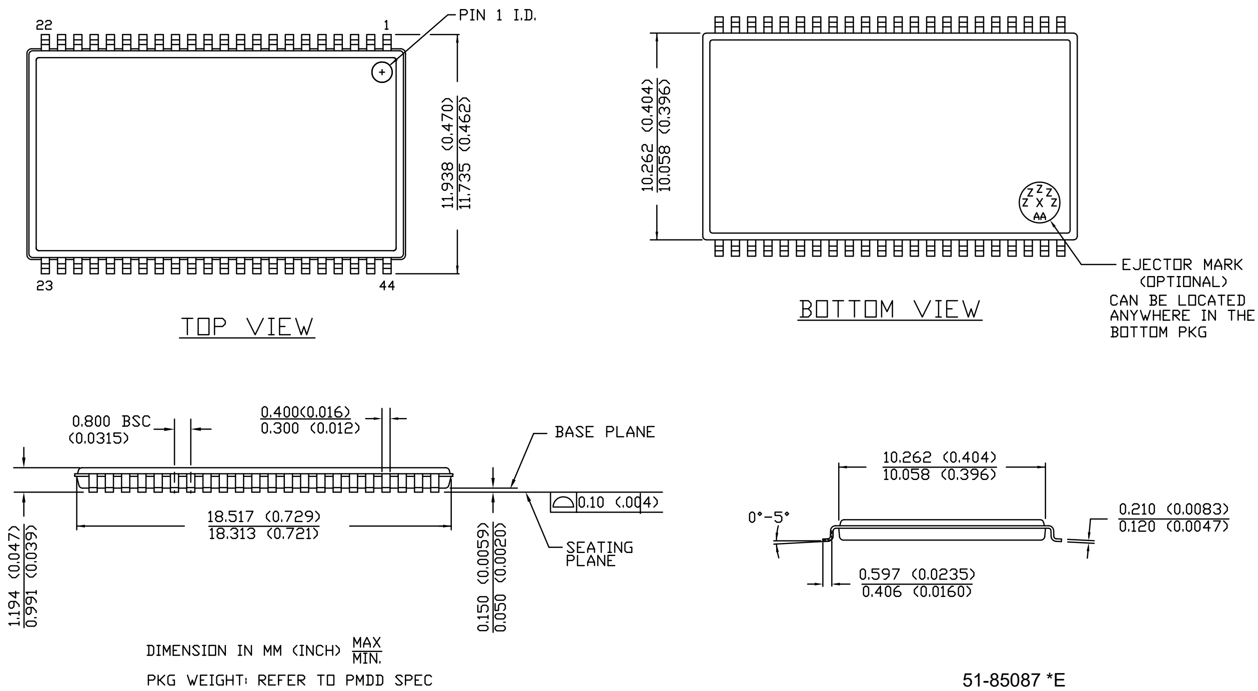
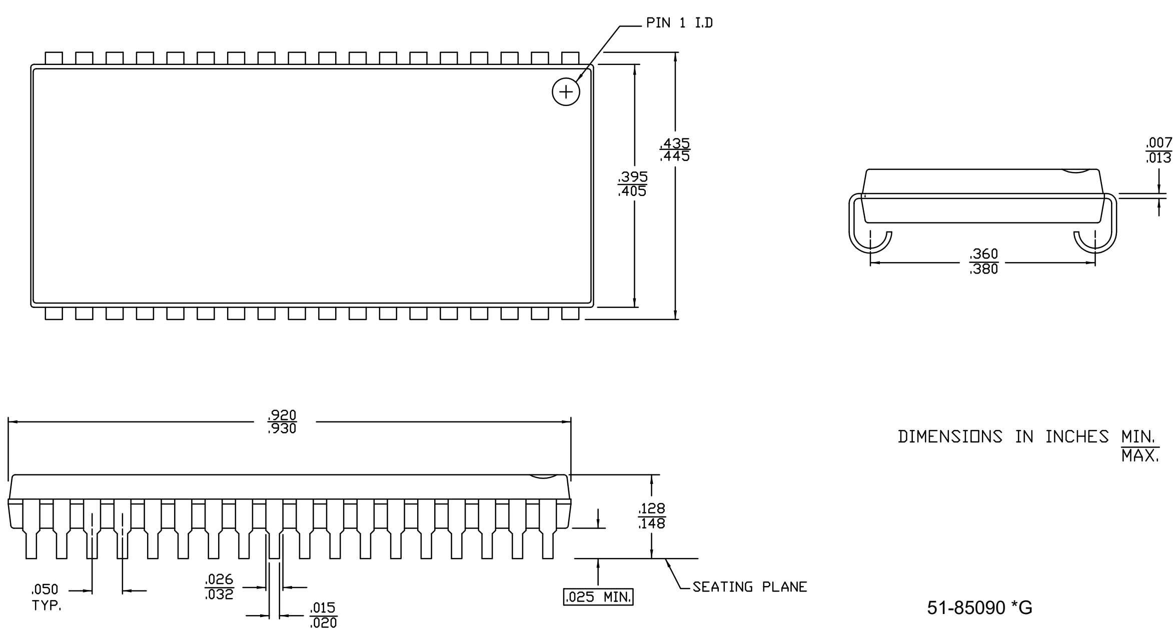


Figure 11. 36-pin SOJ V36.4 (Molded) Package Outline, 51-85090



Acronyms

Acronym	Description
$\overline{BHE}$	byte high enable
$\overline{BLE}$	byte low enable
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
TTL	transistor-transistor logic
VFBGA	very fine-pitch ball grid array
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	Degrees Celsius
MHz	megahertz
µA	microamperes
µs	microseconds
mA	milliamperes
mm	millimeter
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts

Document History Page

Document Title: CY7C1049GN, 4-Mbit (512K words × 8-bit) Static RAM Document Number: 002-10613				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5074703	NILE	01/06/2016	New data sheet.
*A	5082587	NILE	01/12/2016	Updated Logic Block Diagram – CY7C1049GN. Updated Ordering Information: Updated part numbers.
*B	5437570	NILE	09/15/2016	Updated DC Electrical Characteristics: Removed details of V_{OH} parameter corresponding to “2.7 V to 3.6 V” and Test Condition “V_{CC} = Min, I_{OH} = –4.0 mA”. Added details of V_{OH} parameter corresponding to “2.7 V to 3.0 V” and Test Condition “V_{CC} = Min, I_{OH} = –4.0 mA”. Added details of V_{OH} parameter corresponding to “3.0 V to 3.6 V” and Test Condition “V_{CC} = Min, I_{OH} = –4.0 mA”. Changed minimum value of V_{IH} parameter corresponding to “4.5 V to 5.5 V” from 2.2 V to 2 V. Updated Note 3 (Replaced “2 ns” with “20 ns”). Updated Ordering Information: Updated part numbers. Updated to new template.
*C	5966829	NILE	11/14/2017	Updated Switching Waveforms: Updated Figure 6. Updated Figure 7. Updated Figure 8. Updated Figure 9. Updated to new template. Completing Sunset Review.

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