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## Selection Guide

Description	-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	90	mA
Maximum CMOS Standby Current	10	mA

## Pin Configuration

Figure 1. 36-pin SOJ pinout <sup>[1]</sup>

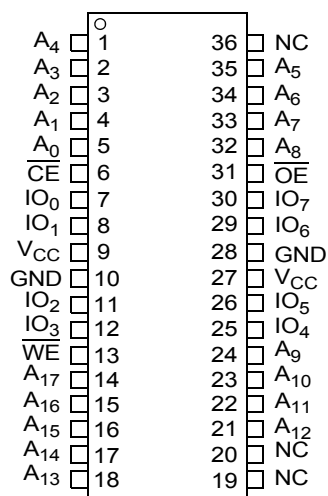
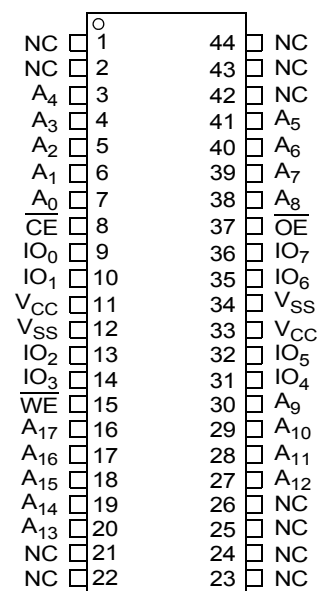


Figure 2. 44-pin TSOP II pinout <sup>[1]</sup>



### Note

1. NC pins are not connected on the die.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65 °C to +150 °C

Ambient Temperature with  
Power Applied ..... -55 °C to +125 °C

Supply Voltage on  
 $V_{CC}$  Relative to GND <sup>[2]</sup> ..... -0.5 V to +4.6 V

DC Voltage Applied to Outputs  
in High Z State <sup>[2]</sup> ..... -0.3 V to  $V_{CC} + 0.3$  V

DC Input Voltage <sup>[2]</sup> ..... -0.3 V to  $V_{CC} + 0.3$  V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage  
(MIL-STD-883, Method 3015) ..... > 2001 V

Latch Up Current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Industrial	-40 °C to +85 °C	3.3V ± 0.3V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10		Unit
				Min	Max	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min; I <sub>OH</sub> = −4.0 mA		2.4	–	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min; I <sub>OL</sub> = 8.0 mA		–	0.4	V
V <sub>IH</sub>	Input HIGH Voltage			2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>			−0.3	0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		−1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled		−1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	100 MHz	–	90	mA
			83 MHz	–	80	
			66 MHz	–	70	
			40 MHz	–	60	
I <sub>SB1</sub>	Automatic CE Power-down Current – TTL Inputs	Max V <sub>CC</sub> , $\overline{\text{CE}} \geq V_{IH}$ ; V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		–	20	mA
I <sub>SB2</sub>	Automatic CE Power-down Current – CMOS Inputs	Max V <sub>CC</sub> , $\overline{\text{CE}} \geq V_{CC} - 0.3 \text{ V}$ , V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3 V, or V <sub>IN</sub> ≤ 0.3 V, f = 0		–	10	mA

### Note

2.  $V_{IL}$  (min.) = -2.0V and  $V_{IH}$  (max.) =  $V_{CC} + 2.0\text{V}$  for pulse durations of less than 20 ns.

## Capacitance

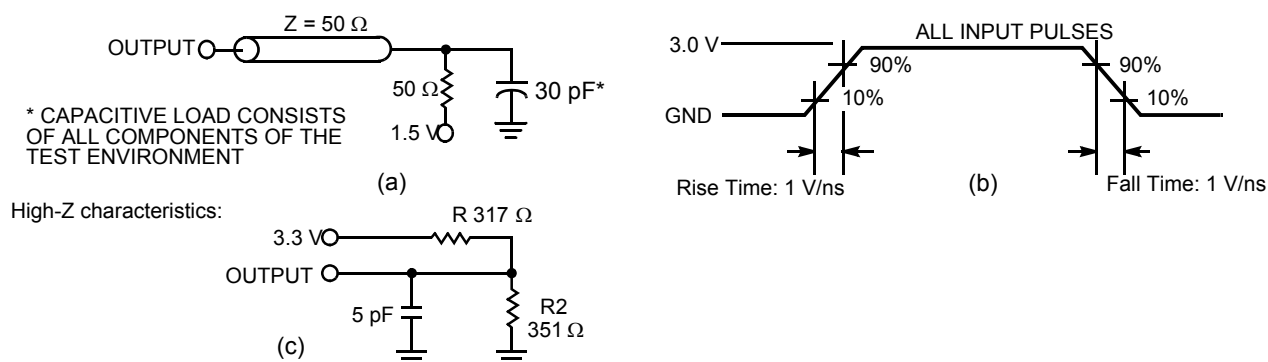
Parameter <sup>[3]</sup>	Description	Test Conditions	36-pin SOJ	44-pin TSOP II	Unit
$C_{IN}$	Input capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 3.3\text{ V}$	8	8	pF
$C_{OUT}$	I/O capacitance		8	8	pF

## Thermal Resistance

Parameter <sup>[3]</sup>	Description	Test Conditions	36-pin SOJ	44-pin TSOP II	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still air, soldered on a $3 \times 4.5$ inch, four layer printed circuit board	59.17	50.66	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		32.63	17.77	$^\circ\text{C/W}$

## AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms <sup>[4]</sup>



### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High Z) are tested using the load conditions shown in Figure 3 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 3 (c).

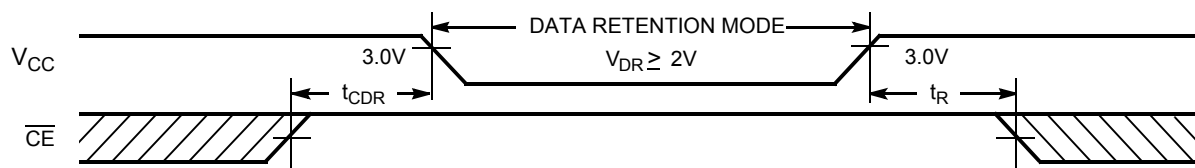
## Data Retention Characteristics

Over the Operating Range

Parameter <sup>[5]</sup>	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2	–	V
$I_{CCDR}$	Data Retention Current	$V_{CC} = V_{DR} = 2.0\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.3\text{ V}$ , $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	–	10	mA
$t_{CDR}$ <sup>[6]</sup>	Chip Deselect to Data Retention Time		0	–	ns
$t_R$ <sup>[7]</sup>	Operation Recovery Time		$t_{RC}$	–	ns

## Data Retention Waveform

Figure 4. Data Retention Waveform



### Notes

- No inputs may exceed  $V_{CC} + 0.3\text{ V}$ .
- Tested initially and after any design or process changes that may affect these parameters.
- Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 50\text{ }\mu\text{s}$  or stable at  $V_{CC(min.)} \geq 50\text{ }\mu\text{s}$ .

## AC Switching Characteristics

Over the Operating Range

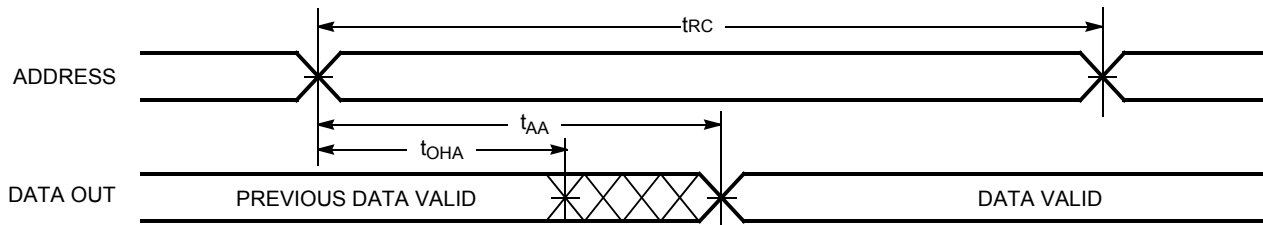
Parameter <sup>[8]</sup>	Description	-10		Unit
		Min	Max	
Read Cycle				
t <sub>power</sub> <sup>[9]</sup>	V <sub>CC</sub> (typical) to the first access	100	–	μs
t <sub>RC</sub>	Read Cycle Time	10	–	ns
t <sub>AA</sub>	Address to Data Valid	–	10	ns
t <sub>OHA</sub>	Data Hold from Address Change	3	–	ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ LOW to Data Valid	–	10	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to Data Valid	–	5	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to Low Z <sup>[10]</sup>	0	–	ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to High Z <sup>[10, 11]</sup>	–	5	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}$ LOW to Low Z <sup>[10]</sup>	3	–	ns
t <sub>HZCE</sub>	$\overline{\text{CE}}$ HIGH to High Z <sup>[10, 11]</sup>	–	5	ns
t <sub>PU</sub>	$\overline{\text{CE}}$ LOW to Power-up	0	–	ns
t <sub>PD</sub>	$\overline{\text{CE}}$ HIGH to Power-down	–	10	ns
Write Cycle <sup>[12, 13]</sup>				
t <sub>WC</sub>	Write Cycle Time	10	–	ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ LOW to Write End	7	–	ns
t <sub>AW</sub>	Address Set-up to Write End	7	–	ns
t <sub>HA</sub>	Address Hold from Write End	0	–	ns
t <sub>SA</sub>	Address Set-up to Write Start	0	–	ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ Pulse Width	7	–	ns
t <sub>SD</sub>	Data Set-up to Write End	5	–	ns
t <sub>HD</sub>	Data Hold from Write End	0	–	ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to Low Z <sup>[10]</sup>	3	–	ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to High Z <sup>[10, 11]</sup>	–	5	ns

### Notes

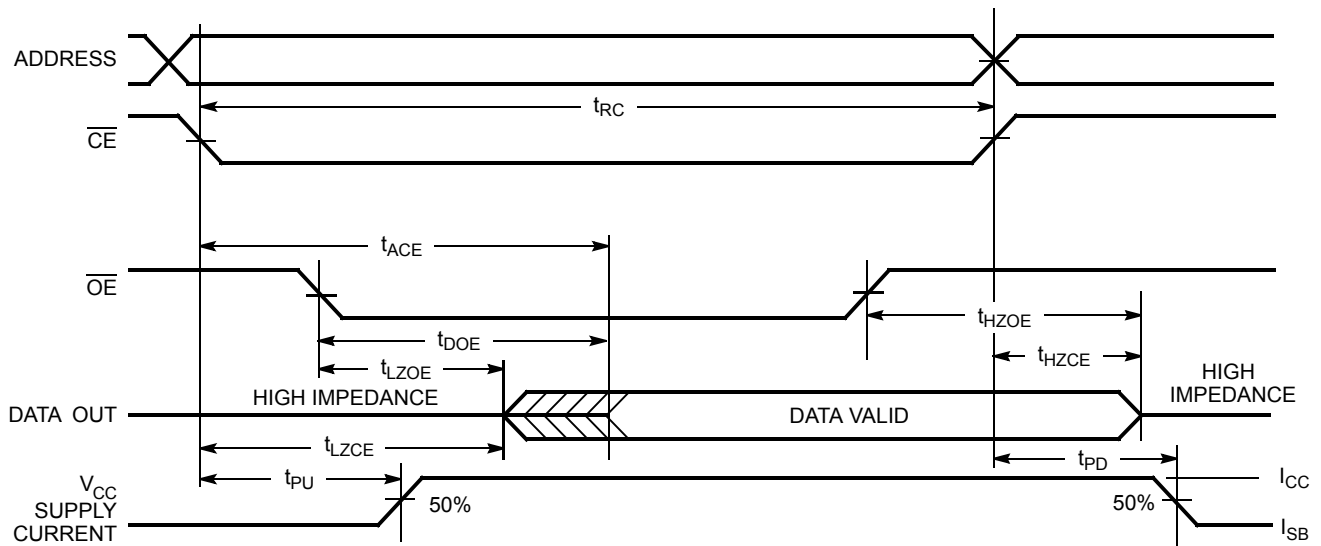
8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
9.  $t_{\text{POWER}}$  gives the minimum amount of time that the power supply should be at stable, typical  $V_{\text{CC}}$  values until the first memory access can be performed.
10. At any given temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any given device.
11.  $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ , and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in part (d) of Figure 3 on page 5. Transition is measured when the outputs enter a high impedance state.
12. The internal Write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW.  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
13. The minimum Write cycle time for Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

## Switching Waveforms

**Figure 5. Read Cycle No. 1** [14, 15]



**Figure 6. Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [15, 16]

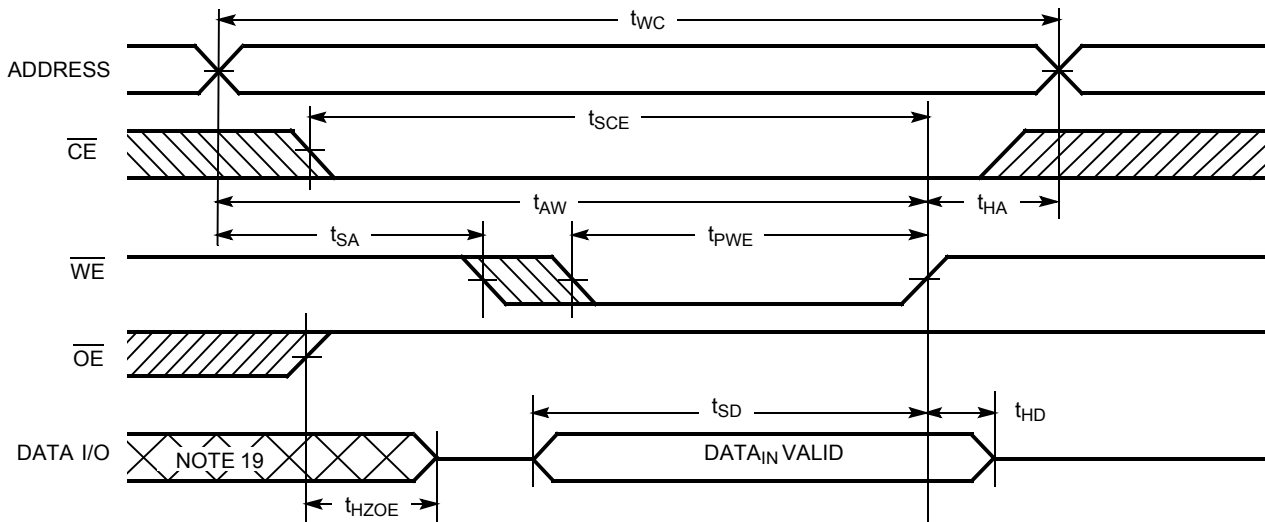


### Notes

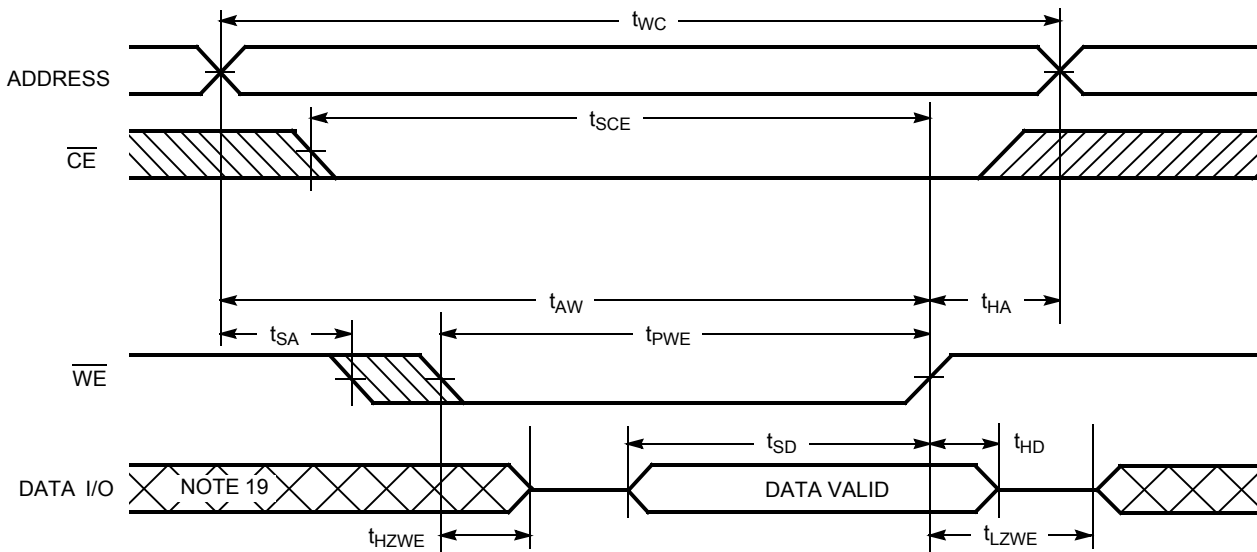
14. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
15.  $\overline{WE}$  is HIGH for read cycle.
16. Address valid before or similar to  $\overline{CE}$  transition LOW.

## Switching Waveforms (continued)

**Figure 7. Write Cycle No. 1 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)** <sup>[17, 18]</sup>



**Figure 8. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)** <sup>[18]</sup>



### Notes

17. Data IO is high impedance if  $\overline{OE} = V_{IH}$ .
18. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high impedance state.
19. During this period, the I/Os are in output state and input signals should not be applied.



## Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	X	X	High Z	High Z	Power Down	Standby (I <sub>SB</sub> )
L	L	H	Data Out	Data Out	Read All Bits	Active (I <sub>CC</sub> )
L	X	L	Data In	Data In	Write All Bits	Active (I <sub>CC</sub> )
L	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

## Ordering Information

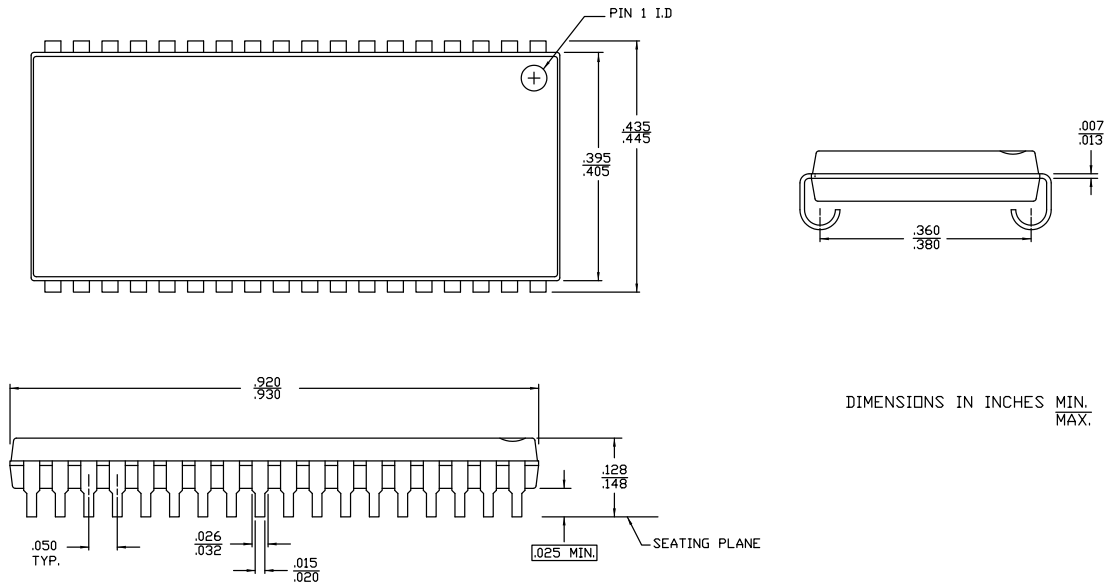
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1010DV33-10VXI	51-85090	36-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1010DV33-10ZSXI	51-85087	44-pin TSOP II (Pb-free)	

## Ordering Code Definitions

CY	7	C	1	01	0	D	V33	-	10	XX	X	I	
													Temperature Range: I = Industrial
													Pb-free
													Package Type: XX = V or ZS V = 36-pin (400-Mil) Molded SOJ ZS = 44-pin TSOP II
													Speed: 10 ns
													V33 = Voltage range (3 V to 3.6 V)
													Process Technology: D = C9, 90 nm Technology
													Data Width: 0 = 8-bits
													Density: 01 = 2-Mbit
													Family Code: 1 = Fast Asynchronous SRAM family
													Technology Code: C = CMOS
													Marketing Code: 7 = SRAM
													Company ID: CY = Cypress

## Package Diagrams

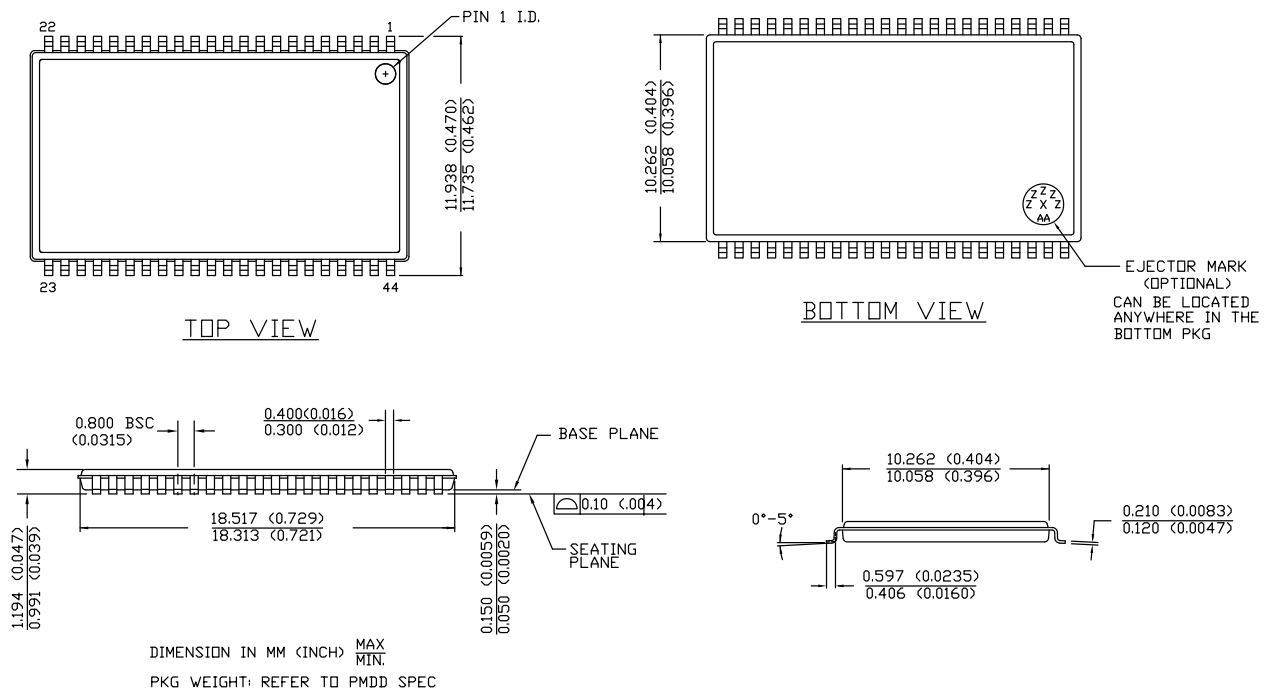
Figure 9. 36-pin SOJ V36.4 (Molded) Package Outline, 51-85090



51-85090 \*F

Package Diagrams (continued)

Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087



## Acronyms

Acronym	Description
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SOJ	Small Outline J-lead
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C1010DV33, 2-Mbit (256 K × 8) Static RAM Document Number: 001-00062				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	342195	See ECN	PCI	New data sheet.
*A	459073	See ECN	NXR	Converted Preliminary to Final. Removed Commercial Operating Range from product offering. Removed -8 ns and -12 speed bin Removed the Pin definitions table. Modified Maximum Ratings for DC input voltage from -0.5V to -0.3V and $V_{CC} + 0.5V$ to $V_{CC} + 0.3V$ Changed $I_{CC}$ max from 65 mA to 90 mA Changed the description of $I_{IX}$ from "Input Load Current" to "Input Leakage Current" Updated the Thermal Resistance table. Updated footnote #7 on High-Z parameter measurement Added footnote #12 Updated the Ordering Information and replaced Package Name column with Package Diagram in the Ordering Information table.
*B	2602853	11/07/08	VKN / PYRS	Added 36-pin SOJ package and its related information
*C	3059211	10/14/2010	PRAS	Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagrams</a> .
*D	3272897	06/07/2011	AJU	Updated <a href="#">Functional Description</a> (Removed "Refer to the Cypress application note AN1064, SRAM System Guidelines for best practice recommendations."). Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated in new template.
*E	4207615	12/02/2013	MEMJ	Updated <a href="#">Package Diagrams</a> : spec 51-85090 – Changed revision from *E to *F. spec 51-85087 – Changed revision from *C to *E. Updated in new template. Completing Sunset Review.
*F	4574311	11/19/2014	MEMJ	Added related documentation hyperlink in page 1.

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