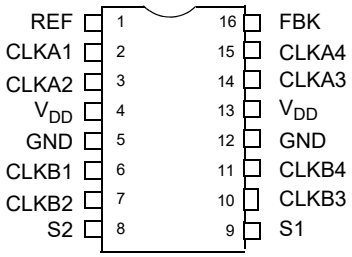
Contents

Pinouts

Figure 1. 16-pin SOIC pinout (Top View)



Pin Definitions

Pin	Signal	Description
1	REF [1]	Input reference frequency, 5 V tolerant input
2	CLKA1 [2]	Clock output, Bank A
3	CLKA2 [2]	Clock output, Bank A
4	V_{DD}	3.3 V supply
5	GND	Ground
6	CLKB1 [2]	Clock output, Bank B
7	CLKB2 [2]	Clock output, Bank B
8	S2 [3]	Select input, bit 2
9	S1 [3]	Select input, bit 1
10	CLKB3 [2]	Clock output, Bank B
11	CLKB4 [2]	Clock output, Bank B
12	GND	Ground
13	V_{DD}	3.3 V supply
14	CLKA3 [2]	Clock output, Bank A
15	CLKA4 [2]	Clock output, Bank A
16	FBK	PLL feedback input

Notes
1. Weak pull-down.
2. Weak pull-down on all outputs.
3. Weak pull-ups on these inputs.

Functional Overview

Select Input Decoding

S2	S1	CLOCK A1–A4	CLOCK B1–B4	Output Source	PLL Shutdown
0	0	Tristate	Tristate	PLL	Y
0	1	Driven	Tristate	PLL	N
1	0	Driven	Driven	Reference	Y
1	1	Driven	Driven	PLL	N

Available CY23S08 Configurations

Device	Feedback From	Bank A Frequency	Bank B Frequency
CY23S08-1	Bank A or Bank B	Reference	Reference
CY23S08-1H	Bank A or Bank B	Reference	Reference
CY23S08-2	Bank A	Reference	Reference/2
CY23S08-2H	Bank A	Reference	Reference/2
CY23S08-2	Bank B	2 X Reference	Reference
CY23S08-2H	Bank B	2 X Reference	Reference
CY23S08-4	Bank A or Bank B	2 X Reference	2 X Reference

Spread Aware

Many systems designed now use the Spread Spectrum frequency timing generation (SSFTG) technology. Cypress is one of the pioneers of SSFTG development, and designed this product so as not to filter off the Spread Spectrum feature of the Reference input, assuming it exists. When a zero delay buffer does not pass through the SS feature, the result is a significant amount of tracking skew which may cause problems in systems requiring synchronization.

For more details on Spread Spectrum timing technology, see Cypress's application note *EMI Suppression Techniques with Spread Spectrum Frequency Timing Generator (SSFTG) ICs*.

Note
4. Output phase is indeterminant (0° or 180° from input clock). If phase integrity is required, use the CY23S08-2.

Maximum Ratings

Supply voltage to ground potential .....–0.5 V to +7.0 V
DC input voltage (except Ref) .....–0.5 V to V_{DD} + 0.5 V
DC input voltage REF .....–0.5 to 7 V

Storage temperature .....–65 °C to +150 °C
Max soldering temperature (10 sec.) ..... 260 °C
Junction temperature ..... 150 °C
Static discharge voltage
(per MIL-STD-883, Method 3015) .....>2000 V

Operating Conditions

Parameter [5]	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.0	3.6	V
T_A	Ambient operating temperature, Commercial	0	70	°C
	Ambient operating temperature, Industrial	–40	85	°C
C_L	Load capacitance, below 100 MHz	–	30	pF
	Load capacitance, from 100 MHz to 140 MHz	–	15	pF
C_{IN}	Input capacitance [6]	–	7	pF

Electrical Characteristics

For CY23S08SXC-xx Commercial Temperature Devices

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input Low voltage		–	0.8	V
V_{IH}	Input High voltage		2.0	–	V
I_{IL}	Input Low current	V_{IN} = 0 V	–	50.0	µA
I_{IH}	Input High current	V_{IN} = V_{DD}	–	100.0	µA
V_{OL}	Output Low voltage[7]	I_{OL} = 8 mA (-1, -2, -4) I_{OL} = 12 mA (-1H, -2H)	–	0.4	V
V_{OH}	Output High voltage[7]	I_{OH} = –8 mA (-1, -2, -4) I_{OH} = –12 mA (-1H, -2H)	2.4	–	V
I_{DD} (PD mode)	Power-down supply current	REF = 0 MHz	–	12.0	µA
I_{DD}	Supply current	Unloaded outputs, 100-MHz REF; Select inputs at V_{DD} or GND	–	45.0	mA
			–	70.0 (-1H, -2H)	mA
		Unloaded outputs, 66 MHz REF (-1, -2, -4)	–	32.0	mA
		Unloaded outputs, 33 MHz REF (-1, -2, -4)	–	18.0	mA

Thermal Resistance

Parameter [8]	Description	Test Conditions	16-pin SOIC	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	108	°C/W
θ_{JC}	Thermal resistance (junction to case)		37	°C/W

Notes
5. Multiple Supplies: The voltage on any input or IO pin cannot exceed the power pin during power up. Power supply sequencing is NOT required.
6. Applies to both Ref Clock and FBK.
7. Parameter is guaranteed by design and characterization. Not 100% tested in production.
8. These parameters are guaranteed by design and are not tested.

Switching Characteristics

For CY23S08SXC-xx Commercial Temperature Devices

Parameter [9]	Description	Test Conditions	Min	Typ	Max	Unit
t1	Output frequency	30 pF load, –1, –1H, –2 devices	10	–	100	MHz
t1	Output frequency	30 pF load, –4 devices	15	–	100	MHz
t1	Output frequency	20 pF load, –1H device	10	–	133.3	MHz
t1	Output frequency	15 pF load, –1, –2 devices	10	–	140.0	MHz
t1	Output frequency	15 pF load, –4 devices	15	–	140.0	MHz
	Duty cycle[10] = $t_2 \div t_1$ (-1, -2, -4, -1H, -2H)	Measured at $V_{DD}/2$, F_{OUT} = 66.66 MHz, 30-pF load	40.0	50.0	60.0	%
	Duty Cycle[10] = $t_2 \div t_1$ (-1, -2, -4, -1H, -2H)	Measured at $V_{DD}/2$, F_{OUT} < 66.66 MHz, 15 pF load	45.0	50.0	55.0	%
t3	Rise Time[10] (-1, -2, -4)	Measured between 0.8 V and 2.0 V, 30 pF load	–	–	2.20	ns
t3	Rise Time[10] (-1, -2, -4)	Measured between 0.8 V and 2.0 V, 15 pF load	–	–	1.50	ns
t3	Rise Time[10] (-1H, -2H)	Measured between 0.8 V and 2.0 V, 30 pF load	–	–	1.50	ns
t_4	Fall Time[10] (-1, -2, -4)	Measured between 0.8 V and 2.0 V, 30 pF load	–	–	2.20	ns
t_4	Fall Time[10] (-1, -2, -4)	Measured between 0.8 V and 2.0 V, 15 pF load	–	–	1.50	ns
t_4	Fall Time[10] (-1H, 2H)	Measured between 0.8 V and 2.0 V, 30 pF load	–	–	1.25	ns
t_5	Output-to-output skew on same Bank (-1) [10]	All outputs equally loaded	–	45	200	ps
	Output-to-output skew on same Bank (-1H, -2, -2H) [10]	All outputs equally loaded	–	105	150	ps
	Output-to-output skew on same Bank (-4) [10]	All outputs equally loaded	–	70	100	ps
	Output-to-output skew (-1H, -2H)	All outputs equally loaded	–	–	200	ps
	Output Bank A to output Bank B Skew (-1, -2)	All outputs equally loaded	–	–	300	ps
	Output Bank A to output Bank B Skew (-4)	All outputs equally loaded	–	–	215	ps
	Output Bank A to output Bank B Skew (-1H)	All outputs equally loaded	–	–	250	ps

Notes
9. All parameters are specified with loaded outputs.
10. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics (continued)

For CY23S08SXC-xx Commercial Temperature Devices

Parameter [9]	Description	Test Conditions	Min	Typ	Max	Unit
t_6	Delay, REF rising edge to FBK rising edge [11]	Measured at $V_{DD}/2$	–250	–	+275	ps
t_7	Device-to-device skew[11]	Measured at $V_{DD}/2$ on the FBK pins of devices	–	–	700	ps
t_8	Output slew rate [11]	Measured between 0.8 V and 2.0 V on -1H, -2H device using Test Circuit #2	1	–	–	V/ns
t_J	Cycle-to-cycle jitter [11] (-1, -1H)	Measured at 66.67 MHz, loaded outputs, 15, 30 pF loads; 133 MHz, 15 pF load	–	65	125	ps
	Cycle-to-cycle jitter [11] (-2)	Measured at 66.67 MHz, loaded outputs, 15 pF load	–	85	300	ps
	Cycle-to-cycle jitter [11] (-2)	Measured at 66.67 MHz, loaded outputs, 30 pF load	–	–	400	ps
t_J	Cycle-to-cycle jitter [11] (-4)	Measured at 66.67 MHz, loaded outputs, 15, 30 pF loads	–	–	200	ps
t_{LOCK}	PLL lock time [11]	Stable power supply, valid clocks presented on REF and FBK pins	–	–	1.0	ms

Note
11. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Waveforms

Figure 2. Duty Cycle Timing

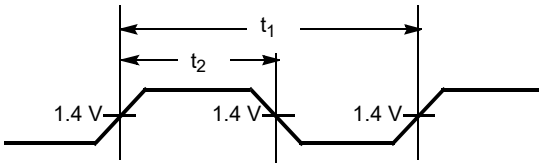


Figure 3. All Outputs Rise and Fall Time

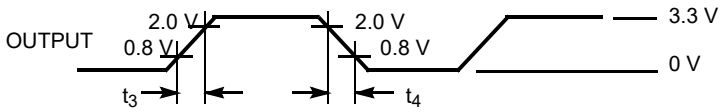


Figure 4. Output-Output Skew

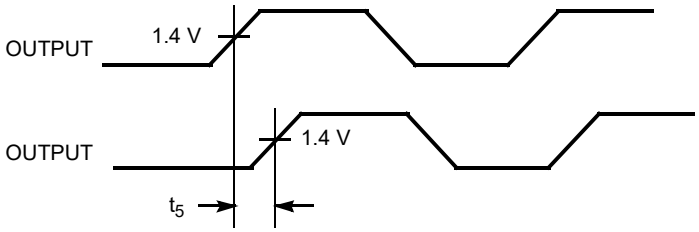


Figure 5. Input-Output Propagation Delay

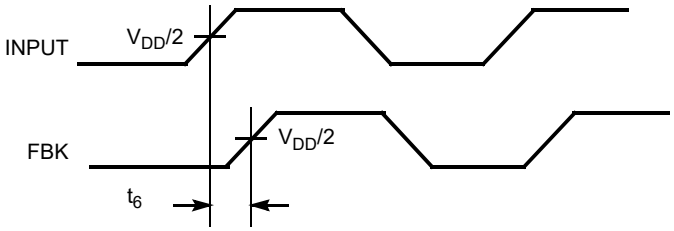
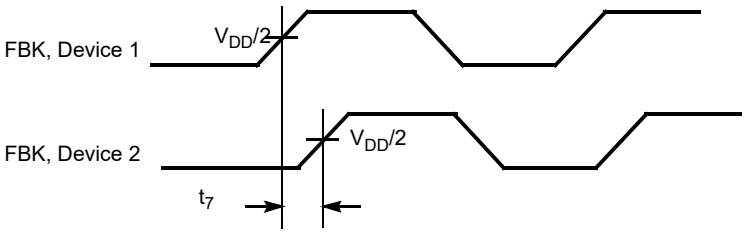
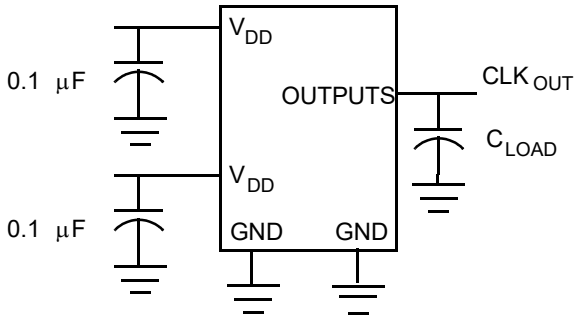


Figure 6. Device-Device Skew



Test Circuits

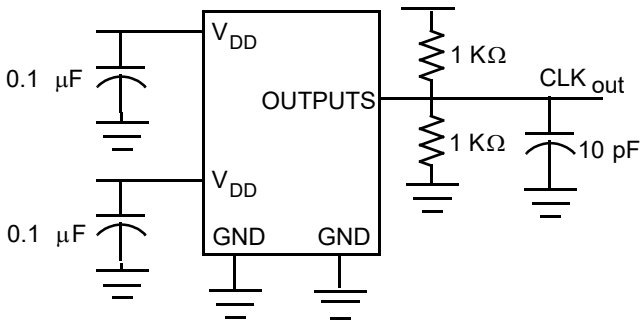
Figure 7. Test Circuit 1



Test Circuit for all parameters except t_8

Figure 8. Test Circuit 2

Test Circuit # 2

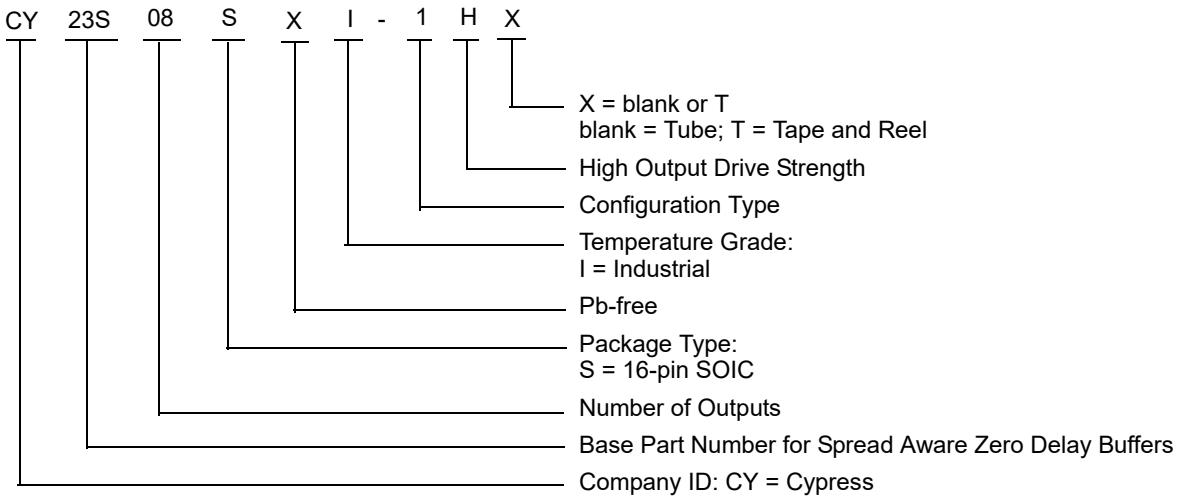


Test Circuit for t_8, Output slew rate on –1H device

Ordering Information

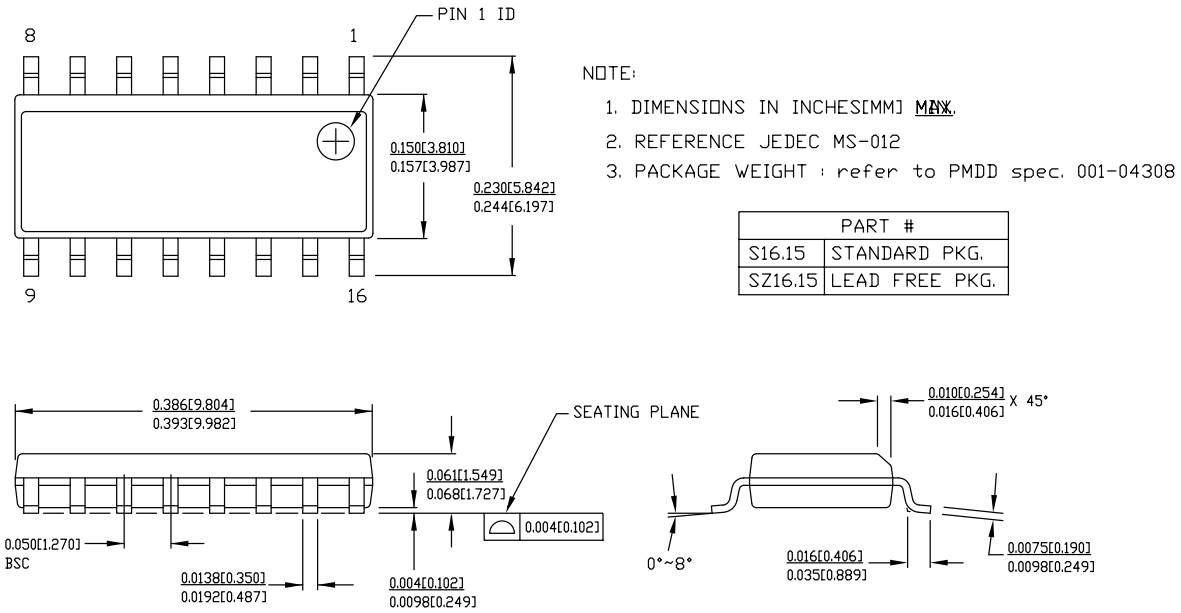
Ordering Code	Package Type	Operating Range
Pb-free		
CY23S08SXI-1H	16-pin SOIC (150 Mils)	Industrial (–40 °C to 85 °C)
CY23S08SXI-1HT	16-pin SOIC (150 Mils) – Tape and Reel	Industrial (–40 °C to 85 °C)

Ordering Code Definitions



Package Drawings and Dimensions

Figure 9. 16-pin SOIC (150 Mils) S16.15/SZ16.15 Package Outline, 51-85068



51-85068 *E

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
OE	Output Enable
PLL	Phase-Locked Loop
RMS	Root Mean Square
SOIC	Small Outline Integrated Circuit
SSFTG	Spread Spectrum Frequency Timing Generation
TSSOP	Thin Shrunk Small Outline Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY23S08, 3.3 V Zero Delay Buffer Document Number: 38-07265				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110530	SZV	12/02/2001	Change from Spec number: 38-01107 to 38-07265.
*A	122863	RBI	12/20/2002	Added power up requirements to operating conditions information.
*B	130951	RGL	11/26/2003	Corrected the Switching Characteristics parameters to reflect the W152 device and new characterization.
*C	204201	RGL	02/11/2004	Corrected the Block Diagram
*D	231100	RGL	06/03/2004	Fixed Typo in table 2.
*E	378878	RGL	06/09/2005	Removed “Preliminary” Added Industrial Temp and Pb Free Devices Added typical char data
*F	391564	RGL	08/11/2005	Changed output-to-output skew typical value from 90ps to 45ps Added cycle-to-cycle jitter (-2) typical value of 85ps
*G	1442823	WWZ / AESA	09/05/2007	Updated ordering info with status update. Added new Pb-free part numbers.
*H	2600345	WWZ / PYRS	11/03/2008	Updated max frequency number from 133 MHz to 140 MHz on page 1 and page 4 load capacitance description
*I	2658081	KVM / PYRS	02/16/2009	Removed references to SOIC in the pinout drawing and pin description table on page 2. Corrected TSSOP package size (from 150 mil to 4.4 mm) in Ordering Information Table. Added CY23S08ZXC-1HT to the Ordering Information Table. Updated Ordering Information Table to remove obsolete devices. Removed Status column.
*J	2761988	KVM	09/10/2009	Added industrial temperature range to Operating Conditions table. Added numerical values to Operating Range column of Ordering Information table. Removed references to –3 device.
*K	2904767	CXQ	04/05/2010	Updated Ordering Information: Updated part numbers. Updated Package Drawings and Dimensions: spec 51-85068 – Changed revision from *B to *C. spec 51-85091 – Changed revision from *A to *B.
*L	3011498	CXQ	08/19/2010	Added Ordering Code Definitions under Ordering Information. Updated Package Drawings and Dimensions: spec 51-85091 – Changed revision from *B to *C. Added Acronyms and Units of Measure. Completing Sunset Review.
*M	3056348	CXQ	10/12/2010	Updated Ordering Information: Updated part numbers. Updated Package Drawings and Dimensions: Removed spec 51-85091 *C.
*N	3211161	CXQ	03/30/2011	Updated Ordering Information: Updated part numbers.
*O	4201668	CINM	11/25/2013	Updated Package Drawings and Dimensions: spec 51-85068 – Changed revision from *C to *E. Updated to new template.
*P	4580603	TAVA	11/26/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.

Document History Page (continued)

Document Title: CY23S08, 3.3 V Zero Delay Buffer Document Number: 38-07265				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*Q	5274556	PSR	05/17/2016	Added Thermal Resistance. Updated to new template.
*R	5554784	TAVA	12/15/2016	Updated to new template. Completing Sunset Review.
*S	6013635	PAWK	01/04/2018	Updated to new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

Cypress Developer Community

Community | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support