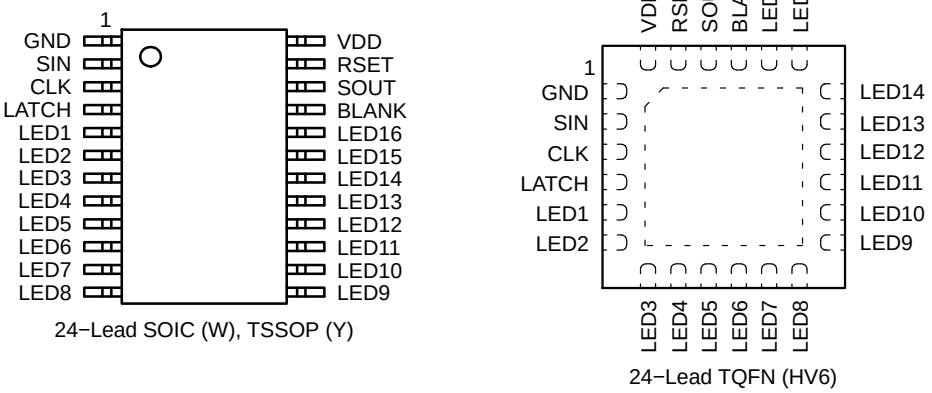
PIN CONNECTIONS



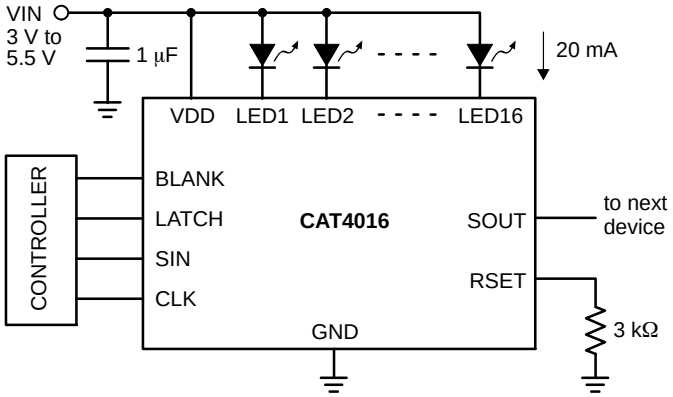


Figure 1. Typical Application Circuit

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
V_{DD} Supply Voltage	6	V
Logic input/output voltage (SIN, SOUT, CLK, BLANK, LATCH)	−0.3 V to V_{DD}+0.3 V	V
LEDn voltage, channel off LEDn voltage, channel on	6 2.5	V
DC output current on LED1 to LED16	150	mA
Storage Temperature Range	−55 to +160	°C
Junction Temperature Range	−40 to +150	°C
Lead Soldering Temperature (10 sec.)	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. RECOMMENDED OPERATING CONDITIONS

Parameter		Range	Unit
V_{DD}		3.0 to 5.5	V
Voltage applied to LED1 to LED16, channel off Voltage applied to LED1 to LED16, channel on		0.4 to 5.5 0.4 to 2.0	V
LED current RSET control range		up to 100	mA
Ambient Temperature Range	CAT4016 CAV4016	−40 to +85 −40 to +125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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Table 3. ELECTRICAL OPERATING CHARACTERISTICS
(V_{DD} = 5.0 V, T_{AMB} = 25°C, over recommended operating conditions unless specified otherwise.)

Symbol	Name	Conditions	Min	Typ	Max	Units
DC CHARACTERISTICS						
$I_{LED-ACC}$	LED Current (any channel)	V_{LED} = 1 V, R_{SET} = 3 kΩ	18	20	22	mA
		V_{LED} = 1 V, R_{SET} = 1.5 kΩ	36	40	44	
		V_{LED} = 1 V, R_{SET} = 750 Ω		80		
$I_{LED-MAT}$	LED Current Matching (I_{LED} − I_{LEDAVR}) / I_{LEDAVR}	V_{LED} = 1 V, R_{SET} = 3 kΩ		±1.5		%
		V_{LED} = 1 V, R_{SET} = 1.5 kΩ	−6.0	±1.5	+6.0	
		V_{LED} = 1 V, R_{SET} = 750 Ω		±2.0		
ΔI_{VDD}	LED current regulation vs. V_{DD}	V_{DD} within 4.5 V and 5.5 V LED current 30 mA		±0.1		% / V
ΔI_{VLED}	LED current regulation vs. V_{LED}	V_{LED} within 1 V and 3 V LED current 30 mA		±0.05		% / V
I_{DDOFF}	Supply Current (all outputs off)	R_{SET} = 3 kΩ		3	8	mA
		R_{SET} = 750 Ω		8.5		
I_{DDON}	Supply Current (all outputs on)	R_{SET} = 3 kΩ		4	9	mA
		R_{SET} = 750 Ω		10		
I_{LKG}	LEDn output Leakage	V_{LED} = 5 V, outputs off	−1		1	μA
R_{LATCH}	LATCH Pull−down Resistance		100	180	300	kΩ
R_{BLANK}	BLANK Pull−up Resistance		100	180	300	kΩ
V_{IH} V_{IL}	Logic high input voltage Logic low input voltage		0.7xV_{DD}		 0.3xV_{DD}	V
V_{HYS}	Logic input hysteresis voltage			0.1xV_{DD}		V
I_{IL}	Logic Input leakage current (CLK, SIN)	V_I = V_{DD} or GND	−5	0	5	μA
V_{OH} V_{OL}	SOUT logic high output voltage SOUT logic low output voltage	I_{OH} = −1 mA I_{OL} = 1 mA	V_{CC}−0.3 V		 0.3	V
V_{RSET}	RSET Regulated Voltage		1.17	1.20	1.23	V
T_{SD}	Thermal Shutdown			160		°C
T_{HYST}	Thermal Hysteresis			20		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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Table 4. TIMING CHARACTERISTICS
(For 3.0 V ≤ V_{DD} ≤ 5.5 V, T_{AMB} = 25°C, unless specified otherwise.)

Symbol	Name	Conditions	Min (Note 1)	Typ (Note 2)	Max (Note 1)	Units
CLK						
f_{clk}	CLK Clock Frequency				25	MHz
t_{cwh}	CLK Pulse Width High		20			ns
t_{cwl}	CLK Pulse Width Low		20			ns
SIN						
t_{ssu}	Setup time SIN to CLK		4			ns
t_{sh}	Hold time SIN to CLK		4			ns
LATCH						
t_{lwh}	LATCH Pulse width		20			ns
T_{lh}	Hold time LATCH to CLK		4			ns
T_{lsu}	Setup time LATCH to CLK	Channel Stagger Delay	800			ns
LEDn						
t_{ld}	LED1 Propagation delay	LATCH to LED1 on LATCH to LED1 off		40 –	300 1000	ns
t_{ls}	LED Propagation delay stagger	LED(n) to LED(n+1)		17	40	ns
t_{lst}	LED Propagation delay stagger total	LED1 to LED16		250		ns
t_{bd}	BLANK Propagation delay	BLANK to LED(n) on BLANK to LED(n) off		60 –	300 800	ns
t_{lr}	LED rise time (10% to 90%)	Pull−up resistor = 50 Ω to 3.0 V		40	200	ns
t_{lf}	LED fall time (90% to 10%)	Pull−up resistor = 50 Ω to 3.0 V		30	250	ns
SOUT						
t_{or}	SOUT rise time (10% to 90%)	C_L = 15 pF		5		ns
t_{of}	SOUT fall time (90% to 10%)	C_L = 15 pF		5		ns
t_{od}	Propagation delay time SOUT	CLK to SOUT	8	15	25	ns

1. All min and max values are guaranteed by design.
2. V_{DD} = 5 V, LED current 30 mA.

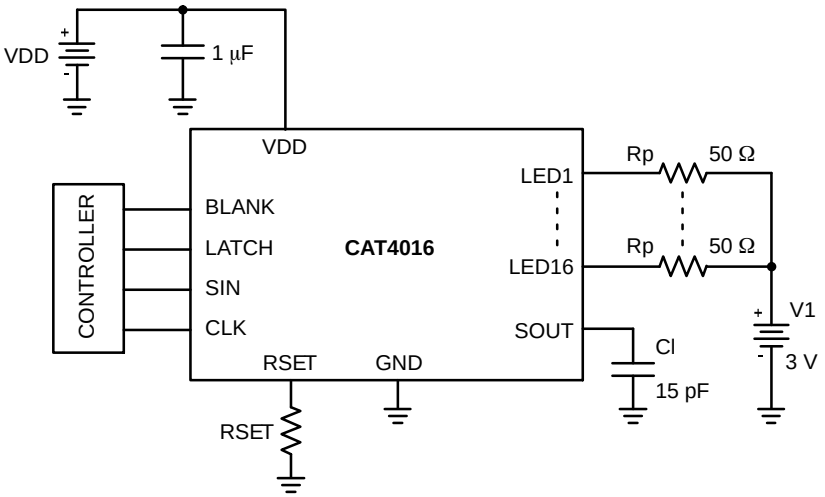

Figure 2. Test Circuit for AC Characteristics

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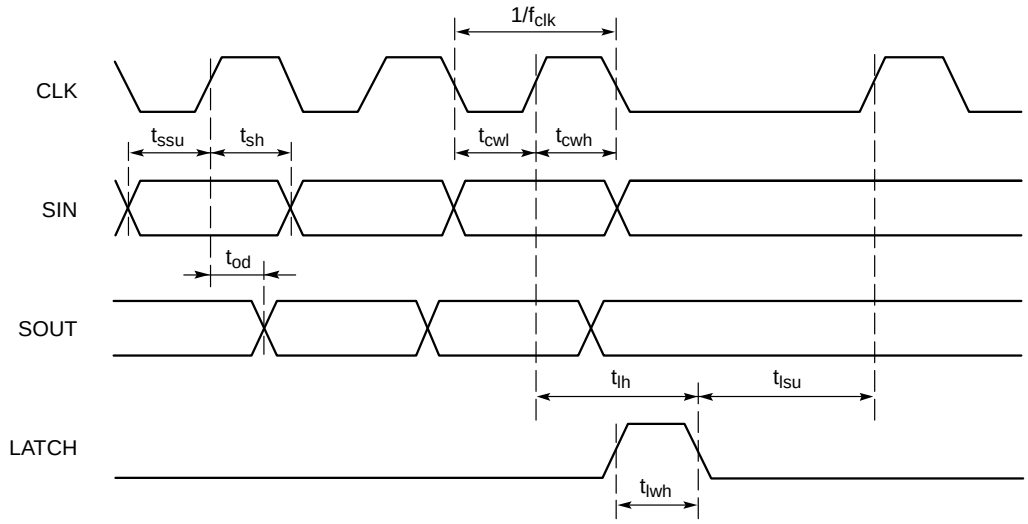

Figure 3. Serial Input Timing Diagram

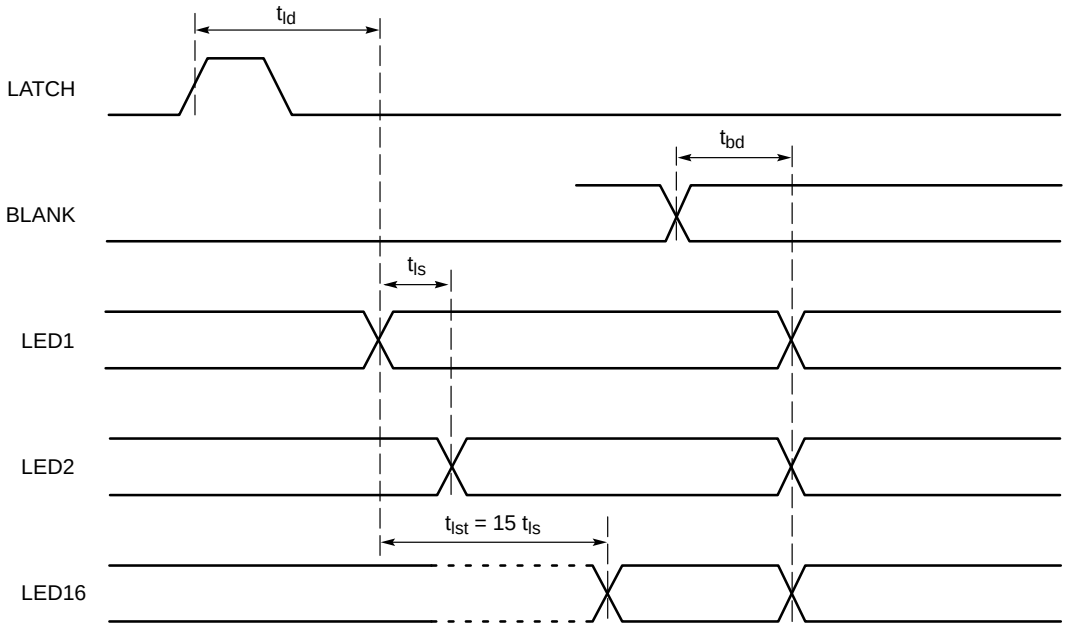

Figure 4. LED Output Timing Diagram

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TYPICAL PERFORMANCE CHARACTERISTICS

(V_{DD} = 5.0 V, LED current 30 mA, all LEDs On, T_{AMB} = 25°C unless otherwise specified.)

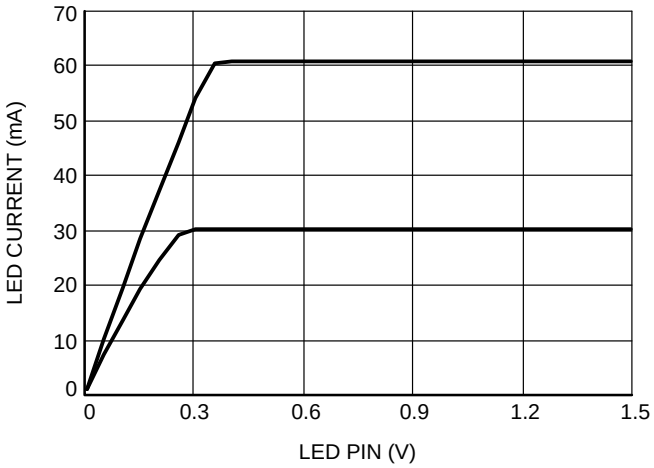

Figure 5. LED Current vs. LED Pin Voltage

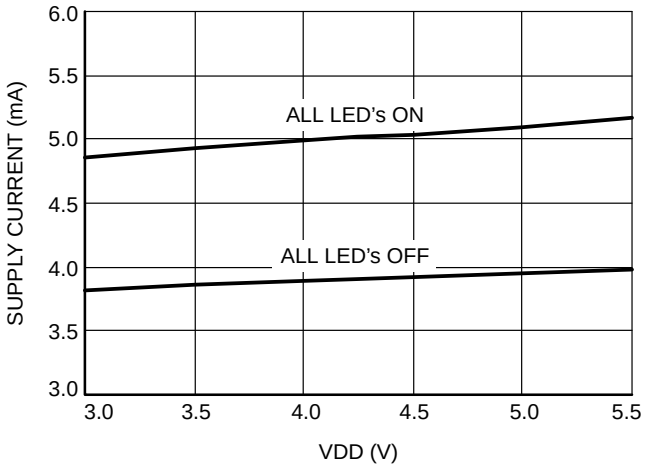

Figure 6. Supply Current vs. VDD Pin Voltage

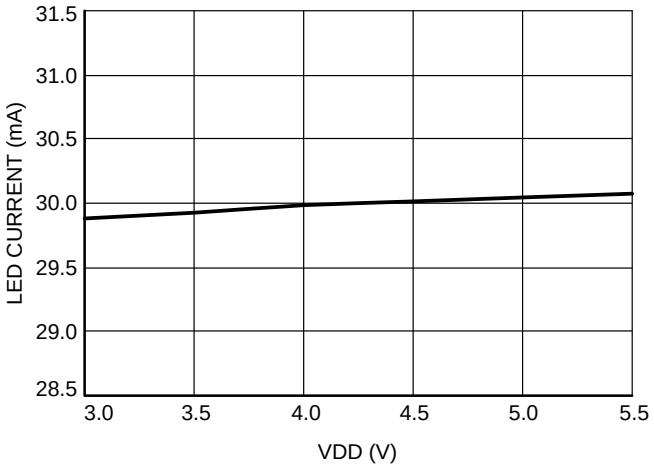

Figure 7. LED Current vs. VDD Pin Voltage

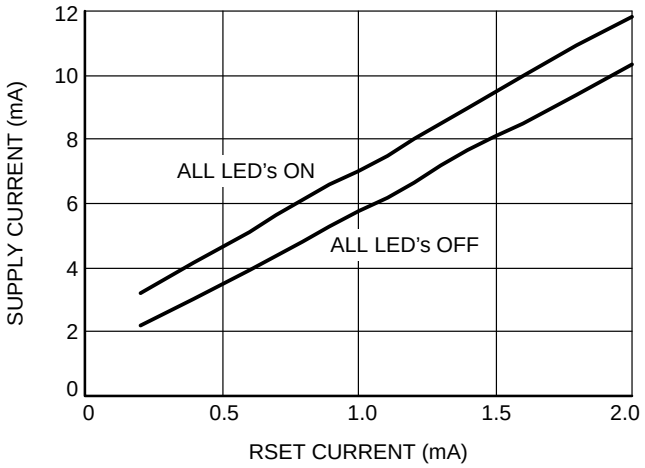

Figure 8. Supply Current vs. RSET Current

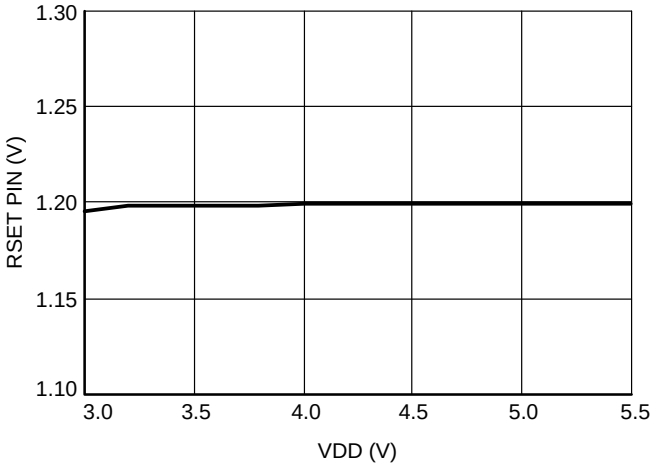

Figure 9. RSET Voltage vs. VDD Pin Voltage

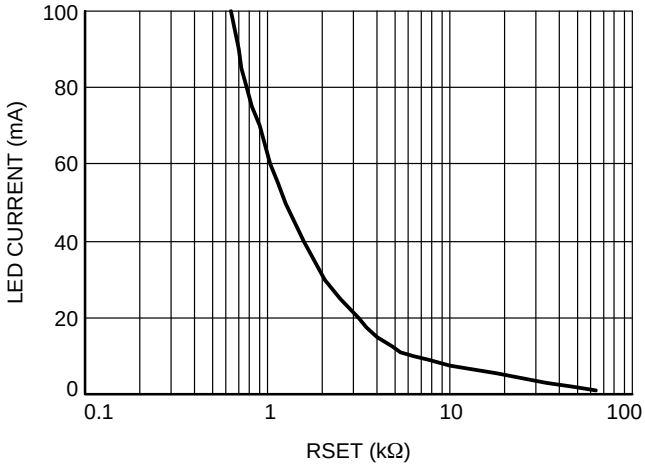

Figure 10. LED Current vs. RSET Resistor

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TYPICAL PERFORMANCE CHARACTERISTICS

(V_{DD} = 5.0 V, LED current 30 mA, all LEDs On, T_{AMB} = 25°C unless otherwise specified.)

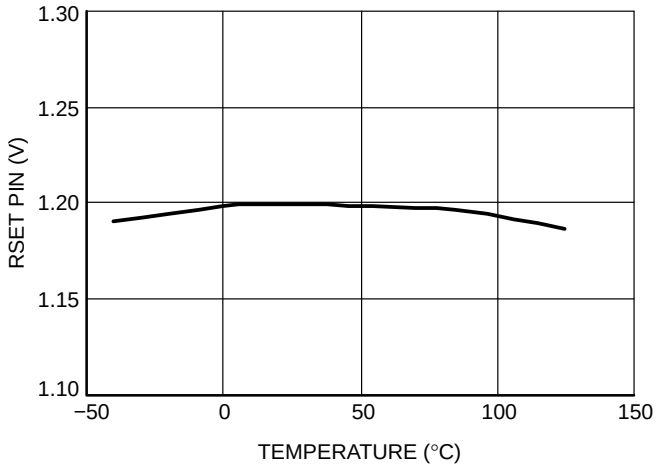

Figure 11. RSET Voltage vs. Temperature

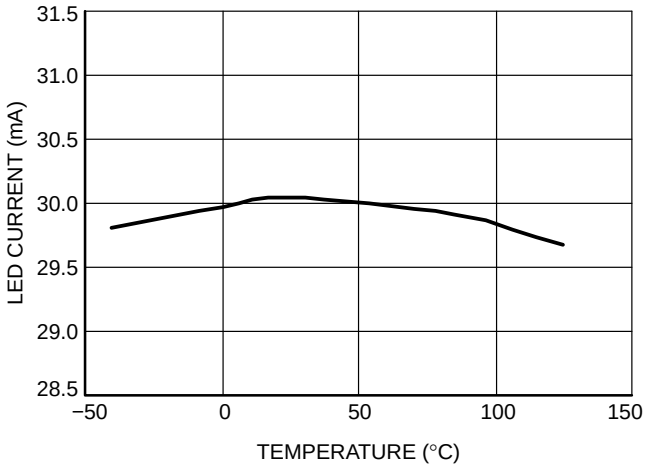

Figure 12. LED Current vs. Temperature

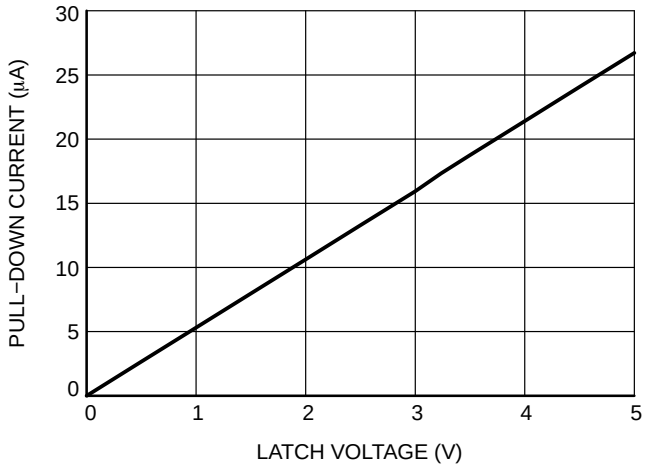

Figure 13. Internal Pull−Down Current (LATCH Pin)

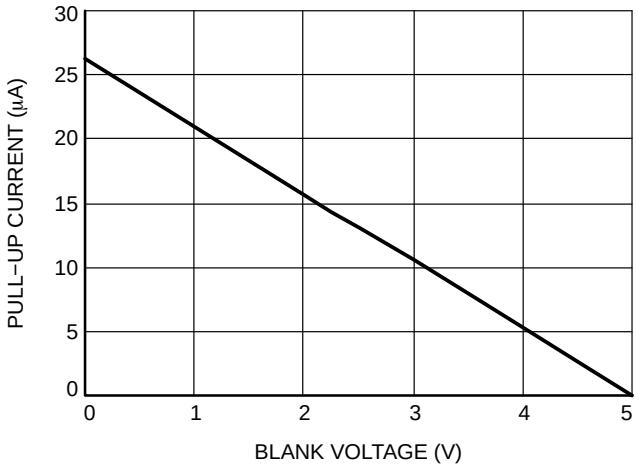

Figure 14. Internal Pull−Up Current (BLANK Pin)

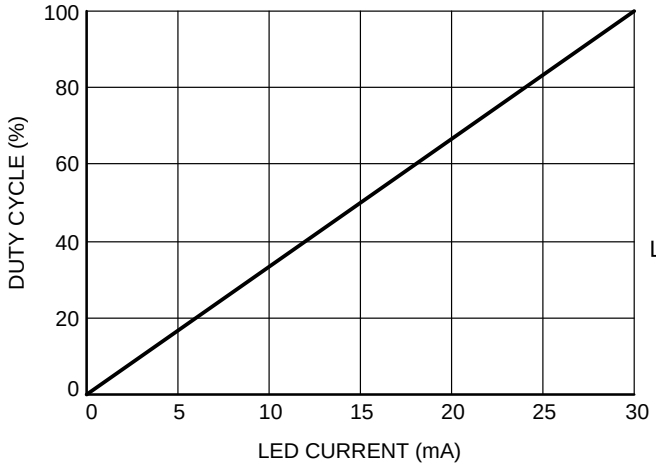

Figure 15. PWM Dimming on BLANK Pin (f = 10 kHz)

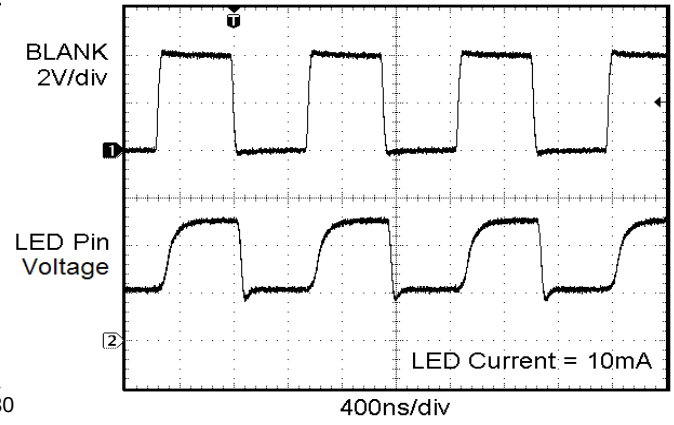

Figure 16. BLANK Transient Response

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Table 5. PIN DESCRIPTION

Name	Function
GND	Ground
SIN	Serial data input pin
CLK	Serial clock input pin
LATCH	Latch serial data to output registers
LED1−LED16	LED channel 1 to 16 cathode terminals
BLANK	Enable / disable all channels
SOUT	Serial data output pin.
RSET	LED current set pin
VDD	Positive supply Voltage
TAB (TQFN package only)	Connect to GND on the PCB

Pin Function

GND is the ground reference pin for the device. This pin must be connected to the ground plane on the PCB.

SIN is the serial data input. Data is loaded into the internal register on each rising edge of CLK.

CLK is the serial clock input. On each rising CLK edge, data is transferred from SIN to the internal 16−bit serial shift register.

LATCH is the latch data input. On the rising edge of LATCH, data is loaded from the 16−bit serial shift register into the output register latch. On the falling edge, this data is latched in the output register and isolated from the state of the serial shift register.

LED1 – LED16 are the LED current sink channels. These pins are connected to the LED cathodes. The current sinks drive the LEDs with a current equal to 50 times RSET pin current. For the LED sink to operate correctly, the voltage on the LED pin must be above 0.4 V.

BLANK is the LED channel enable and disable input pin. When low, LEDs are enabled according to the output latch register content. When high, all LEDs are off, while preserving the data in the output latch register.

SOUT is the serial data output of the 16−bit serial shift register. This pin is used to cascade several devices on the serial bus. The SOUT pin is then connected to the SIN input of the next device on the serial bus to cascade.

RSET is the LED current setting pin. A resistor is connected between this pin and ground. Each LED channel current is set to 50 times the current pulled out of the pin. The RSET pin voltage is regulated to 1.2 V.

VDD is the positive supply pin voltage for the entire device. A small 1 μF ceramic is recommended close to pin.

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Block Diagram

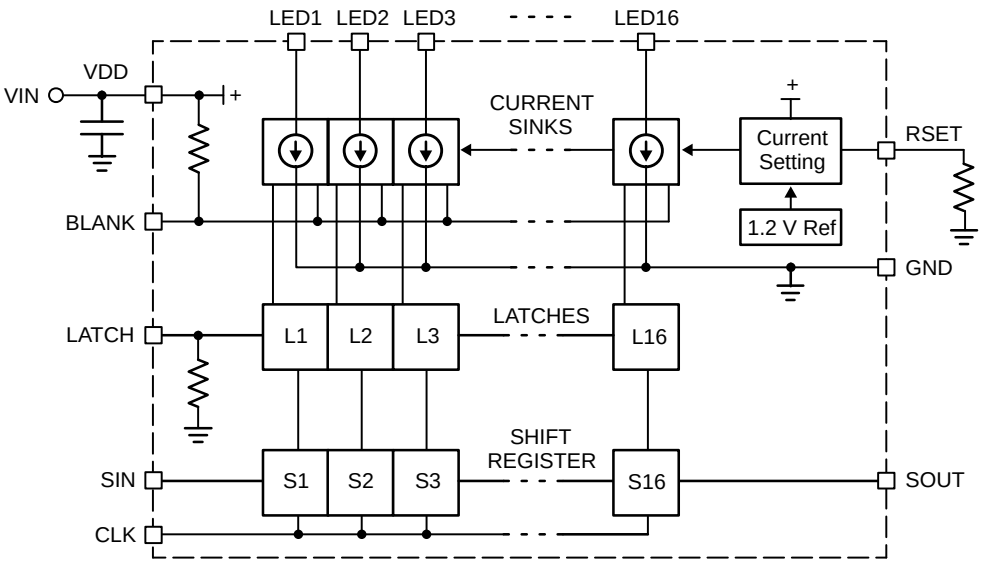

Figure 17. CAT4016 Functional Block Diagram

Basic Operation

The CAT4016 uses 16 tightly matched current sinks to accurately regulate the LED current in each channel. The external resistor, R_{SET}, is used to set the LED channel current to 50 times the current in R_{SET}.

$$\text{LED current} = 50 \times \frac{1.2}{R_{SET}}$$

Tight current regulation for all channels is possible over a wide range of input and LED voltages due to independent current sensing circuitry on each channel. The LED channels have a maximum dropout of 0.4 V for most current and supply voltage conditions. This helps improve the heat dissipation and efficiency of the LED driver.

Upon power−up, an under−voltage lockout circuit clears all latches and shift registers and sets all outputs to off. Once the under−voltage lockout threshold has been reached the device can be programmed.

The driver delays the activation of each consecutive LED output channel by 17 ns (typical). Relative to LED1, LED2 is delayed by 17 ns, LED3 by 34 ns and LED16 by 250 ns typical. The delay is introduced when LATCH is activated. The delay minimizes the inrush current on the LED supply by staggering the turn on and off current spikes over a period of time and therefore allowing usage of smaller bypass capacitors.

Pull−up and pull−down resistors are internally provided to set the state of the BLANK and LATCH pins to the off−state when not externally driven.

Serial Interface

A high−speed serial 4−wire interface is provided to program the state of each LED on or off. The interface contains a 16−bit serial to parallel shift register (S1−S16) and a 16−bit latch (L1−L16). Programming the serial to parallel register is accomplished via SIN and CLK input pins. On each rising edge of the CLK signal, the data from SIN is moved through the shift register serially. Data is also moved out of SOUT which can be connected to a next device if programming more than one device on the same interface.

On the rising edge of LATCH, the data contents of the serial to parallel shift register is reflected in the latches. On the falling edge of LATCH, the state of the serial to parallel register at that particular time is saved in the latches and does not change irrespective of the contents of the serial to parallel register.

BLANK is used to disable all LEDs (turn off) simultaneously while maintaining the same data in the latch register. When low, the LED outputs reflect the data in the latches. When high, all outputs are high impedance (zero current).

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Table 6. ORDERING INFORMATION

Part Number	Package Marking	Package	Shipping†
CAT4016W-T1	CAT4016W	SOIC24 (Note 7) (Pb−Free)	1000 / Tape & Reel
CAT4016Y-T2	CAT4016Y	TSSOP24 (Note 7) (Pb−Free)	2000 / Tape & Reel
CAT4016HV6-T2	LAAA	TQFN24 (Note 7) (Pb−Free)	2000 / Tape & Reel
CAT4016HV6-GT2	LAAD	TQFN24 (Note 8) (Pb−Free)	2000 / Tape & Reel
CAV4016HV6−T2 (Note 3)	VAAA	TQFN24 (Note 7) (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

3. CAV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.
4. All packages are RoHS−compliant (Pb−Free, Halogen−free).
5. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
6. SOIC package availability in 1000 / Tape & Reel. All other packages are 2000 / Tape & Reel.
7. Matte−Tin Plated Finish (RoHS−compliant).
8. NiPdAu Plated Finish (RoHS−compliant).

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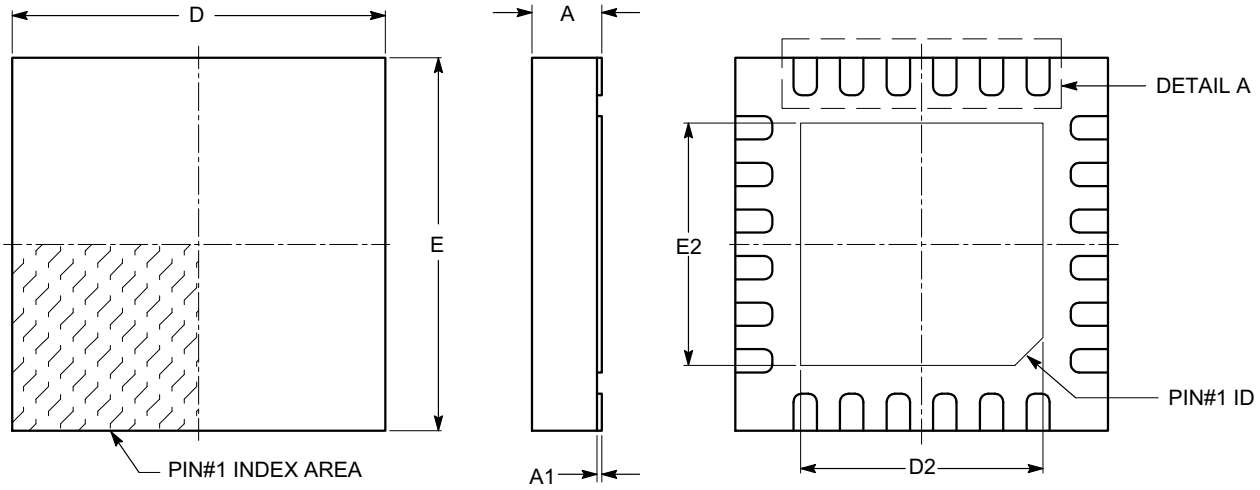
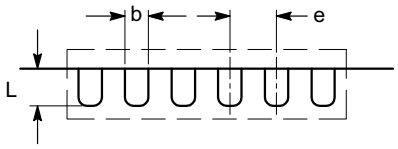
TQFN24, 4x4
CASE 510AG−01
ISSUE B

DATE 04 DEC 2009

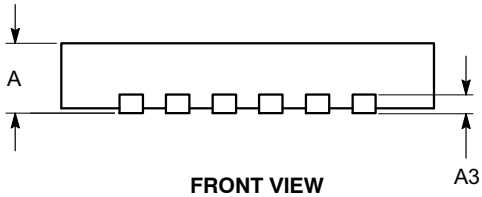


TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00		0.05
A3		0.20 REF	
b	0.20	0.25	0.30
D		4.00 BSC	
D2	2.70	2.80	2.90
E		4.00 BSC	
E2	2.70	2.80	2.90
e		0.50 BSC	
L	0.30		0.50



DETAIL A



FRONT VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MO-220.
(3) Minimum space between leads and flag cannot be smaller than 0.15 mm.

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DESCRIPTION:	**TQFN24, 4X4**	**PAGE 1 OF 1**

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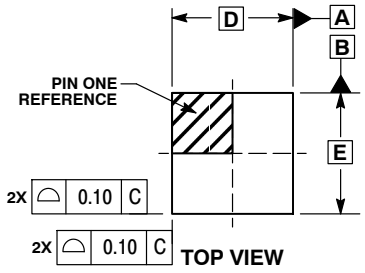
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

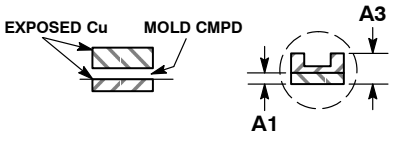
ON Semiconductor®

WQFN24, 4x4, 0.5P
CASE 510BF
ISSUE O

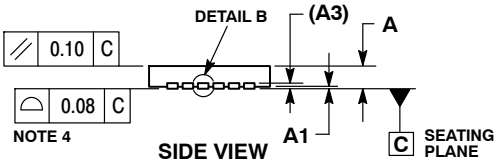
DATE 16 OCT 2013

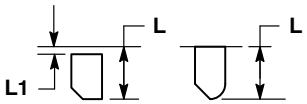
SCALE 2:1



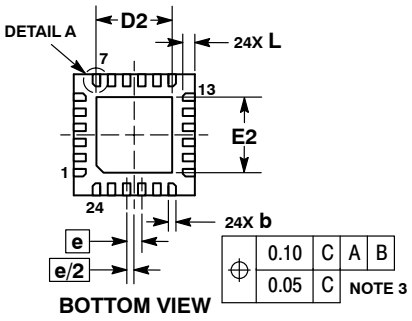


DETAIL B
ALTERNATE CONSTRUCTIONS





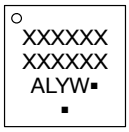
DETAIL A
ALTERNATE CONSTRUCTIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.40	2.60
E	4.00 BSC	
E2	2.40	2.60
e	0.50 BSC	
L	0.30	0.50
L1	0.00	0.15

GENERIC MARKING DIAGRAM*

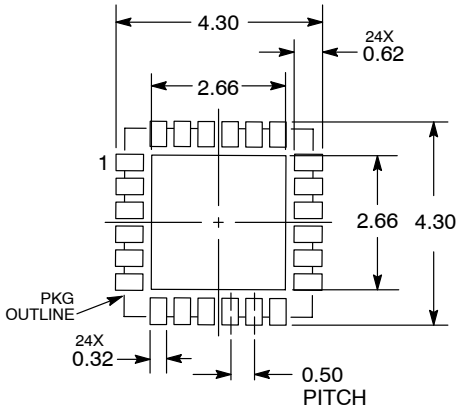


XXXXXX= Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	WQFN24, 4X4, 0.5P	PAGE 1 OF 1

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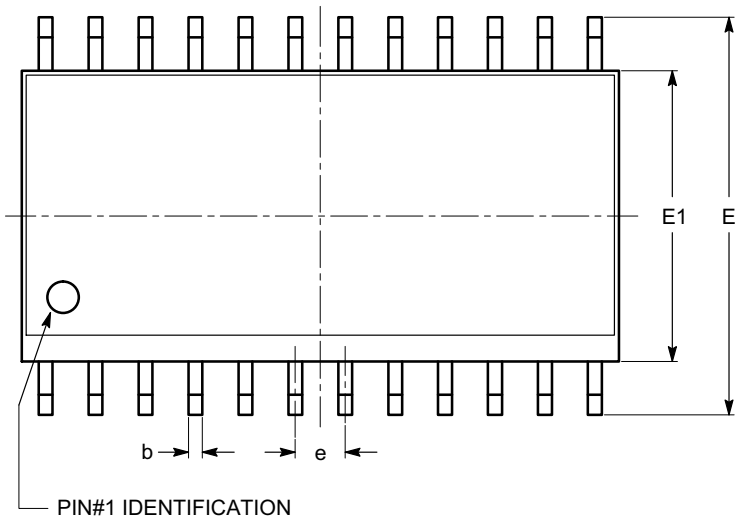
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

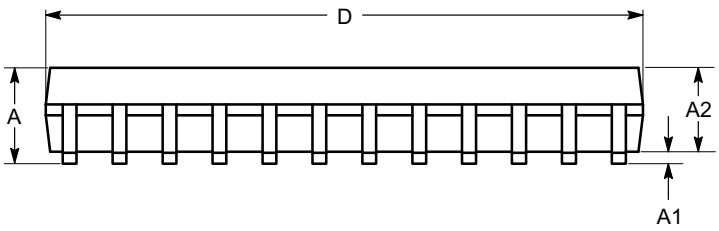
SOIC−24, 300 mils
CASE 751BK−01
ISSUE O

DATE 19 DEC 2008

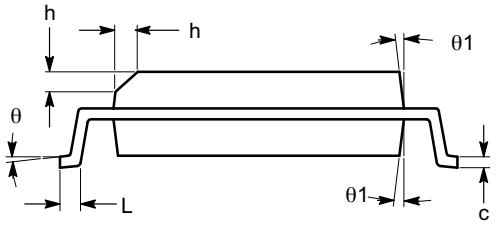


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.35		2.65
A1	0.10		0.30
A2	2.05		2.55
b	0.31		0.51
c	0.20		0.33
D	15.20		15.40
E	10.11		10.51
E1	7.34		7.60
e		1.27 BSC	
h	0.25		0.75
L	0.40		1.27
θ	0°		8°
θ1	5°		15°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-013.

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DESCRIPTION:	SOIC−24, 300 MILS	PAGE 1 OF 1

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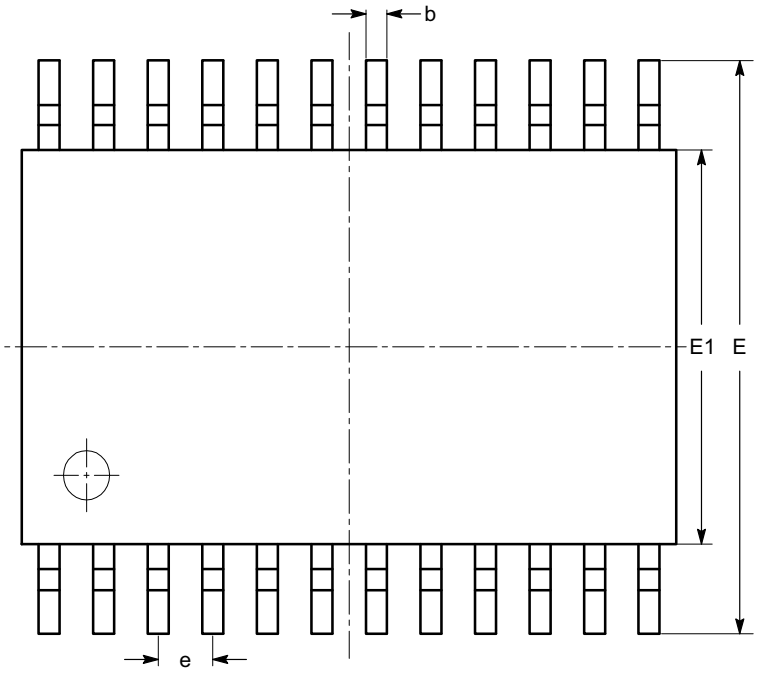
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

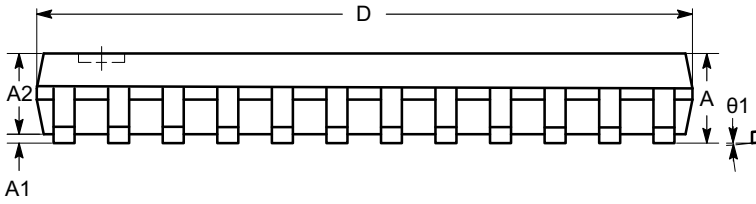
TSSOP24, 4.4x7.8
CASE 948AR−01
ISSUE A

DATE 17 MAR 2009

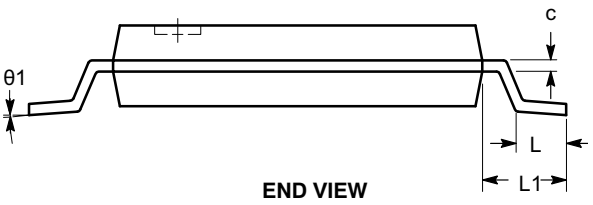


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.50	0.60	0.70
L1		1.00 REF	
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

DOCUMENT NUMBER:	**98AON34454E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TSSOP24, 4.4X7.8**	**PAGE 1 OF 1**

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