

## **N-Channel Power MOSFET** **50V, 30A, 40 mΩ**

This is an N-Channel enhancement mode silicon gate power field effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits.

Formerly developmental type TA9771.

### **Ordering Information**

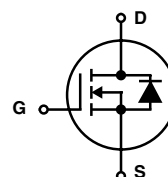
PART NUMBER	PACKAGE	BRAND
BUZ11_NR4941	TO-220AB	BUZ11

NOTE: When ordering, use the entire part number.

### **Features**

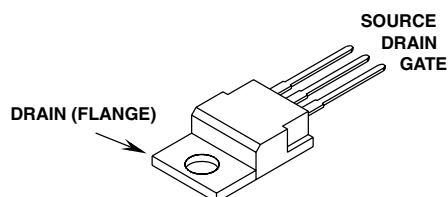
- 30A, 50V
- $r_{DS(ON)} = 0.040\Omega$
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

### **Symbol**



### **Packaging**

#### **JEDEC TO-220AB**



## BUZ11

### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	BUZ11	UNITS
Drain to Source Breakdown Voltage (Note 1) . . . . .	$V_{DS}$	50 V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . .	$V_{DGR}$	50 V
Continuous Drain Current $T_C = 30^\circ\text{C}$ . . . . .	$I_D$	30 A
Pulsed Drain Current (Note 3) . . . . .	$I_{DM}$	120 A
Gate to Source Voltage . . . . .	$V_{GS}$	$\pm 20$ V
Maximum Power Dissipation . . . . .	$P_D$	75 W
Linear Derating Factor . . . . .		0.6 W/ $^\circ\text{C}$
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$	-55 to 150 $^\circ\text{C}$
DIN Humidity Category - DIN 40040 . . . . .	E	
IEC Climatic Category - DIN IEC 68-1 . . . . .	55/150/56	
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s . . . . .	$T_L$	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	$T_{pkg}$	260 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

1.  $T_J = 25^\circ\text{C}$  to  $125^\circ\text{C}$ .

### Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	50	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 1\text{mA}$ (Figure 9)	2.1	3	4	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$T_J = 25^\circ\text{C}$ , $V_{DS} = 50\text{V}$ , $V_{GS} = 0\text{V}$	-	20	250	$\mu\text{A}$
		$T_J = 125^\circ\text{C}$ , $V_{DS} = 50\text{V}$ , $V_{GS} = 0\text{V}$	-	100	1000	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = 20\text{V}$ , $V_{DS} = 0\text{V}$	-	10	100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 15\text{A}$ , $V_{GS} = 10\text{V}$ (Figure 8)	-	0.03	0.04	$\Omega$
Forward Transconductance (Note 2)	$g_{fs}$	$V_{DS} = 25\text{V}$ , $I_D = 15\text{A}$ (Figure 11)	4	8	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{CC} = 30\text{V}$ , $I_D \approx 3\text{A}$ , $V_{GS} = 10\text{V}$ , $R_{GS} = 50\Omega$ , $R_L = 10\Omega$	-	30	45	ns
Rise Time	$t_r$		-	70	110	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	180	230	ns
Fall Time	$t_f$		-	130	170	ns
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$ (Figure 10)	-	1500	2000	pF
Output Capacitance	$C_{OSS}$		-	750	1100	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	250	400	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		$\leq 1.67$			$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		$\leq 75$			$^\circ\text{C/W}$

### Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	$I_{SD}$	$T_C = 25^\circ\text{C}$	-	-	30	A
Pulsed Source to Drain Current	$I_{SDM}$	$T_C = 25^\circ\text{C}$	-	-	120	A
Source to Drain Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}$ , $I_{SD} = 60\text{A}$ , $V_{GS} = 0\text{V}$	-	1.7	2.6	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}$ , $I_{SD} = 30\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$ , $V_R = 30\text{V}$	-	200	-	ns
Reverse Recovery Charge	$Q_{RR}$		-	0.25	-	$\mu\text{C}$

#### NOTES:

2. Pulse Test: Pulse width  $\leq 300\text{ms}$ , duty cycle  $\leq 2\%$ .
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).

**Typical Performance Curves** Unless Otherwise Specified

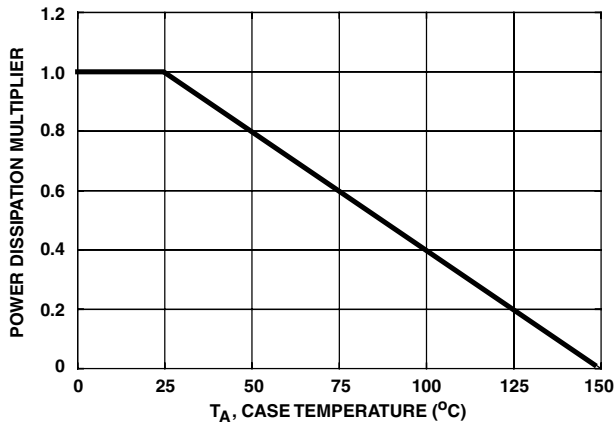


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

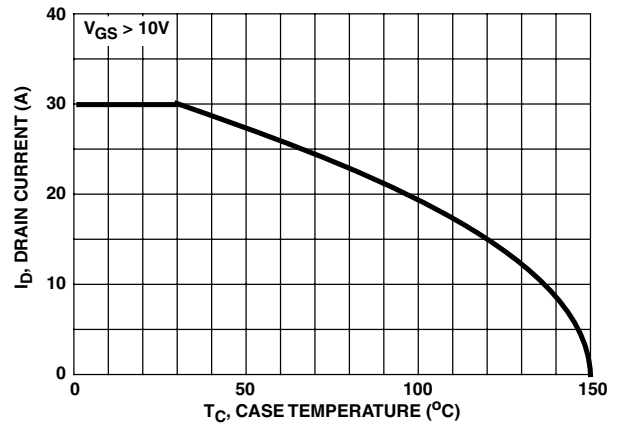


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

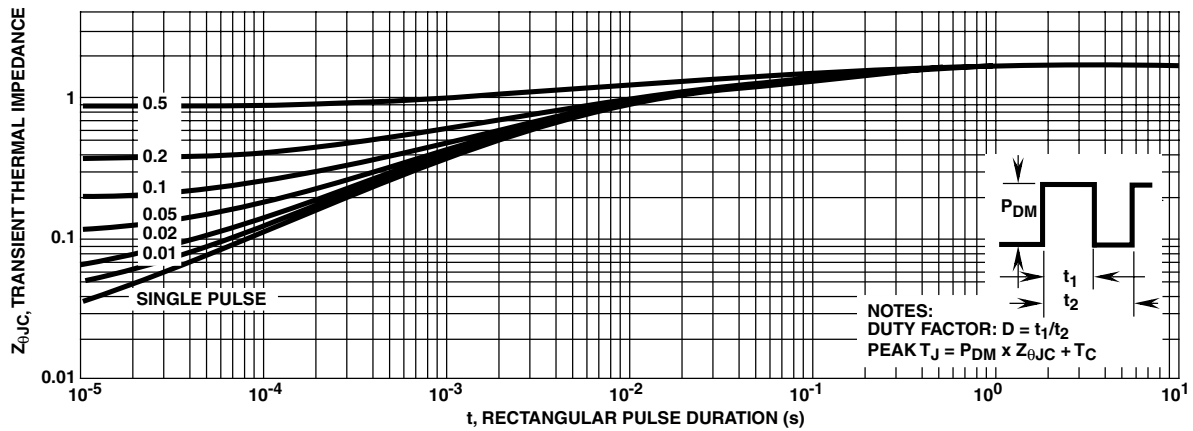


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

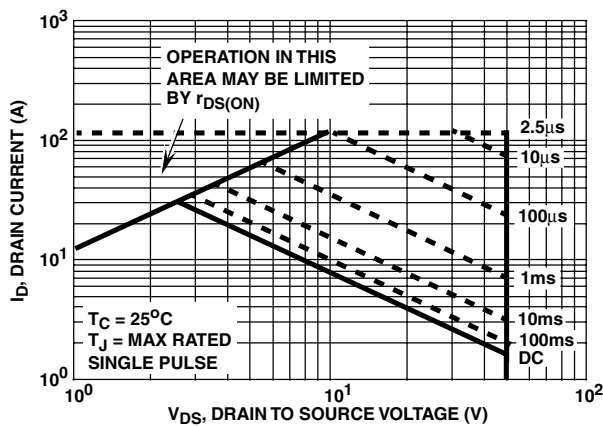


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

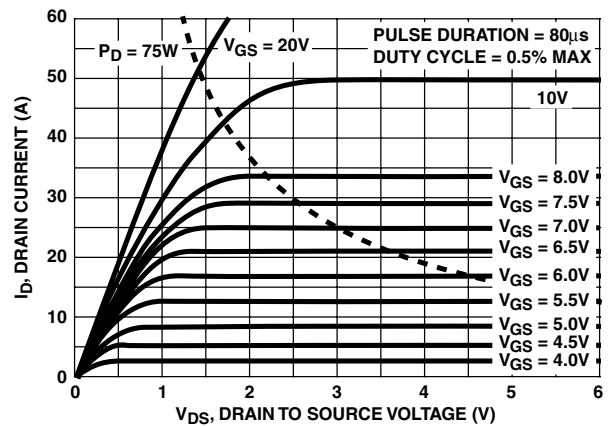


FIGURE 5. OUTPUT CHARACTERISTICS

**Typical Performance Curves** Unless Otherwise Specified (Continued)

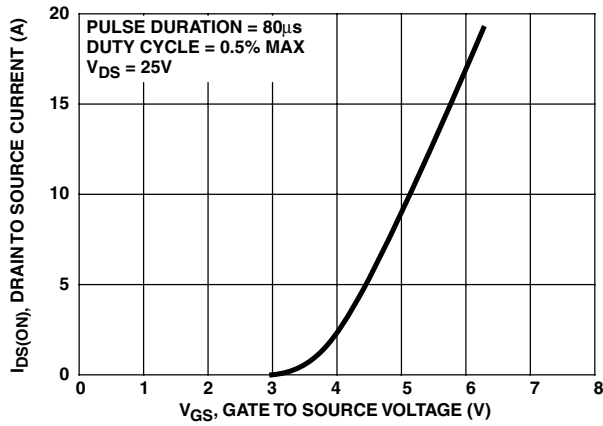


FIGURE 6. TRANSFER CHARACTERISTICS

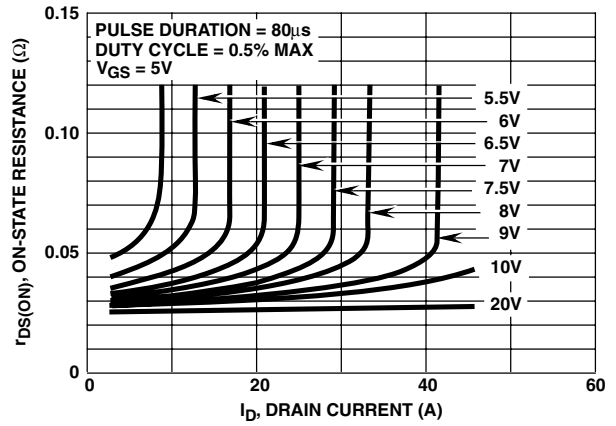


FIGURE 7. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

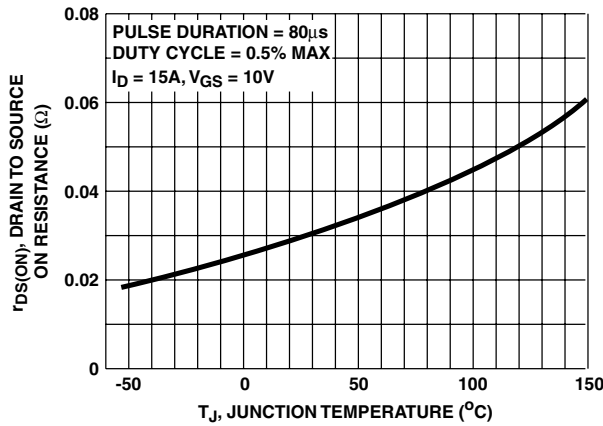


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

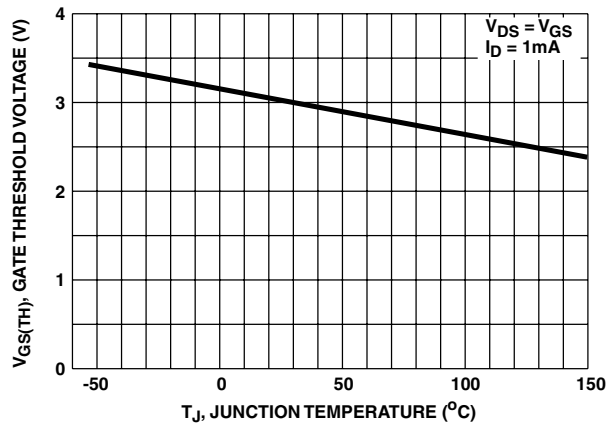


FIGURE 9. GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

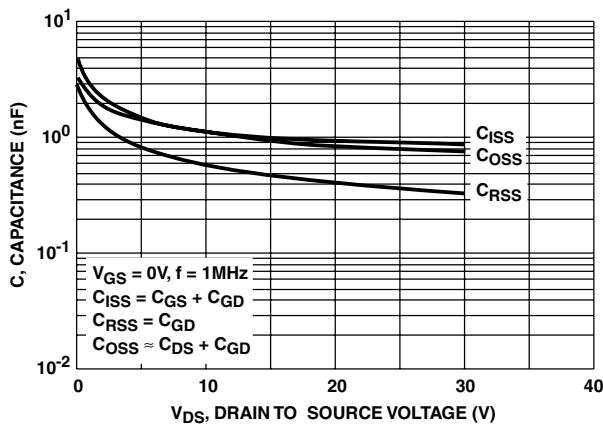


FIGURE 10. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

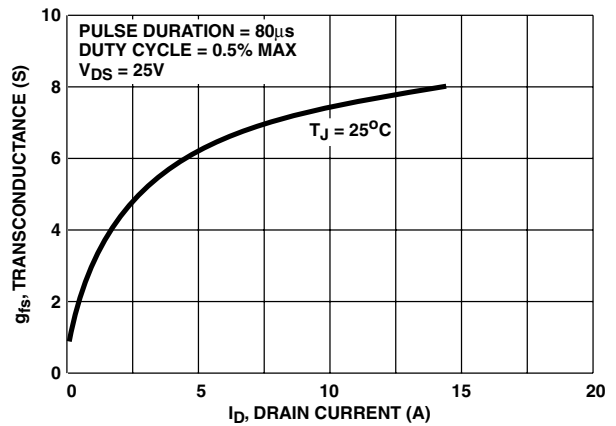


FIGURE 11. TRANSCONDUCTANCE vs DRAIN CURRENT

**Typical Performance Curves** Unless Otherwise Specified (Continued)

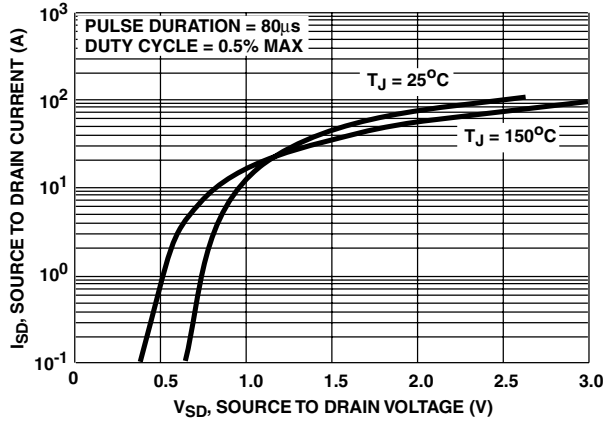


FIGURE 12. SOURCE TO DRAIN DIODE VOLTAGE

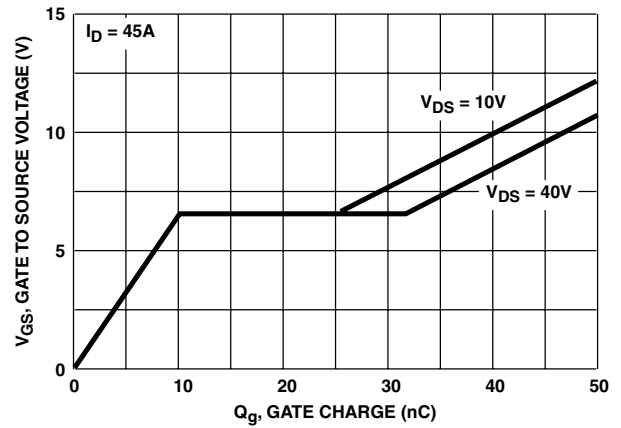


FIGURE 13. GATE TO SOURCE VOLTAGE vs GATE CHARGE

**Test Circuits and Waveforms**

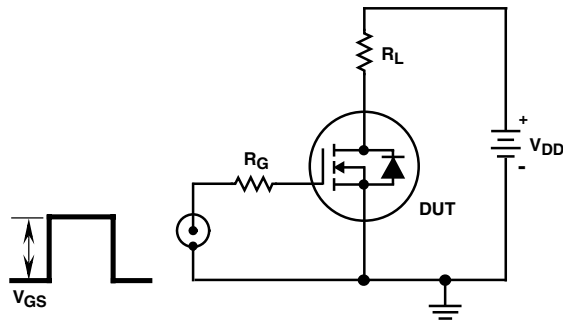


FIGURE 14. SWITCHING TIME TEST CIRCUIT

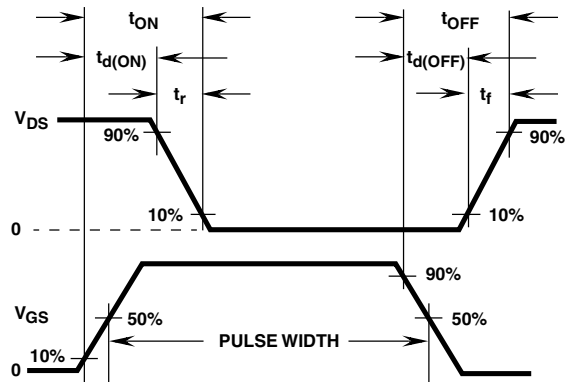


FIGURE 15. RESISTIVE SWITCHING WAVEFORMS

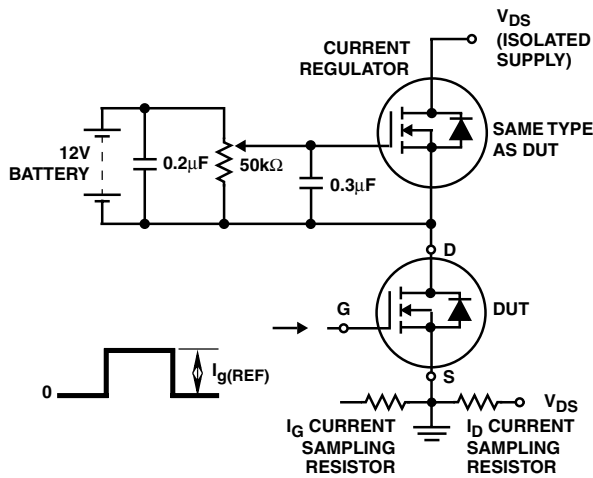


FIGURE 16. GATE CHARGE TEST CIRCUIT

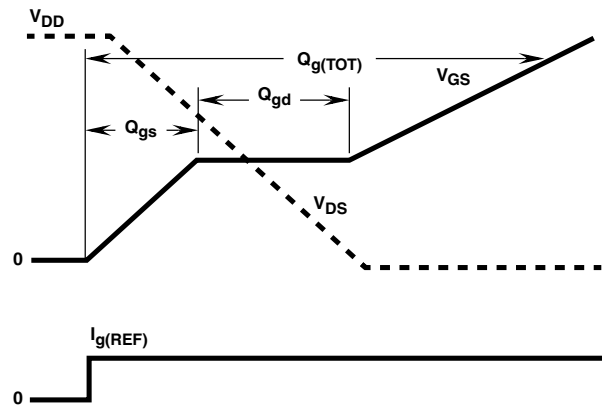




FIGURE 17. GATE CHARGE WAVEFORMS



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