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10/04—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±5 V, V_{REF} = 0 V, R_F = 100 kΩ, R_G = 1 kΩ (@ T_A = 25°C, G = 202, R_L = 10 kΩ, unless otherwise noted).

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
VOLTAGE OFFSET					
RTI Offset, V_{OSI}	$V_{+IN} = V_{-IN}$ = 0 V			10	µV
Offset Drift	$V_{+IN} = V_{-IN}$ = 0 V, T_A = −40°C to +125°C			50	nV/°C
COMMON-MODE REJECTION (CMR)					
CMR to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = −5 V to +5 V	110	120		dB
VOLTAGE OFFSET RTI vs. SUPPLY (PSR)					
G = 2		120	120		dB
G = 202		120	140		dB
GAIN	G = 2(1 + R_F/R_G)				
Gain Range		10[1]		1000	V/V
Gain Error[2]					
G = 2			0.01	0.04	%
G = 10			0.01	0.04	%
G = 100			0.01	0.04	%
G = 1000			0.02	0.05	%
Gain Nonlinearity				20	ppm
Gain Drift					
G = 2, 10, 102				14	ppm/°C
G = 1002				60	ppm/°C
INPUT					
Input Common-Mode Operating Voltage Range		$-V_S$		$+V_S$	V
Over Temperature	T = −40°C to +125°C	$-V_S$		$+V_S$	V
Input Differential Operating Voltage Range			750		mV
Average Input Offset Current[3]	V_{CM} = 0 V		33	300	pA
Average Input Bias Current[3]	V_{CM} = 0 V		0.15	1	nA
OUTPUT					
Output Swing		$-V_S$ + 0.1		$+V_S$ − 0.2	V
Over Temperature	T = −40°C to +125°C	$-V_S$ + 0.1		$+V_S$ − 0.2	V
Short-Circuit Current			15		mA
REFERENCE INPUT					
Voltage Range[4]		$-V_S$ + 3.5		$+V_S$ − 2.5	V
NOISE					
Voltage Noise Density, 1 kHz, RTI	V_{IN+}, V_{IN-}, V_{REF} = 0 V		240		nV/√Hz
Voltage Noise	f = 0.1 Hz to 10 Hz		3		µV p-p
SLEW RATE	V_{IN} = 500 mV, G = 10		2		V/µs
INTERNAL SAMPLE RATE			6		kHz
POWER SUPPLY					
Operating Range (Dual Supplies)		±4		±8	V
Operating Range (Single Supply)		8		16	V
Quiescent Current	T = −40°C to +125°C		2.7	3.5	mA
TEMPERATURE RANGE					
Specified Performance		−40		+125	°C

[1] The AD8230 can operate as low as G = 2. However, since the differential input range is limited to approximately 750 mV, the AD8230 configured at G < 10 does not make use of the full output voltage range.
[2] Gain drift is determined by the TC match of the external gain setting resistors.
[3] Differential source resistance less than 10 kΩ does not result in voltage offset due to input bias current or mismatched series resistors.
[4] For G < 10, the reference voltage range is limited to $-V_S$ + 4.24 V to $+V_S$ − 2.75 V.

V_S = ±8 V, V_{REF} = 0 V, R_F = 100 kΩ, R_G = 1 kΩ (@ T_A = 25°C, G = 202, R_L = 10 kΩ, unless otherwise noted).

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
VOLTAGE OFFSET					
RTI Offset, V_{OSI}	$V_{+IN} = V_{-IN}$ = 0 V			20	µV
Offset Drift	$V_{+IN} = V_{-IN}$ = 0 V, T = −40°C to +125°C			50	nV/°C
COMMON-MODE REJECTION (CMR)					
CMR to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = −8 V to +8 V	110	120		dB
VOLTAGE OFFSET RTI vs. SUPPLY (PSR)					
G = 2		120	120		dB
G = 202		120	140		dB
GAIN	G = 2(1 + R_F/R_G)				
Gain Range		10[1]		1000	V/V
Gain Error[2]					
G = 2			0.01	0.04	%
G = 10			0.01	0.04	%
G = 100			0.01	0.04	%
G = 1000			0.02	0.05	%
Gain Nonlinearity				20	ppm
Gain Drift					
G = 2, 10, 102				14	ppm/°C
G=1002				60	ppm/°C
INPUT					
Input Common-Mode Operating Voltage Range		$-V_S$		$+V_S$	V
Over Temperature	T = −40°C to +125°C	$-V_S$		$+V_S$	V
Input Differential Operating Voltage Range			750		mV
Average Input Offset Current[3]	V_{CM} = 0 V		33	300	pA
Average Input Bias Current[3]	V_{CM} = 0 V		0.15	1	nA
OUTPUT					
Output Swing		$-V_S$ + 0.1		$+V_S$ − 0.2	V
Over Temperature	T = −40°C to +125°C	$-V_S$ + 0.1		$+V_S$ − 0.4	V
Short-Circuit Current			15		mA
REFERENCE INPUT					
Voltage Range[4]		$-V_S$ + 3.5		$+V_S$ − 2.5	V
NOISE					
Voltage Noise Density, 1 kHz, RTI	V_{IN+}, V_{IN-}, V_{REF} = 0 V		240		nV/√Hz
Voltage Noise	f = 0.1 Hz to 10 Hz		3		µV p-p
SLEW RATE	V_{IN} = 500 mV, G = 10		2		V/µs
INTERNAL SAMPLE RATE			6		kHz
POWER SUPPLY					
Operating Range (Dual Supplies)		±4		±8	V
Operating Range (Single Supply)		8		16	V
Quiescent Current	T = −40°C to +125°C		3.2	4	mA
TEMPERATURE RANGE					
Specified Performance		−40		+125	°C

[1] The AD8230 can operate as low as G = 2. However, since the differential input range is limited to approximately 750 mV, the AD8230 configured at G < 10 does not make use of the full output voltage range.
[2] Gain drift is determined by the TC match of the external gain setting resistors.
[3] Differential source resistance less than 10 kΩ does not result in voltage offset due to input bias current or mismatched series resistors.
[4] For G < 10, the reference voltage range is limited to $-V_S$ + 4.24 V to $+V_S$ − 2.75V.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±8 V, +16 V
Internal Power Dissipation	304 mW
Output Short-Circuit Current	20 mA
Input Voltage (Common-Mode)	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Storage Temperature Range	−65°C to +150°C
Operational Temperature Range	−40°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Specification is for device in free air SOIC.

Table 4.

Parameter	Value	Unit
θ_{JA} (4-Layer JEDEC Board)	121	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

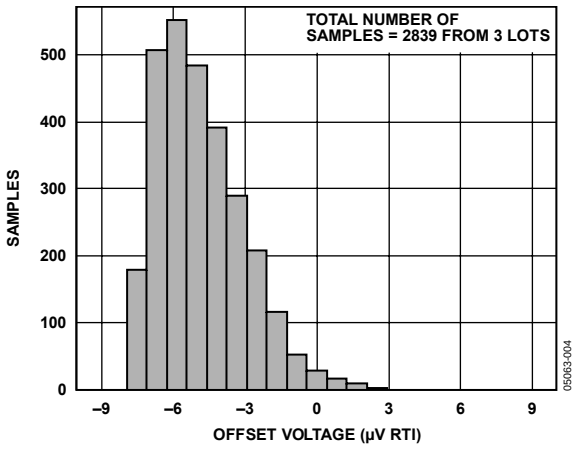

Figure 4. Offset Voltage (RTI) Distribution at ±5 V, CM = 0 V, T_A = 25°C

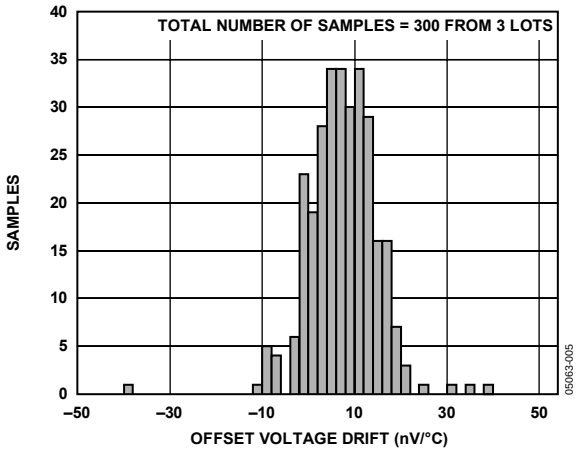

Figure 5. Offset Voltage (RTI) Drift Distribution

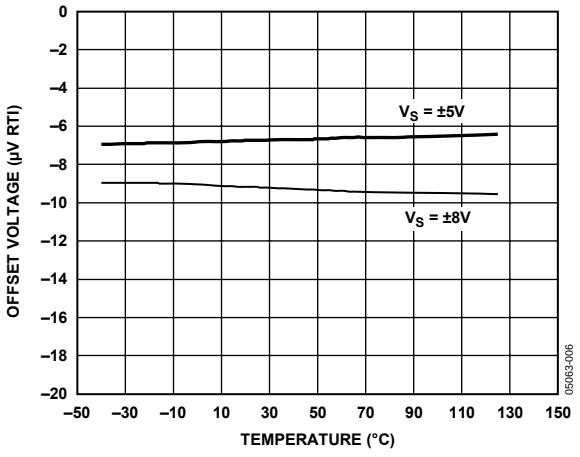

Figure 6. Offset Voltage (RTI) vs. Temperature

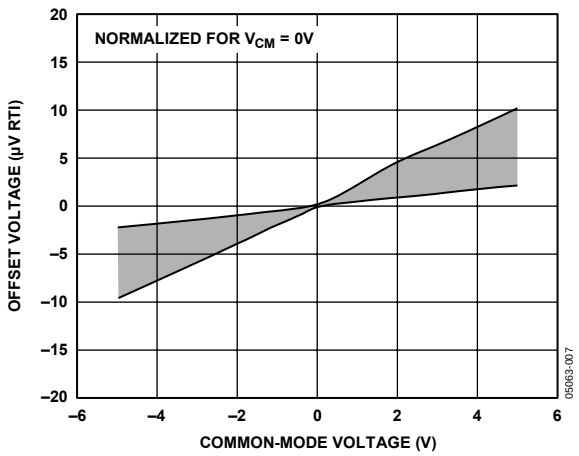

Figure 7. Offset Voltage (RTI) vs. Common-Mode Voltage, V_S = ±5 V

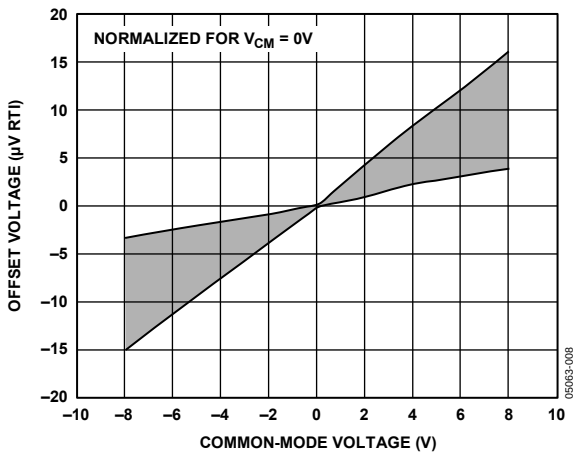

Figure 8. Offset Voltage (RTI) vs. Common-Mode Voltage, V_S = ±8 V

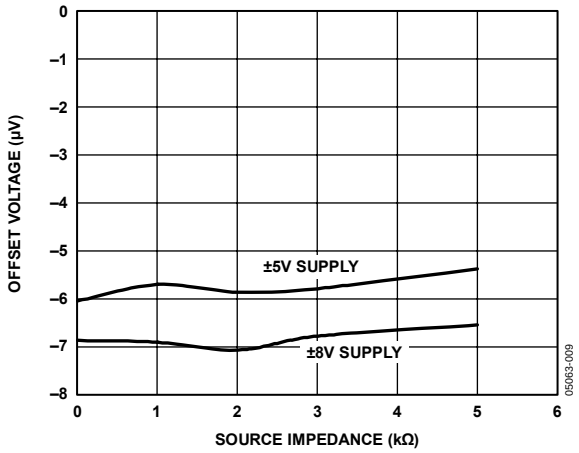

Figure 9. Offset Voltage (RTI) vs. Source Impedance, 1 µF Across Input Pins

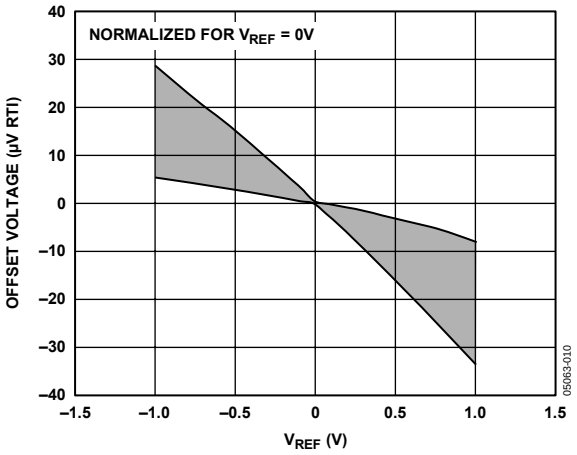

Figure 10. Offset Voltage (RTI) vs. Reference Voltage

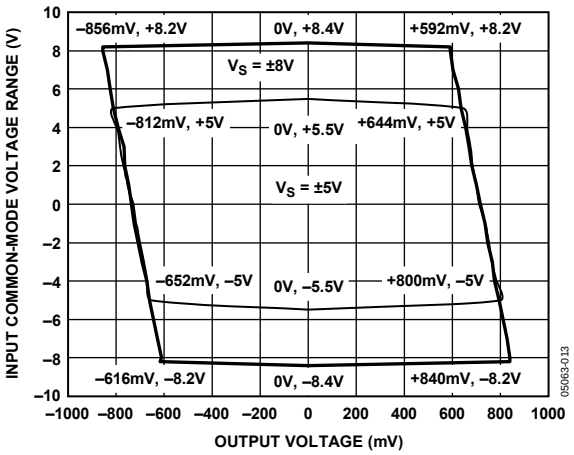

Figure 13. Input Common-Mode Voltage Range vs. Output Voltage, G = 2

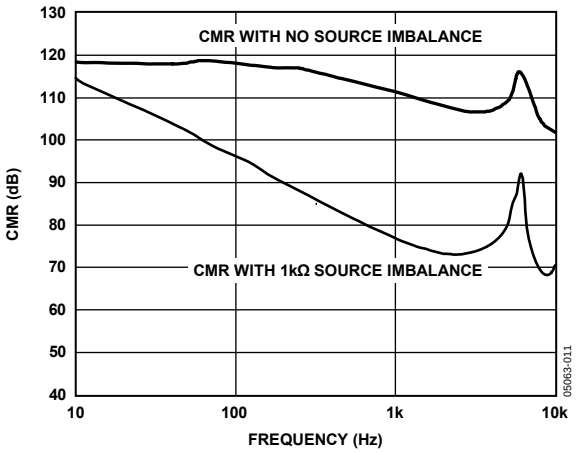

Figure 11. Common-Mode Rejection (CMR) vs. Frequency

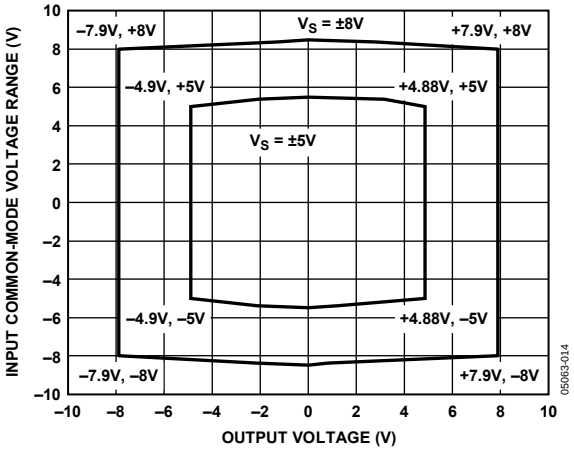

Figure 14. Input Common-Mode Voltage Range vs. Output Voltage, G = 10

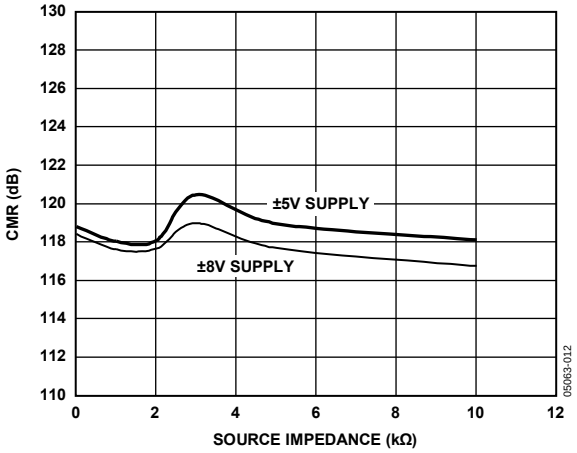

Figure 12. Common-Mode Rejection (CMR) vs. Source Impedance, 1.1 µF Across Input Pins

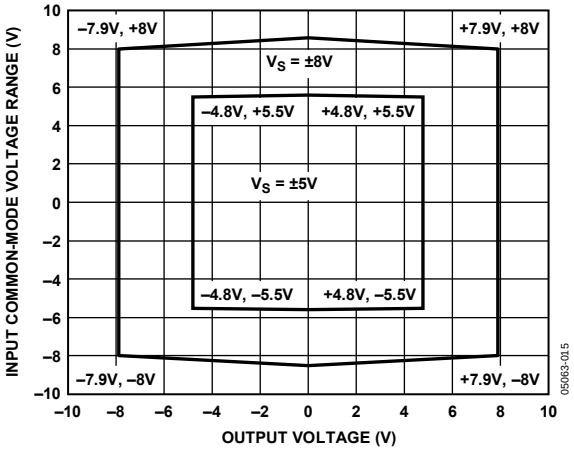

Figure 15. Input Common-Mode Voltage Range vs. Output Voltage, G = 100

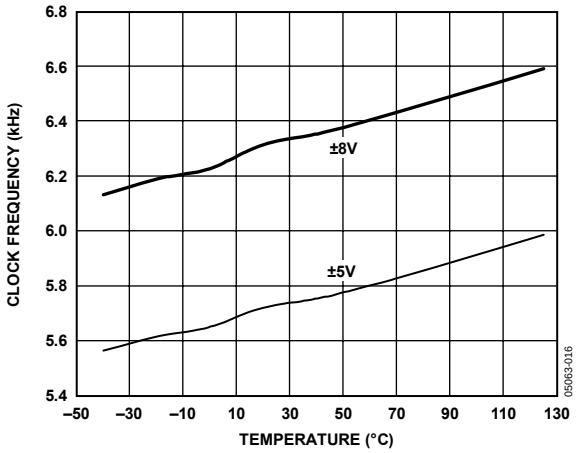

Figure 16. Clock Frequency vs. Temperature

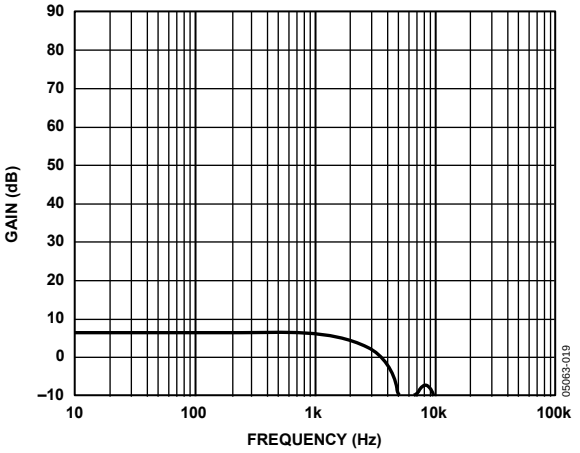

Figure 19. Gain vs. Frequency, G = 2

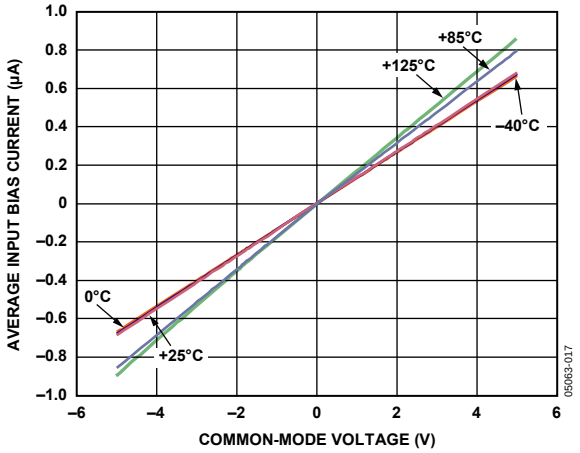

Figure 17. Average Input Bias Current vs. Common-Mode Voltage, −40°C, +25°C, +85°C, +125°C

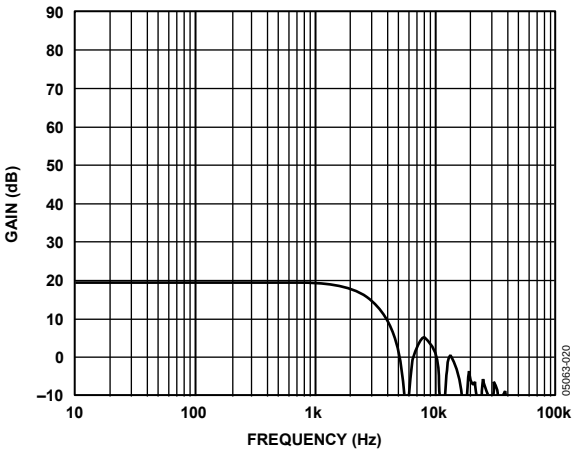

Figure 20. Gain vs. Frequency, G = 10

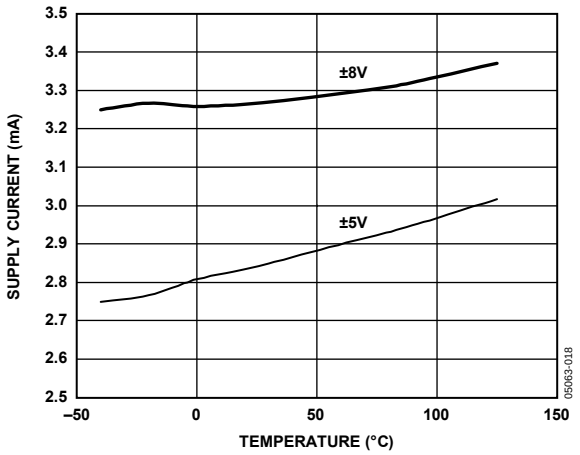

Figure 18. Supply Current vs. Temperature

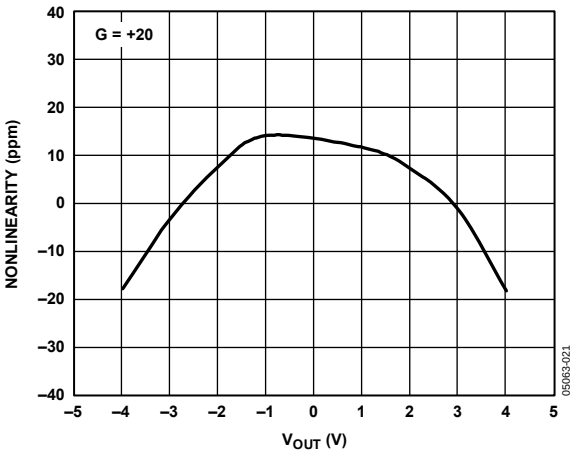

Figure 21. Gain Nonlinearity, G = 20

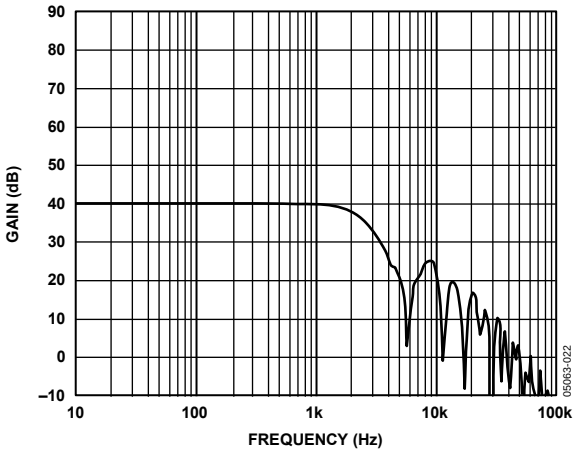

Figure 22. Gain vs. Frequency, G = 100

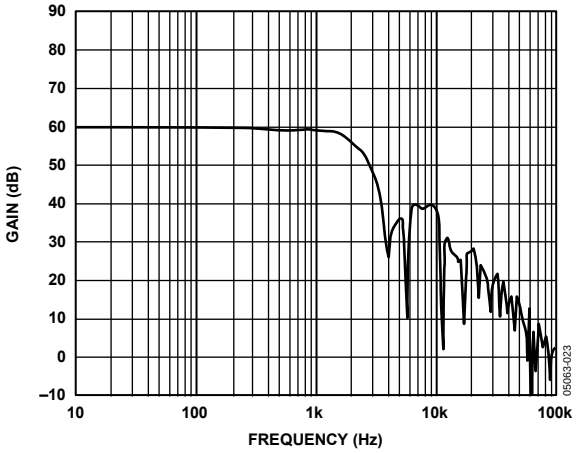

Figure 23. Gain vs. Frequency, G = 1000

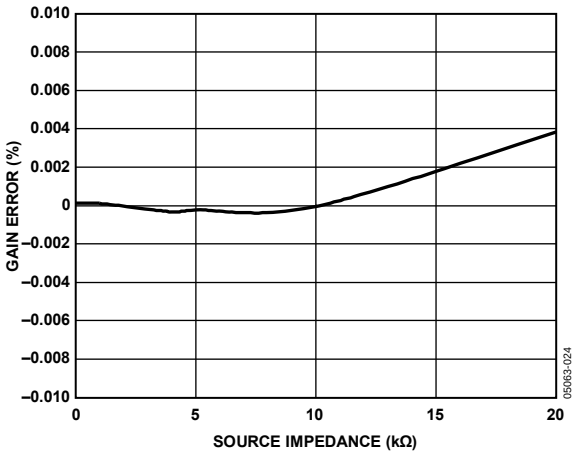

Figure 24. Gain Error vs. Differential Source Impedance

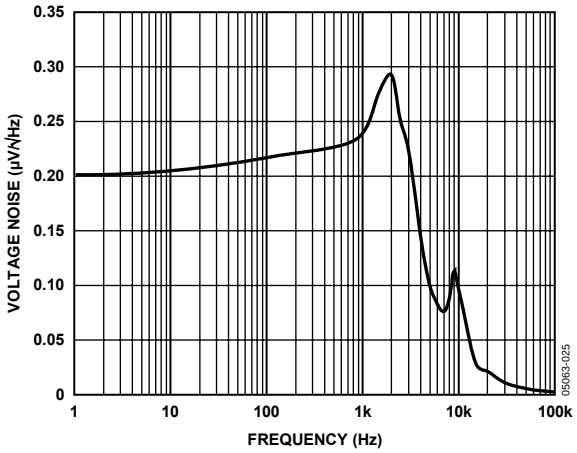

Figure 25. Voltage Noise Spectral Density vs. Frequency

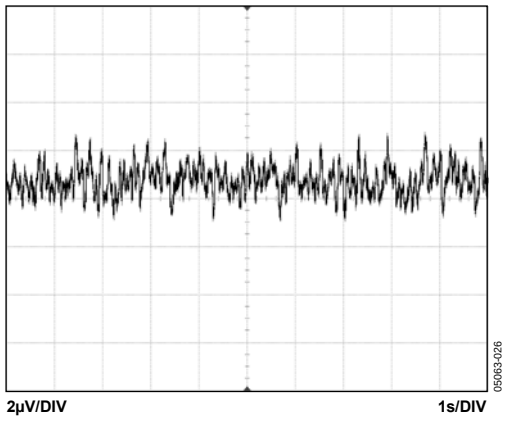

Figure 26. 0.1 Hz to 10 Hz RTI Voltage Noise, G = 100

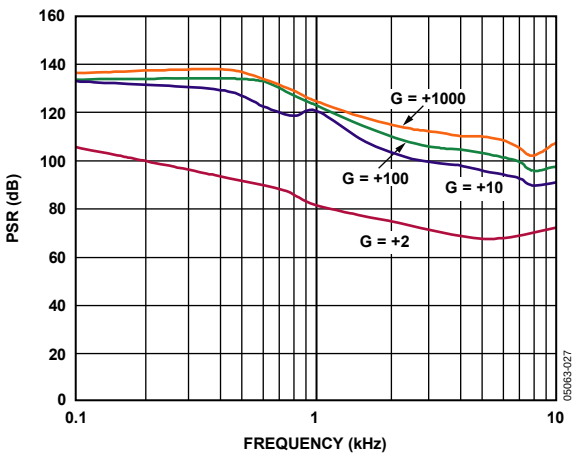

Figure 27. Positive PSR vs. Frequency, RTI

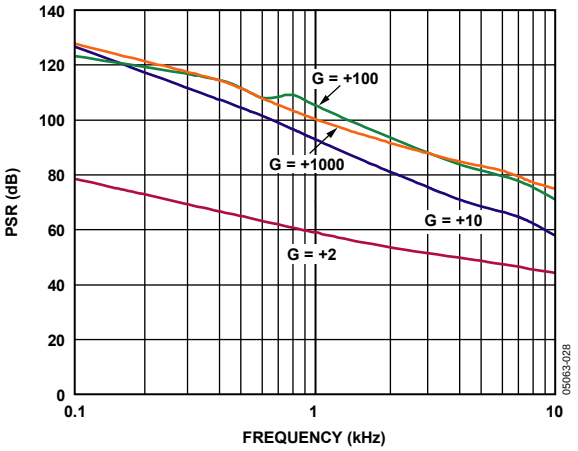

Figure 28. Negative PSR vs. Frequency, RTI

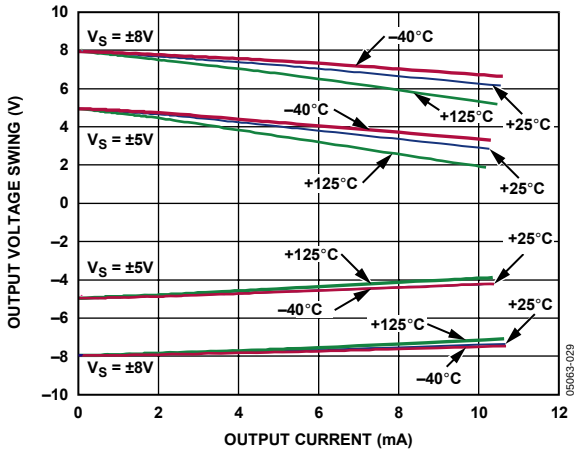

Figure 29. Output Voltage Swing vs. Output Current, −40°C, +25°C, +85°C, +125°C

THEORY OF OPERATION

Auto-zeroing is a dynamic offset and drift cancellation technique that reduces input-referred voltage offset to the μV level and voltage offset drift to the nV/°C level. A further advantage of dynamic offset cancellation is the reduction of low frequency noise, in particular the 1/f component.

The AD8230 is an instrumentation amplifier that uses an auto-zeroing topology and combines it with high common-mode signal rejection. The internal signal path consists of an active differential sample-and-hold stage (preamp) followed by a differential amplifier (gain amp). Both amplifiers implement auto-zeroing to minimize offset and drift. A fully differential topology increases the immunity of the signals to parasitic noise and temperature effects. Amplifier gain is set by two external resistors for convenient TC matching.

The signal sampling rate is controlled by an on-chip, 6 kHz oscillator and logic to derive the required nonoverlapping clock phases. For simplification of the functional description, two sequential clock phases, A and B, are shown to distinguish the order of internal operation, as depicted in Figure 30 and Figure 31, respectively.

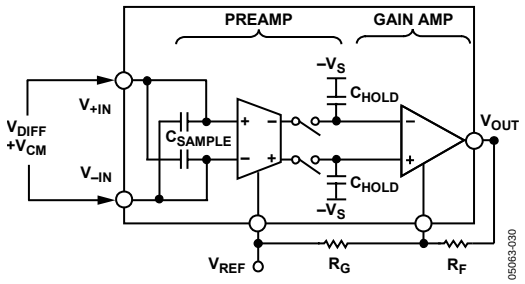

Figure 30. Phase A of the Sampling Phase

During Phase A, the sampling capacitors are connected to the inputs. The input signal's difference voltage, V_{DIFF}, is stored across the sampling capacitors, C_{SAMPLE}. Because the sampling capacitors only retain the difference voltage, the common-mode voltage is rejected. During this period, the gain amplifier is not connected to the preamplifier so its output remains at the level set by the previously sampled input signal held on C_{HOLD}, as shown in Figure 30.

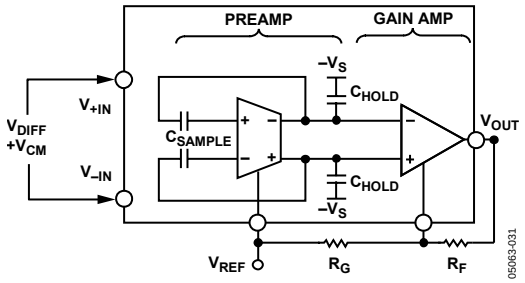

Figure 31. Phase B of the Sampling Phase

In Phase B, the differential signal is transferred to the hold capacitors refreshing the value stored on C_{HOLD}. The output of the preamplifier is held at a common-mode voltage determined by the reference potential, V_{REF}. In this manner, the AD8230 is able to condition the difference signal and set the output voltage level. The gain amplifier conditions the updated signal stored on the hold capacitors, C_{HOLD}.

SETTING THE GAIN

Two external resistors set the gain of the AD8230. The gain is expressed in the following equation:

$$Gain = 2\left(1+\frac{R_F}{R_G}\right) \quad (1)$$

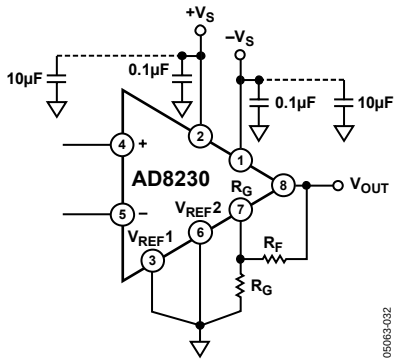

Figure 32. Gain Setting

Table 5. Gains Using Standard 1% Resistors

Gain	R_F	R_G	Actual Gain
2	0 Ω (short)	None	2
10	8.06 kΩ	2 kΩ	10
50	12.1 kΩ	499 Ω	50.5
100	9.76 kΩ	200 Ω	99.6
200	10 kΩ	100 Ω	202
500	49.9 kΩ	200 Ω	501
1000	100 kΩ	200 Ω	1002

Figure 32 and Table 5 provide an example of some gain settings. As Table 5 shows, the AD8230 accepts a wide range of resistor values. Because the instrumentation amplifier has finite driving capability, ensure that the output load in parallel with the sum of the gain setting resistors is greater than 2 kΩ.

$$R_L||(R_F + R_G) > 2\ \text{k}\Omega \quad (2)$$

Offset voltage drift at high temperature can be minimized by keeping the value of the feedback resistor, R_F, small. This is due to the junction leakage current on the R_G pin, Pin 7. The effect of the gain setting resistor on offset voltage drift is shown in Figure 33. In addition, experience has shown that wire-wound resistors in the gain feedback loop may degrade the offset voltage performance.

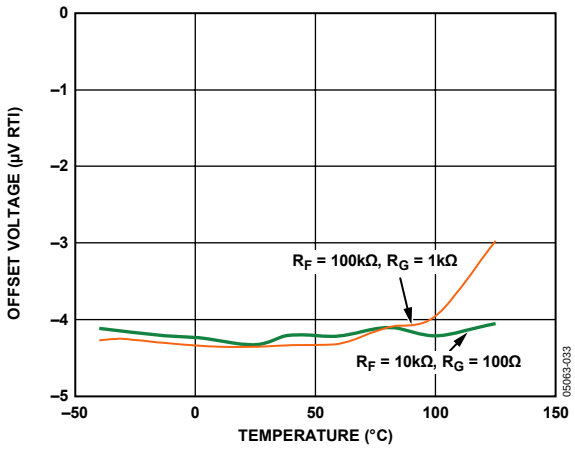

Figure 33. Effect of Feedback Resistor on Offset Voltage Drift

LEVEL-SHIFTING THE OUTPUT

A reference voltage, as shown in Figure 34, can be used to level-shift the output. The reference voltage, V_R, is limited to $-V_S + 3.5$ V to $+V_S - 2.5$ V. (For G < 10, the reference voltage range is limited to $-V_S + 4.24$ V to $+V_S - 2.75$ V.) Otherwise, it is nominally tied to midsupply. The voltage source used to level-shift the output should have a low output impedance to avoid contributing to gain error. In addition, it should be able to source and sink current. To minimize offset voltage, the V_{REF} pins should be connected either to the local ground or to a reference voltage source that is connected to the local ground.

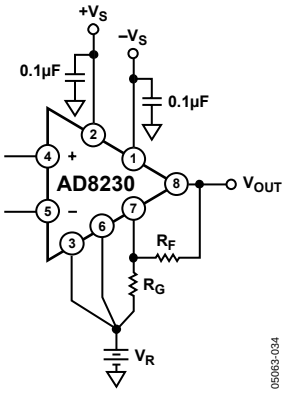

Figure 34. Level-Shifting the Output

The output can also be level-shifted by adding a resistor, R_O, as shown in Figure 35. The benefit is that the output can be level-shifted to as low as 100 mV of the negative supply rail and to as high as 200 mV of the positive supply rail, increasing unipolar output swing. This can be useful in applications, such as strain gauges, where the force is only applied in one direction. Another benefit of this configuration is that a supply rail can be used for $V_{R'}$ eliminating the need to add an additional external reference voltage.

The gain changes with the inclusion of R_O. The full expression is

$$V_{OUT} = 2\left(\frac{R_F}{R_G \,||\, R_O}+1\right)V_{IN} - \frac{R_F}{R_O}V_{R'} = 2\left(\frac{R_F(R_G+R_O)}{R_G R_O}+1\right)V_{IN} - \frac{R_F}{R_O}V_{R'} \quad (3)$$

The following steps can be taken to set the gain and level-shift the output:

1. Select an R_F value. Table 5 shows R_F values for various gains.
2. Solve for R_O using Equation 4.

$$R_O = -\frac{V_{R'} \times R_F}{V_{DESIRED-LEVEL}} \quad (4)$$

where:
$V_{R'}$ is a voltage source, such as a supply voltage.
$V_{DESIRED-LEVEL}$ is the desired output bias voltage.

3. Solve for R_G.

$$R_G = \frac{R_O}{\left(\frac{Gain}{2}-1\right)\frac{R_O}{R_F}-1} \quad (5)$$

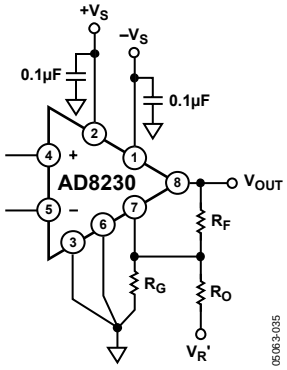

Figure 35. Level-Shifting the Output Without an Additional Voltage Reference

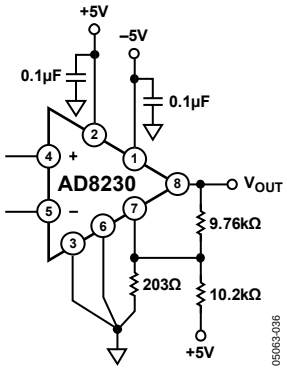

Figure 36. An AD8230 with its Output Biased at –4.8 V; G = 100; $V_{DESIRED-LEVEL}$ = –4.8 V

SOURCE IMPEDANCE AND INPUT SETTLING TIME

The input stage of the AD8230 consists of two actively driven, differential switched capacitors, as described in Figure 30 and Figure 31. Differential input signals are sampled on C_{SAMPLE} such that the associated parasitic capacitances, 70 pF, are balanced between the inputs to achieve high common-mode rejection. On each sample period (approximately 85 µs), these parasitic capacitances must be recharged to the common-mode voltage by the signal source impedance (10 kΩ maximum). If resistors and capacitors are used at the input of the AD8230, care should be taken to maintain close match to maximize CMRR.

INPUT VOLTAGE RANGE

The input common-mode range of the AD8230 is rail to rail. However, the differential input voltage range is limited to approximately 750 mV. The AD8230 does not phase invert when its inputs are overdriven.

INPUT PROTECTION

The input voltage is limited to within 0.6 V beyond the supply rails by the internal ESD protection diodes. Resistors and low leakage diodes can be used to limit excessive, external voltage and current from damaging the inputs, as shown in Figure 37. Figure 39 shows an overvoltage protection circuit between the thermocouple and the AD8230.

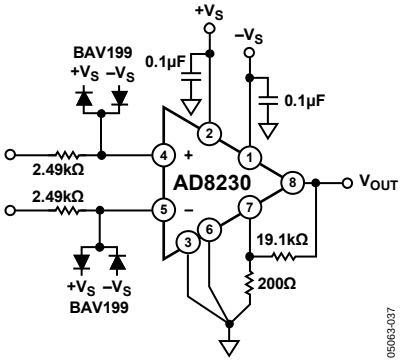

Figure 37. Overvoltage Input Protection

POWER SUPPLY BYPASSING

A regulated dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. Bypass capacitors should be used to decouple the amplifier.

The AD8230 has internal clocked circuitry that requires adequate supply bypassing. A 0.1 µF capacitor should be placed as close to each supply pin as possible. As shown in Figure 32, a 10 µF tantalum capacitor can be used further away from the part.

POWER SUPPLY BYPASSING FOR MULTIPLE CHANNEL SYSTEMS

The best way to prevent clock interference in multichannel systems is to lay out the PCB with a star node for the positive supply and a star node for the negative supply. Using such a technique, crosstalk between clocks is minimized. If laying out star nodes is not feasible, use wide traces to minimize parasitic inductance and decouple frequently along the power supply traces. Examples are shown in Figure 38. Care and forethought go a long way in maximizing performance.

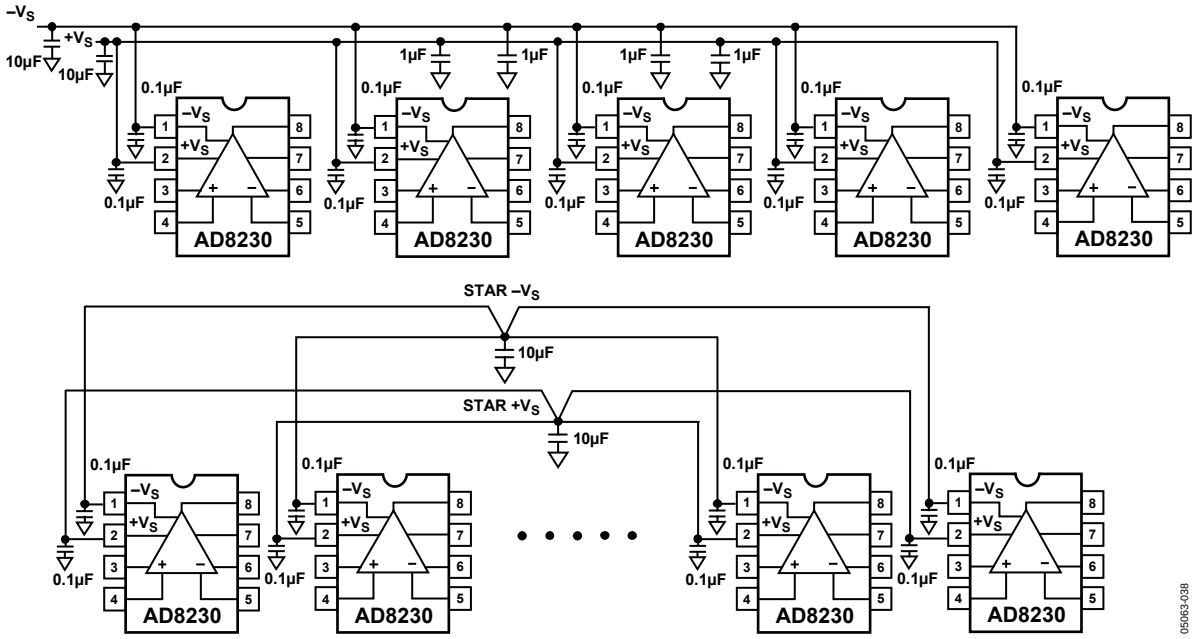

Figure 38. Use Star Nodes for +VS and –VS or Use Thick Traces and Decouple Frequently Along the Supply Lines

LAYOUT

The AD8230 has two reference pins: $V_{REF}1$ and $V_{REF}2$. $V_{REF}1$ draws current to set the internal voltage references. In contrast, $V_{REF}2$ does not draw current. It sets the common mode of the output signal. As such, $V_{REF}1$ and $V_{REF}2$ should be star-connected to ground (or to a reference voltage). In addition, to maximize CMR, the trace between $V_{REF}2$ and the gain resistor, R_G, should be kept short.

APPLICATIONS

The AD8230 can be used in thermocouple applications, as shown in Figure 3 and Figure 39. Figure 39 is an example of such a circuit for use in an industrial environment. Series resistors and low leakage diodes serve to clamp overload voltages (see the Input Protection section for more information).

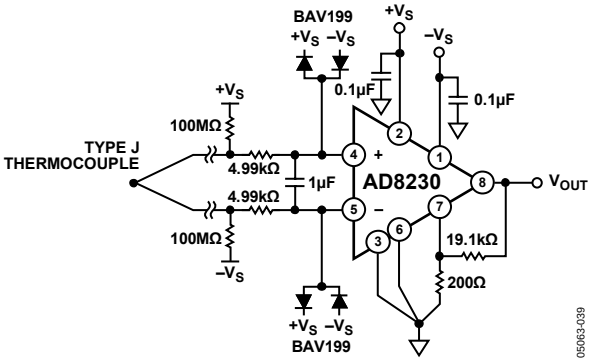

Figure 39. Type J Thermocouple with Overvoltage Protection and RFI Filter

An antialiasing filter reduces unwanted high frequency signals. The matched 100 MΩ resistors serve to provide input bias current to the input transistors and serve as an indicator as to when the thermocouple connection is broken. Well-matched 1% 4.99 kΩ resistors are used to form the antialiasing filter. It is good practice to match the source impedances to ensure high CMR. The circuit is configured for a gain of 193, which provides an overall temperature sensitivity of 10 mV/°C.

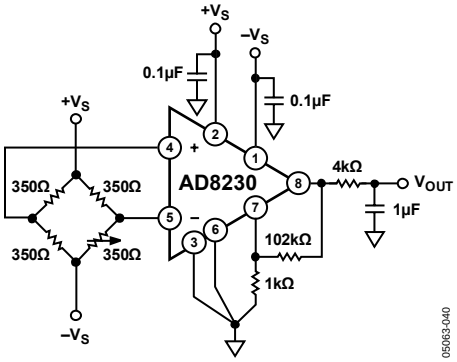

Figure 40. Bridge Measurement with Filtered Output

Measuring load cells in industrial environments can be a challenge. Often, the load cell is located some distance away from the instrumentation amplifier. The common-mode potential can be several volts, exceeding the common-mode input range of many 5 V auto-zero instrumentation amplifiers. Fortunately, the wide common-mode input voltage range of the AD8230 spans 16 V, relieving designers of having to worry about the common-mode range.

OUTLINE DIMENSIONS

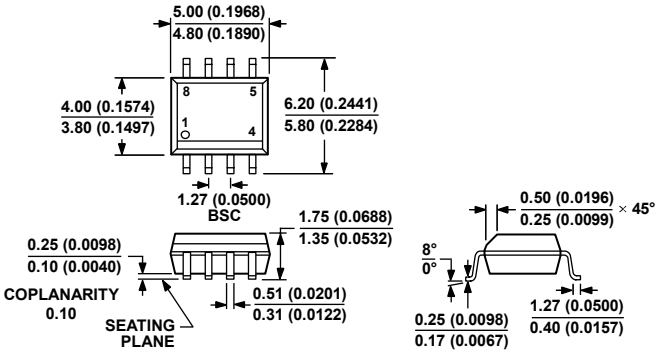

Figure 41. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8230YRZ[1]	−40°C to +125°C	8-Lead SOIC_N	R-8
AD8230YRZ-REEL[1]	−40°C to +125°C	8-Lead SOIC_N, 13" Tape and Reel	R-8
AD8230YRZ-REEL7[1]	−40°C to +125°C	8-Lead SOIC_N, 7" Tape and Reel	R-8
AD8230-EVAL		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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